Rail-to-Rail, Very Fast, 2.5 V to 5.5 V, Single-Supply LVDS Comparators

ADCMP604/ADCMP605

FEATURES

Fully specified rail to rail at V_{CCI} = 2.5 V to 5.5 V
Input common-mode voltage from −0.2 V to V_{CCI} + 0.2 V
Low glitch LVDS-compatible output stage
1.6 ns propagation delay
37 mW at 2.5 V
Shutdown pin
Single-pin control for programmable hysteresis and latch
Power supply rejection > 60 dB
−40°C to +125°C operation

APPLICATIONS

High speed instrumentation
Clock and data signal restoration
Logic level shifting or translation
Pulse spectroscopy
High speed line receivers
Threshold detection
Peak and zero-crossing detectors
High speed trigger circuitry
Pulse-width modulators
Current-/voltage-controlled oscillators
Automatic test equipment (ATE)

FUNCTIONAL BLOCK DIAGRAM

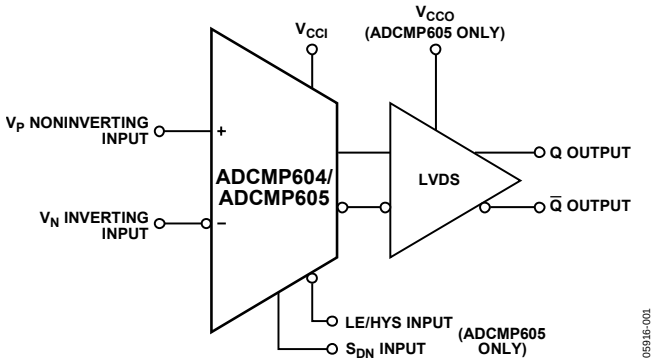

Figure 1.

GENERAL DESCRIPTION

The ADCMP604/ADCMP605 are very fast comparators fabricated on the Analog Devices, Inc. proprietary XFCB2 process. These comparators are exceptionally versatile and easy to use. Features include an input range from V_{EE} − 0.5 V to V_{CCI} + 0.2 V, low noise, LVDS-compatible output drivers, and TTL/CMOS latch inputs with adjustable hysteresis and/or shutdown inputs.

The devices offer 1.5 ns propagation delays with 1 ps rms random jitter (RJ). Overdrive and slew rate dispersion are typically less than 50 ps.

A flexible power supply scheme allows the devices to operate with a single 2.5 V positive supply and a −0.5 V to +2.7 V input signal range up to a 5.5 V positive supply with a −0.5 V to +5.7 V input signal range. Split input/output supplies, with no sequencing restrictions on the ADCMP605, support a wide input signal range with greatly reduced power consumption.

The LVDS-compatible output stage is designed to drive any standard LVDS input. The comparator input stage offers robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded. High speed latch and programmable hysteresis features are also provided in a unique single-pin control option.

The ADCMP604 is available in a 6-lead SC70 package, and the ADCMP605 is available in a 12-lead LFCSP.

Rev. A

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10/06—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CCI} = V_{CCO} = 2.5 V, T_A = −40°C to +125°C, typical at T_A = 25 °C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Voltage Range	V_P, V_N	V_{CCI} = 2.5 V to 5.5 V	−0.5		V_{CCI} + 0.2	V
Common-Mode Range		V_{CCI} = 2.5 V to 5.5 V	−0.2		V_{CCI} + 0.2	V
Differential Voltage		V_{CCI} = 2.5 V to 5.5 V			V_{CCI}	V
Offset Voltage	V_{OS}		−5.0		+5.0	mV
Bias Current	I_P, I_N		−5.0	±2	+5.0	µA
Offset Current			−2.0		+2.0	µA
Capacitance	C_P, C_N			1		pF
Resistance, Differential Mode		−0.1 V to V_{CCI}	200	750	7500	kΩ
Resistance, Common Mode		−0.5 V to V_{CCI} + 0.5 V	100	370	4000	kΩ
Active Gain	A_V			62		dB
Common-Mode Rejection Ratio	CMRR	V_{CCI} = 2.5 V, V_{CCO} = 2.5 V, V_{CM} = −0.2 V to +2.7 V	50			dB
		V_{CCI} = 2.5 V, V_{CCO} = 5.0 V	50			dB
Hysteresis		R_{HYS} = ∞		<0.1		mV
LATCH ENABLE PIN CHARACTERISTICS (ADCMP605 ONLY)						
V_{IH}		Hysteresis is shut off	2.0		V_{CCO}	V
V_{IL}		Latch mode guaranteed	−0.2	+0.4	+0.8	V
I_{IH}		V_{IH} = V_{CCO} + 0.2 V	−6		+6	µA
I_{IL}		V_{IL} = 0.4 V	−0.1		+0.1	mA
HYSTERESIS MODE AND TIMING (ADCMP605 ONLY)						
Hysteresis Mode Bias Voltage		Current sink −1 µA	1.145	1.25	1.40	V
Minimum Resistor Value		Hysteresis = 120 mV	30		110	kΩ
Hysteresis Current		Hysteresis = 120 mV	−25		−8	µA
Latch Setup Time	t_S	V_{OD} = 50 mV		−2		ns
Latch Hold Time	t_H	V_{OD} = 50 mV		2.7		ns
Latch-to-Output Delay	t_{PLOH}, t_{PLOL}	V_{OD} = 50 mV		20		ns
Latch Minimum Pulse Width	t_{PL}	V_{OD} = 50 mV		24		ns
SHUTDOWN PIN CHARACTERISTICS (ADCMP605 ONLY)						
V_{IH}		Comparator is operating	2.0		V_{CCO}	V
V_{IL}		Shutdown guaranteed	−0.2	+0.4	+0.6	V
I_{IH}		V_{IH} = V_{CCO}	−6		+6	µA
I_{IL}		V_{IL} = 0 V			−0.1	mA
Sleep Time	t_{SD}	10% output swing		1.4		ns
Wake-Up Time	t_H	V_{OD} = 50 mV, output valid		25		ns
DC OUTPUT CHARACTERISTICS		V_{CCI} = V_{CCO} = 2.5 V to 5.0 V (ADCMP604) V_{CCO} = 2.5 V to 5.0 V (ADCMP605)				
Differential Output Voltage Level	V_{OD}	R_{LOAD} = 100 Ω	245	350	445	mV
ΔV_{OD}		R_{LOAD} = 100 Ω			50	mV
Common-Mode Voltage	V_{OCI}	R_{LOAD} = 100 Ω	1.125		1.375	V
Peak-to-Peak Common-Mode Output	$V_{OC\ (p-p)}$	R_{LOAD} = 100 Ω			50	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AC PERFORMANCE[1]						
Rise Time/Fall Time	t_R, t_F	10% to 90%		600		ps
Propagation Delay	t_{PD}	$V_{CCI} = V_{CCO}$ = 2.5 V to 5.0 V, V_{OD} = 50 mV		1.6		ns
		$V_{CCI} = V_{CCO}$ = 2.5 V, V_{OD} = 10 mV		3.0		ns
Propagation Delay Skew—Rising to Falling Transition	$t_{PINSKEW}$	$V_{CCI} = V_{CCO}$ = 2.5 V to 5.0 V		70		ps
Propagation Delay Skew—Q to QB		$V_{CCI} = V_{CCO}$ = 2.5 V to 5.0 V		70		ps
Overdrive Dispersion		10 mV < V_{OD} < 125 mV		1.6		ns
Common-Mode Dispersion		V_{CM} = −0.2 V to V_{CCI} + 0.2 V		250		ps
Input Bandwidth				500		MHz
Minimum Pulse Width	PW_{MIN}	$V_{CCI} = V_{CCO}$ = 2.5 V to 5.0 V, PW_{OUT} = 90% of PW_{IN}		1.3		ns
POWER SUPPLY						
Input Supply Voltage Range	V_{CCI}		2.5		5.5	V
Output Supply Voltage Range	V_{CCO}		2.5		5.0	V
Positive Supply Differential (ADCMP605)	$V_{CCI} - V_{CCO}$	Operating	−3		+3	V
	$V_{CCI} - V_{CCO}$	Nonoperating	−5.0		+5.0	V
Positive Supply Current (ADCMP604)	$I_{VCCI/VCCO}$	$V_{CCI} = V_{CCO}$ = 2.5 V to 5.0 V		15	21	mA
Input Section Supply Current (ADCMP605)	I_{VCCI}	V_{CCI} = 2.5 V to 5.5 V		1.6	3.0	mA
Output Section Supply Current (ADCMP605)	I_{VCCO}	V_{CCO} = 2.5 V to 5.0 V		15	23	mA
Power Dissipation	P_D	$V_{CCI} = V_{CCO}$ = 2.5 V		37	55	mW
		$V_{CCI} = V_{CCO}$ = 5.0 V		95	120	mW
Power Supply Rejection Ratio	PSRR	$V_{CCI} = V_{CCO}$ = 2.5 V to 5.0 V	−50			dB
Shutdown Mode I_{CCI}		$V_{CCI} = V_{CCO}$ = 2.5 V to 5.0 V		0.92	1.1	mA
Shutdown Mode I_{CCO}		$V_{CCI} = V_{CCO}$ = 2.5 V to 5.0 V	−30		+30	µA

[1] V_{IN} = 100 mV square input at 50 MHz, V_{OD} = 50 mV, V_{CM} = 1.25 V, $V_{CCI} = V_{CCO}$ = 2.5 V, unless otherwise noted.

TIMING INFORMATION

Figure 2 illustrates the ADCMP604/ADCMP605 latch timing relationships. Table 2 provides definitions of the terms shown in Figure 2.

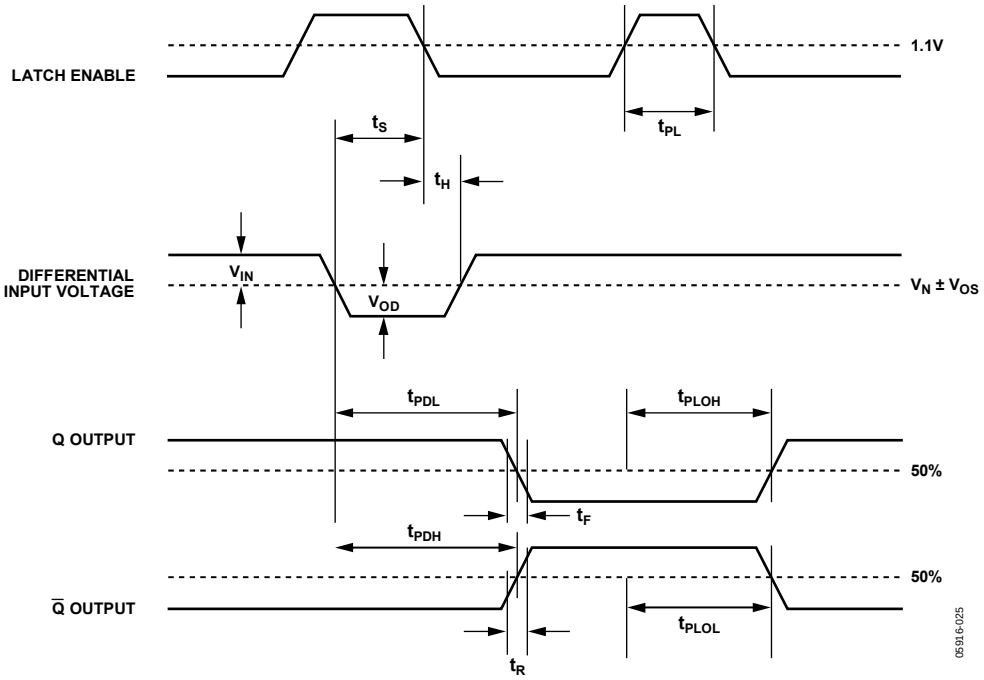

Figure 2. System Timing Diagram

Table 2. Timing Descriptions

Symbol	Timing	Description
t_{PDH}	Input-to-Output High Delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition.
t_{PDL}	Input-to-Output Low Delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition.
t_{PLOH}	Latch Enable-to-Output High Delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition.
t_{PLOL}	Latch Enable-to-Output Low Delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition.
t_H	Minimum Hold Time	Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
t_{PL}	Minimum Latch Enable Pulse Width	Minimum time that the latch enable signal must be high to acquire an input signal change.
t_S	Minimum Setup Time	Minimum time before the negative transition of the latch enable signal occurs that an input signal change must be present to be acquired and held at the outputs.
t_R	Output Rise Time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
t_F	Output Fall Time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
V_{OD}	Voltage Overdrive	Difference between the input voltages, V_A and V_B.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltages	
Input Supply Voltage (V_{CCI} to GND)	−0.5 V to +6.0 V
Output Supply Voltage (V_{CCO} to GND)	−0.5 V to +6.0 V
Positive Supply Differential ($V_{CCI} – V_{CCO}$)	−6.0 V to +6.0 V
Input Voltages	
Input Voltage	−0.5 V to V_{CCI} + 0.5 V
Differential Input Voltage	±(V_{CCI} + 0.5 V)
Maximum Input/Output Current	±50 mA
Shutdown Control Pin	
Applied Voltage (S_{DN} to GND)	−0.5 V to V_{CCO} + 0.5 V
Maximum Input/Output Current	±50 mA
Latch/Hysteresis Control Pin	
Applied Voltage (HYS to GND)	−0.5 V to V_{CCO} + 0.5 V
Maximum Input/Output Current	±50 mA
Output Current	±50 mA
Temperature	
Operating Temperature Range, Ambient	−40°C to +125°C
Operating Temperature, Junction	150°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	Unit
6-Lead SC70 (KS-6)	426	°C/W
12-Lead LFCSP_VQ (CP-12-1)	62	°C/W

[1] Measurement in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

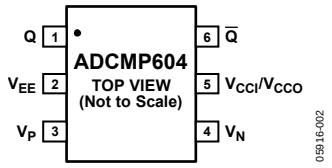

Figure 3. ADCMP604 Pin Configuration

Table 5. ADCMP604 Pin Function Descriptions (6-Lead SC70)

Pin No.	Mnemonic	Description
1	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N.
2	V_{EE}	Negative Supply Voltage.
3	V_P	Noninverting Analog Input.
4	V_N	Inverting Analog Input.
5	V_{CCI}/V_{CCO}	Input Section Supply/Output Section Supply. V_{CCI} and V_{CCO} are shared pin.
6	$\overline{Q}$	Inverting Output. $\overline{Q}$ is at logic low if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N.

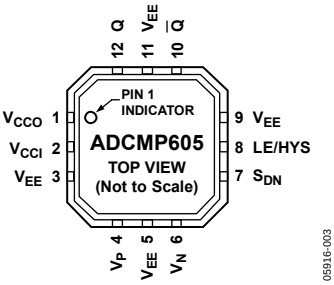

Figure 4. ADCMP605 Pin Configuration

Table 6. ADCMP605 Pin Function Descriptions (12-Lead LFCSP_VQ)

Pin No.	Mnemonic	Description
1	V_{CCO}	Output Section Supply.
2	V_{CCI}	Input Section Supply.
3, 5, 9, 11	V_{EE}	Negative Supply Voltages.
4	V_P	Noninverting Analog Input.
6	V_N	Inverting Analog Input.
7	S_{DN}	Shutdown. Drive this pin low to shut down the device.
8	LE/HYS	Latch/Hysteresis Control. Bias with resistor or current for hysteresis; drive low to latch.
10	$\overline{Q}$	Inverting Output. $\overline{Q}$ is at Logic low if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, if the comparator is in compare mode.
12	Q	Noninverting Output. Q is at Logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, if the comparator is in compare mode.
Heat Sink Paddle	V_{EE}	The metallic back surface of the package is electrically connected to V_{EE}. It can be left floating because Pin 3, Pin 5, Pin 9, and Pin 11 provide adequate electrical connection. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CCI} = V_{CCO} = 2.5$ V, $T_A = 25°C$, unless otherwise noted.

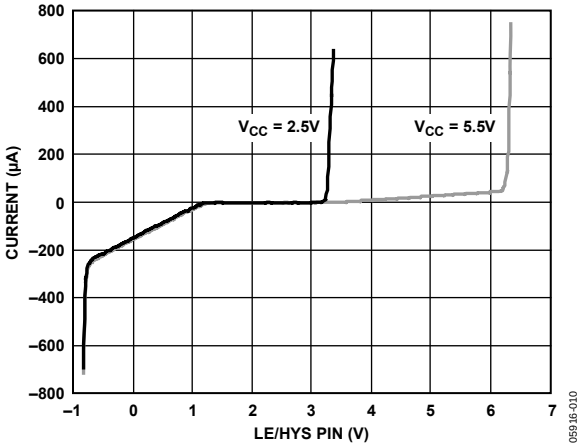

Figure 5. LE/HYS Pin Current vs. Voltage

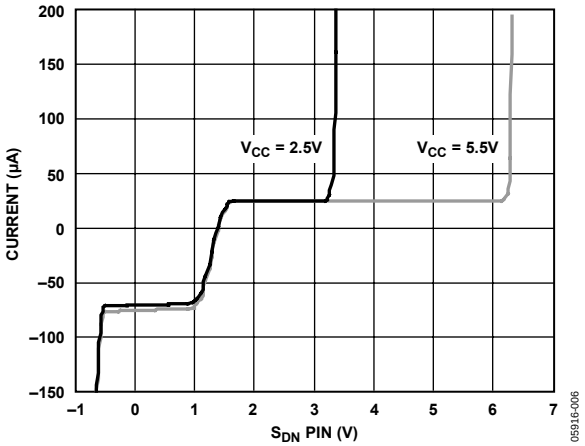

Figure 6. S_{DN} Pin Current vs. Voltage

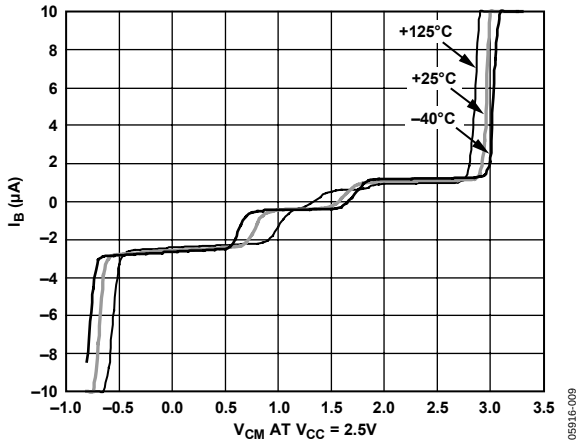

Figure 7. Input Bias Current vs. Input Common-Mode Voltage

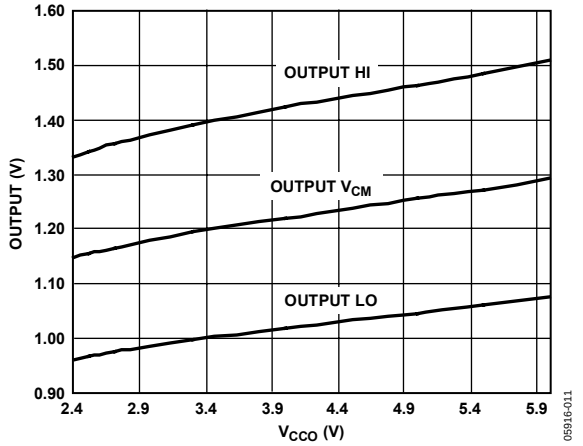

Figure 8. LVDS Output Level vs. V_{CCO} (V)

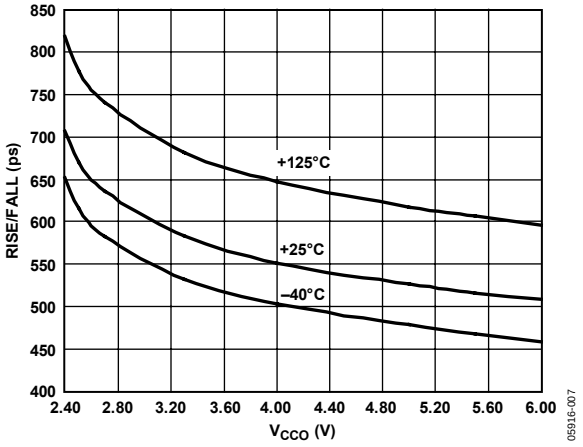

Figure 9. LVDS Output Rise/Fall Time vs. V_{CCO} (V)

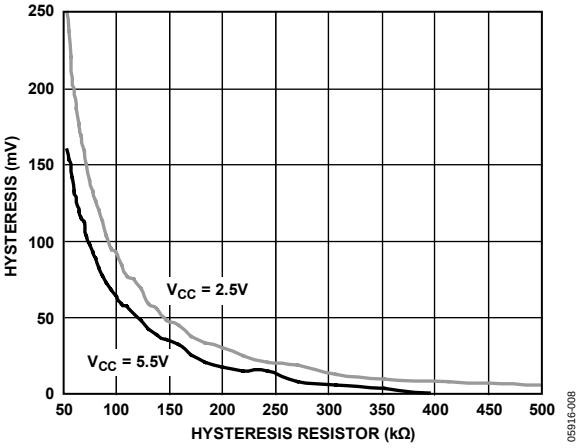

Figure 10. Hysteresis vs. Hysteresis Resistor

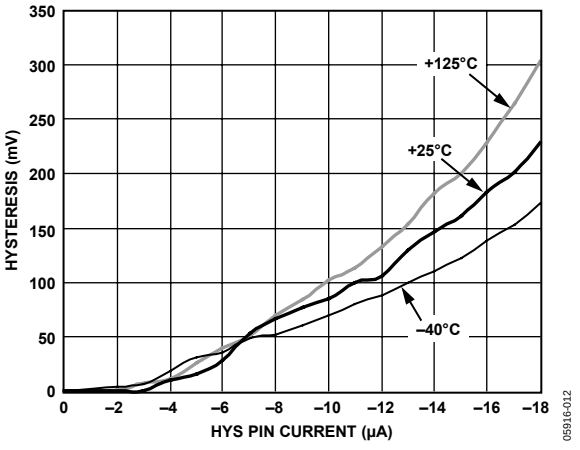

Figure 11. Hysteresis vs. HYS Pin Current

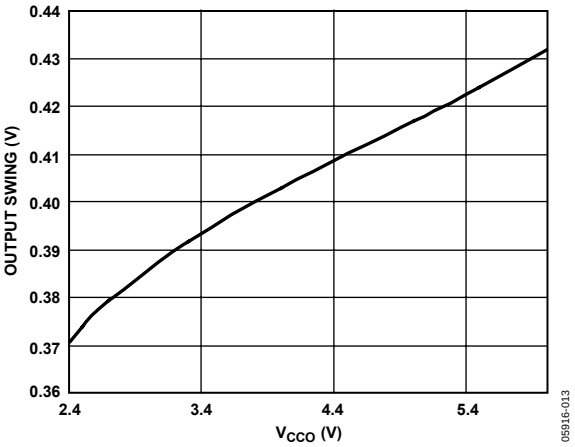

Figure 14. LVDS Output Swing vs. V_{CCO} (V)

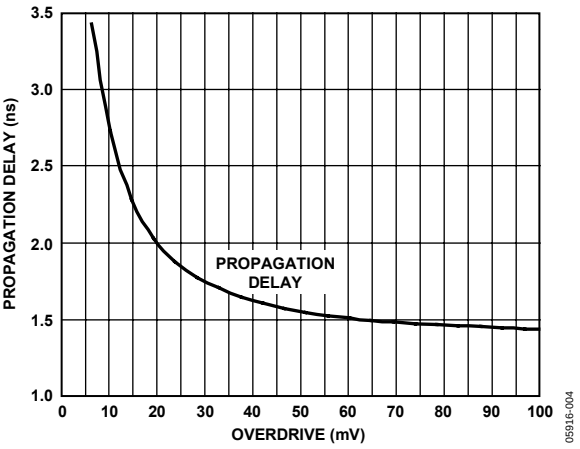

Figure 12. Propagation Delay vs. Input Overdrive

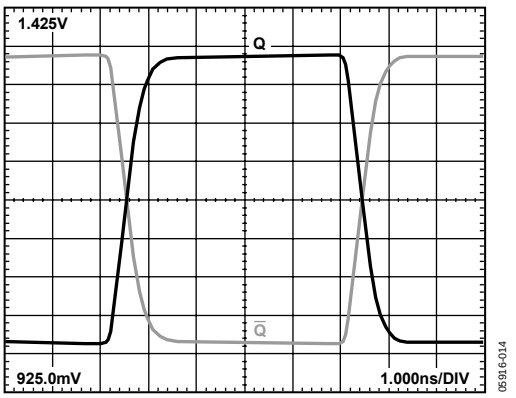

Figure 15. 50 MHz Output Voltage Waveform at V_{CCO} = 2.5 V

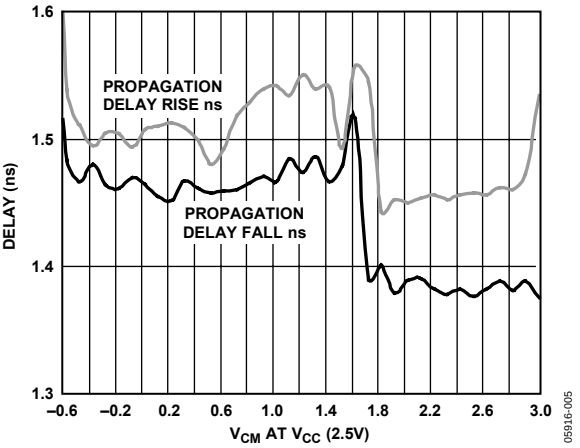

Figure 13. Propagation Delay vs. Input Common-Mode Voltage

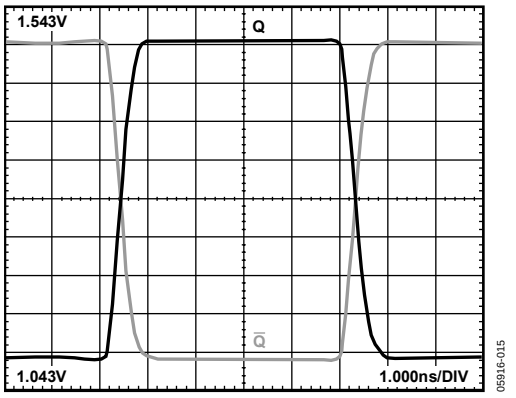

Figure 16. 50 MHz Output Voltage Waveform at V_{CCO} = 5.5 V

APPLICATION INFORMATION

POWER/GROUND LAYOUT AND BYPASSING

The ADCMP604/ADCMP605 comparators are very high speed devices. Despite the low noise output stage, it is essential to use proper high speed design techniques to achieve the specified performance. Because comparators are uncompensated amplifiers, feedback in any phase relationship is likely to cause oscillations or undesired hysteresis. The use of low impedance supply planes is of critical importance particularly the output supply plane (V_{CCO}) and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. Multiple high quality 0.01 µF bypass capacitors should be placed as close as possible to each of the V_{CCI} and V_{CCO} supply pins and should be connected to the GND plane with redundant vias. At least one of these should be placed to provide a physically short return path for output currents flowing back from ground to the V_{CCI} pin and the V_{CCO} pin. High frequency bypass capacitors should be carefully selected for minimum inductance and ESR. Parasitic layout inductance should also be strictly controlled to maximize the effectiveness of the bypass at high frequencies.

If the package allows, and the input and output supplies have been connected separately ($V_{CCI} \neq V_{CCO}$), be sure to bypass each of these supplies separately to the GND plane. Do not connect a bypass capacitor between these supplies. It is recommended that the GND plane separate the V_{CCI} and V_{CCO} planes when the circuit board layout is designed to minimize coupling between the two supplies to take advantage of the additional bypass capacitance from each respective supply to the ground plane. This enhances the performance when split input/output supplies are used. If the input and output supplies are connected together for single-supply operation ($V_{CCI} = V_{CCO}$), coupling between the two supplies is unavoidable; however, careful board placement can help keep output return currents away from the inputs.

LVDS-COMPATIBLE OUTPUT STAGE

Specified propagation delay dispersion performance is only achieved by keeping parasitic capacitive loads at or below the specified minimums. The outputs of the ADCMP604 and ADCMP605 are designed to directly drive any standard LVDS-compatible input.

USING/DISABLING THE LATCH FEATURE

The latch input is designed for maximum versatility. It can safely be left floating or it can be driven low by any standard TTL/CMOS device as a high speed latch. In addition, the pin can be operated as a hysteresis control pin with a bias voltage of 1.25 V nominal and an input resistance of approximately 70 kΩ. This allows the comparator hysteresis to be easily controlled by either a resistor or an inexpensive CMOS DAC. Driving this pin high or floating the pin disables all hysteresis.

Hysteresis control and latch mode can be used together if an open drain, an open collector, or a three-state driver is connected in parallel to the hysteresis control resistor or current source.

Due to the programmable hysteresis feature, the logic threshold of the latch pin is approximately 1.1 V, regardless of V_{CCO}.

OPTIMIZING PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential for obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and often cause oscillation. Large discontinuities along input and output transmission lines can also limit the specified pulse-width dispersion performance. The source impedance should be minimized as much as is practicable. High source impedance, in combination with the parasitic input capacitance of the comparator, causes an undesirable degradation in bandwidth at the input, thus degrading the overall response. Thermal noise from large resistances can easily cause extra jitter with slowly slewing input signals. Higher impedances encourage undesired coupling.

COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP604/ADCMP605 comparators are designed to reduce propagation delay dispersion over a wide input overdrive range of 5 mV to V_{CCI} − 1 V. Propagation delay dispersion is the variation in propagation delay that results from a change in the degree of overdrive or slew rate (how far or how fast the input signal is driven past the switching threshold).

Propagation delay dispersion is a specification that becomes important in high speed, time-critical applications, such as data communications, automatic test and measurement, and instrumentation. It is also important in event-driven applications, such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed (see Figure 17 and Figure 18).

The ADCMP604/ADCMP605 dispersion is typically <1.6 ns as the overdrive varies from 10 mV to 125 mV. This specification applies to both positive and negative signals because each of the ADCMP604 and ADCMP605 has substantially equal delays for positive-going and negative-going inputs and very low output skews.

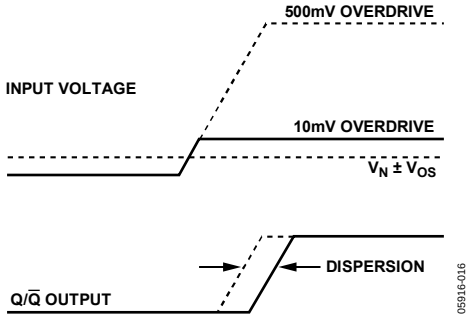

Figure 17. Propagation Delay—Overdrive Dispersion

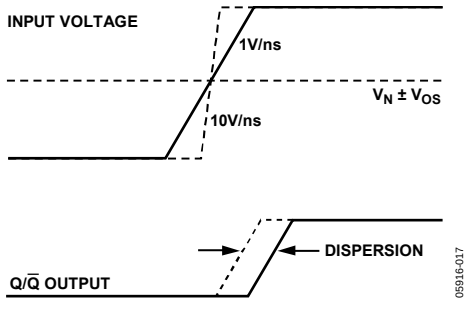

Figure 18. Propagation Delay—Slew Rate Dispersion

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often desirable in a noisy environment, or when the differential input amplitudes are relatively small or slow moving. The transfer function for a comparator with hysteresis is shown in Figure 19. As the input voltage approaches the threshold (0 V, in this example) from below the threshold region in a positive direction, the comparator switches from low to high when the input crosses $+V_H/2$. The new switching threshold becomes $-V_H/2$. The comparator remains in the high state until the threshold, $-V_H/2$, is crossed from below the threshold region in a negative direction. In this manner, noise or feedback output signals centered on 0 V input cannot cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

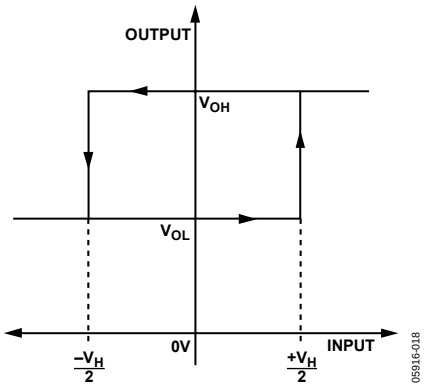

Figure 19. Comparator Hysteresis Transfer Function

The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. One limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that is not symmetric about the threshold. The external feedback network can also introduce significant parasitics that reduce high speed performance and induce oscillation in some cases.

The ADCMP605 comparator offers a programmable hysteresis feature that significantly improves accuracy and stability. Connecting an external pull-down resistor or a current source from the LE/HYS pin to GND varies the amount of hysteresis in a predictable and stable manner. Leaving the LE/HYS pin disconnected or driving it high removes hysteresis. The maximum hysteresis that can be applied using this pin is approximately 160 mV. Figure 20 illustrates the amount of hysteresis applied as a function of external resistor value. Figure 11 illustrates hysteresis as a function of current.

The hysteresis control pin appears as a 1.25 V bias voltage seen through a series resistance of 70 kΩ ± 20% throughout the hysteresis control range. The advantages of applying hysteresis in this manner are improved accuracy, improved stability, reduced component count, and maximum versatility. An external bypass capacitor is not recommended on the HYS pin because it would likely degrade the jitter performance of the device and impair the latch function. As described in the Using/Disabling the Latch Feature section, hysteresis control need not compromise the latch function.

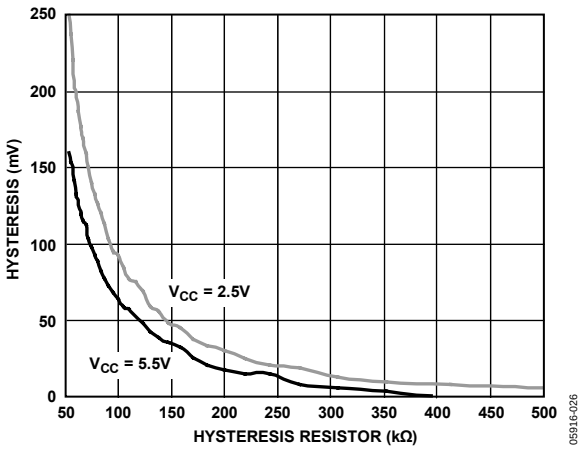

Figure 20. Hysteresis vs. R_{HYS} Control Resistor

CROSSOVER BIAS POINTS

Rail-to-rail inputs of this type, in both op amps and comparators, have a dual front-end design. Certain devices are active near the V_{CCI} rail and others are active near the V_{EE} rail. At some predetermined point in the common-mode range, a crossover occurs. At this point, normally $V_{CCI}/2$, the direction of the bias current reverses and there are changes in measured offset voltages and currents.

MINIMUM INPUT SLEW RATE REQUIREMENT

With the rated load capacitance and normal good PCB design practice, as discussed in the Optimizing Performance section, these comparators should be stable at any input slew rate with no hysteresis. Broadband noise from the input stage is observed in place of the violent chattering seen with most other high speed comparators. With additional capacitive loading or poor bypassing, oscillation is observed. This oscillation is due to the high gain bandwidth of the comparator in combination with feedback parasitics in the package and PCB. In many applications, chattering is not harmful.

TYPICAL APPLICATION CIRCUITS

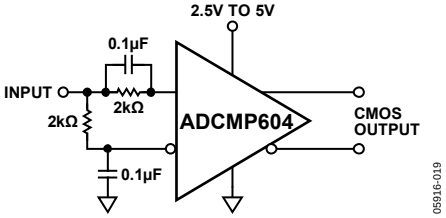

Figure 21. Self-Biased, 50% Slicer

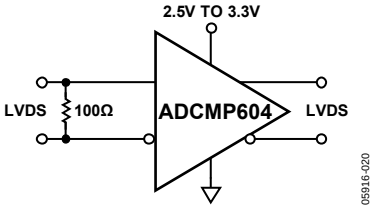

Figure 22. LVDS to Repeater

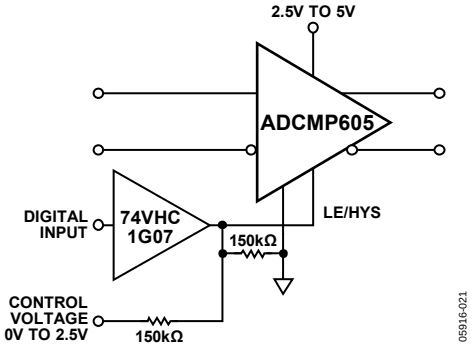

Figure 23. Hysteresis Adjustment with Latch

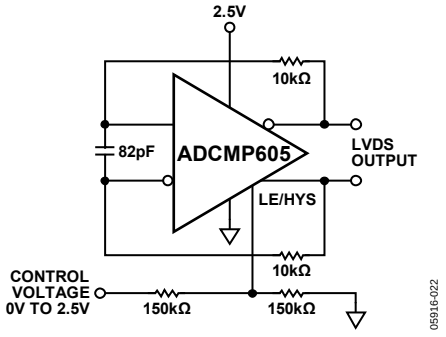

Figure 24. Voltage-Controlled Oscillator

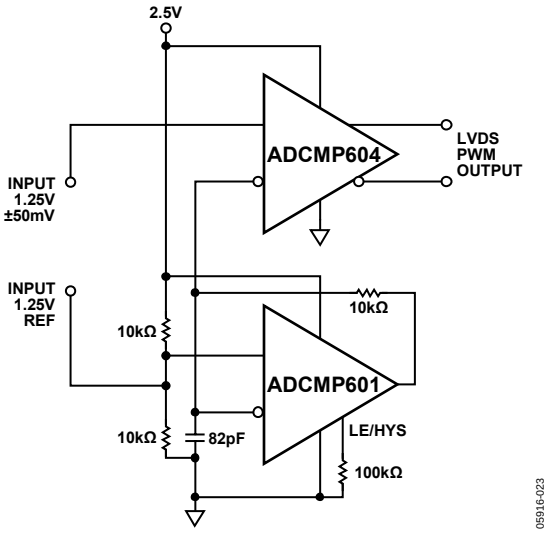

Figure 25. Oscillator and Pulse-Width Modulator

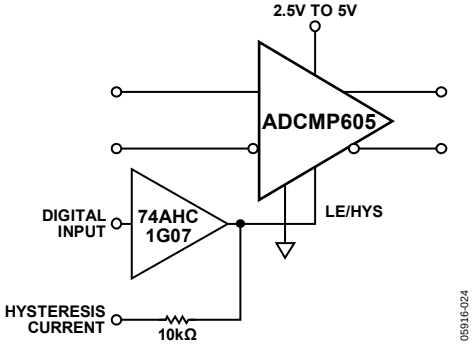

Figure 26. Hysteresis Adjustment with Latch

OUTLINE DIMENSIONS

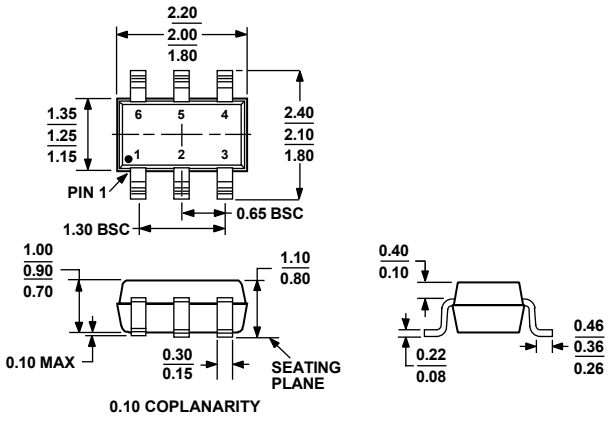

Figure 27. 6-Lead Thin Shrink Small Outline Transistor Package (SC70)
(KS-6)
Dimensions shown in millimeters

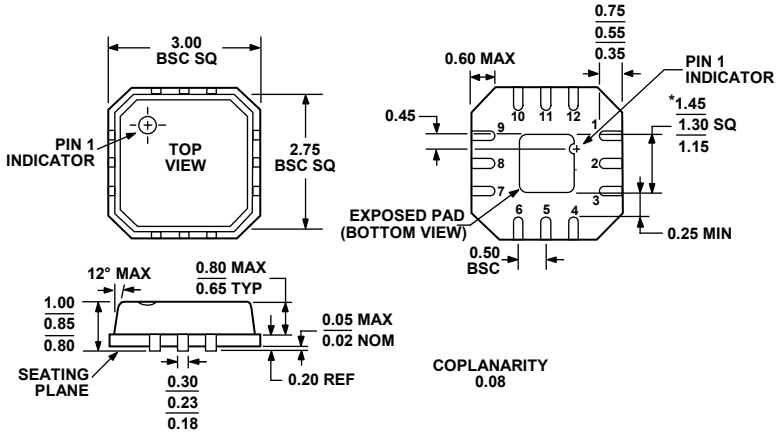

Figure 28. 12-Lead Lead Frame Chip Scale Package (LFCSP_VQ)
3 mm × 3 mm Body, Very Thin Quad
(CP-12-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADCMP604BKSZ-R2[1]	−40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	G0Q
ADCMP604BKSZ-REEL7[1]	−40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	G0Q
ADCMP604BKSZ-RL[1]	−40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	G0Q
ADCMP605BCPZ-WP[1]	−40°C to +125°C	12-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-12-1	G0K
ADCMP605BCPZ-R2[1]	−40°C to +125°C	12-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-12-1	G0K
ADCMP605BCPZ-R7[1]	−40°C to +125°C	12-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-12-1	G0K
EVAL-ADCMP605BCPZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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