DG408BP45

Gate Turn-off Thyristor

Replaces March 1998 version, DS4091-2.3

DS4091-3.0 January 2000

APPLICATIONS

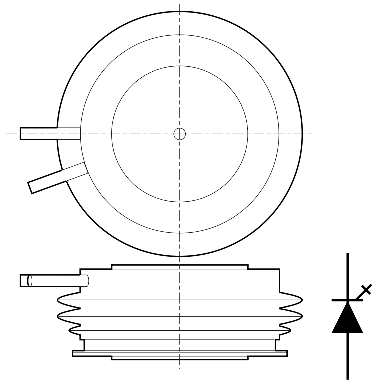
- Variable speed A.C. motor drive inverters (VSD-AC)
- Uninterruptable Power Supplies
- High Voltage Converters
- Choppers
- Welding
- Induction Heating
- DC/DC Converters.

KEY PARAMETERS

I_{TCM}	1000A
V_{DRM}	4500V
$I_{T(AV)}$	320A
dV_D/dt	1000V/µs
di_T/dt	300A/µs

FEATURES

- Double Side Cooling
- High Reliability In Service
- High Voltage Capability
- Fault Protection Without Fuses
- High Surge Current Capability
- Turn-off Capability Allows Reduction In Equipment Size And Weight. Low Noise Emission Reduces Acoustic Cladding Necessary For Environmental Requirements



Outline type code: P.
See Package Details for further information.

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} V	Repetitive Peak Reverse Voltage V_{RRM} V	Conditions
DG408BP45	4500	16	T_{vj} = 125°C, I_{DM} = 50mA, I_{RRM} = 50mA

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TCM}	Repetitive peak controllable on-state current	$V_D = V_{DRM}$, T_j = 125°C, di_{GQ}/dt = 30A/µs, Cs = 1.0µF	1000	A
$I_{T(AV)}$	Mean on-state current	T_{HS} = 80°C. Double side cooled. Half sine 50Hz.	320	A
$I_{T(RMS)}$	RMS on-state current	T_{HS} = 80°C. Double side cooled. Half sine 50Hz.	500	A

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine. T_j = 125ºC	7.0	kA
I^2t	I^2t for fusing	10ms half sine. T_j =125ºC	0.245×10^6	A^2s
di_T/dt	Critical rate of rise of on-state current	V_D = 3000V, I_T = 1000A, T_j = 125ºC, I_{FG} > 30A, Rise time > 1.5µs	300	A/µs
dV_D/dt	Rate of rise of off-state voltage	To 66% V_{DRM}; $R_{GK} \le 1.5\Omega$, T_j = 125ºC	225	V/µs
		To 66% V_{DRM}; V_{RG} = -2V, T_j = 125ºC	1000	V/µs
L_S	Peak stray inductance in snubber circuit	-	200	nH

GATE RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{RGM}	Peak reverse gate voltage	This value maybe exceeded during turn-off	-	16	V
I_{FGM}	Peak forward gate current		20	70	A
$P_{FG(AV)}$	Average forward gate power		-	10	W
P_{RGM}	Peak reverse gate power		-	15	kW
di_{GQ}/dt	Rate of rise of reverse gate current		15	60	A/µs
$t_{ON(min)}$	Minimum permissable on time		20	-	µs
$t_{OFF(min)}$	Minimum permissable off time		100	-	µs

THERMAL RATINGS AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-hs)}$	DC thermal resistance - junction to heatsink surface	Double side cooled		-	0.041	ºC/W
		Anode side cooled		-	0.07	ºC/W
		Cathode side cooled		-	0.1	ºC/W
$R_{th(c-hs)}$	Contact thermal resistance	Clamping force 12.0kN With mounting compound	per contact	-	0.009	ºC/W
T_{vj}	Virtual junction temperature			-	125	ºC
T_{OP}/T_{stg}	Operating junction/storage temperature range			-40	125	ºC
-	Clamping force			11.0	15.0	kN

CHARACTERISTICS

T_j = 125°C unless stated otherwise					
Symbol	**Parameter**	**Conditions**	**Min.**	**Max.**	**Units**
V_{TM}	On-state voltage	At 1000A peak, $I_{G(ON)}$ = 4A d.c.	-	3.5	V
I_{DM}	Peak off-state current	V_{DRM} = 4500V, V_{RG} = 0V	-	50	mA
I_{RRM}	Peak reverse current	At V_{RRM}	-	50	mA
V_{GT}	Gate trigger voltage	V_D = 24V, I_T = 100A, T_j = 25°C	-	1.0	V
I_{GT}	Gate trigger current	V_D = 24V, I_T = 100A, T_j = 25°C	-	1.5	A
I_{RGM}	Reverse gate cathode current	V_{RGM} = 16V, No gate/cathode resistor	-	50	mA
E_{ON}	Turn-on energy	V_D = 3000V I_T = 1000A, dI_T/dt = 300A/µs I_{FG} = 30A, rise time < 1.5µs	-	2300	mJ
t_d	Delay time		-	1.5	µs
t_r	Rise time		-	5.0	µs
E_{OFF}	Turn-off energy	I_T = 1000A, V_{DM} = V_{DRM} Snubber Cap Cs = 1.0µF, di_{GQ}/dt = 30A/µs	-	4120	mJ
t_{gs}	Storage time		-	14.0	µs
t_{gf}	Fall time		-	1.5	µs
t_{gq}	Gate controlled turn-off time		-	15.5	µs
Q_{GQ}	Turn-off gate charge		-	3000	µC
Q_{GQT}	Total turn-off gate charge		-	6000	µC
I_{GQM}	Peak reverse gate current		-	420	A

CURVES

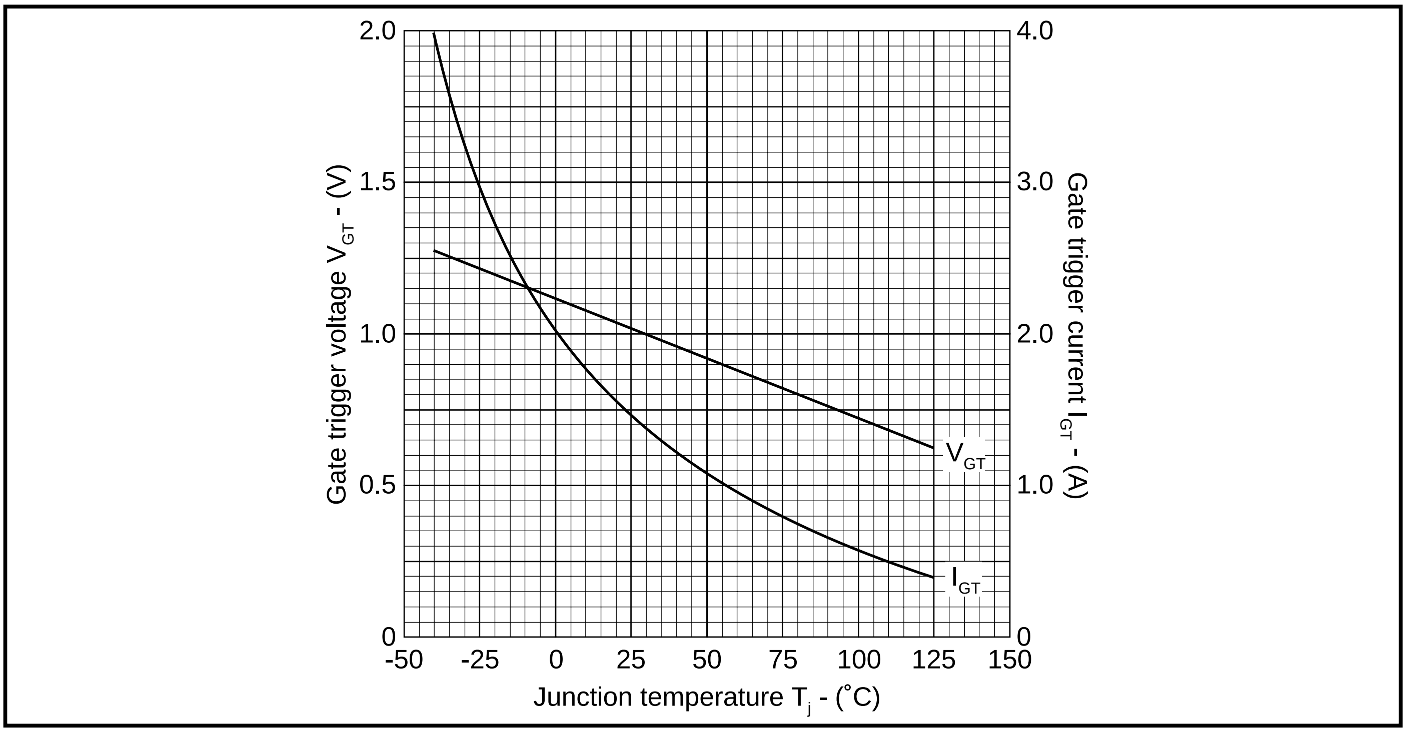


Fig.1 Maximum gate trigger voltage/current vs junction temperature

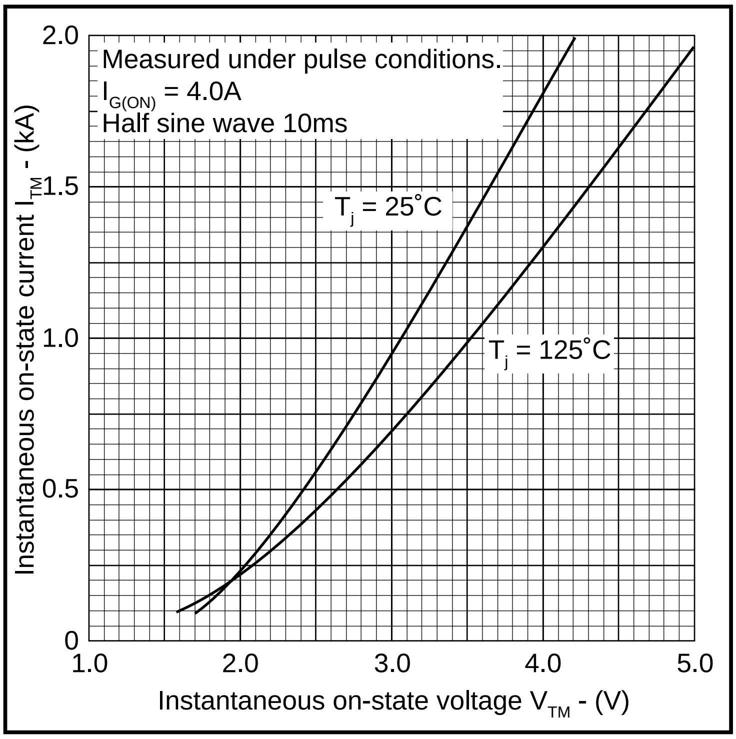


Fig.2 On-state characteristics

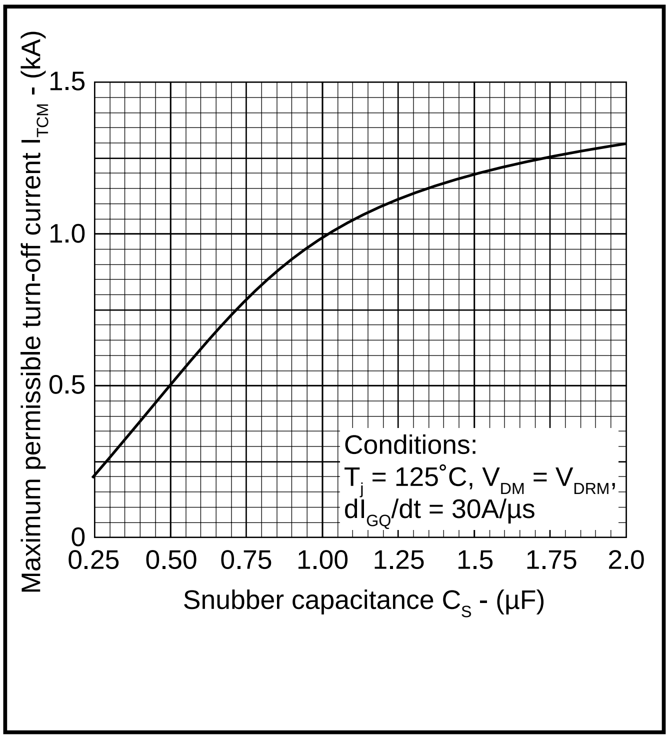


Fig.3 Maximum dependence of I_{TCM} on C_S

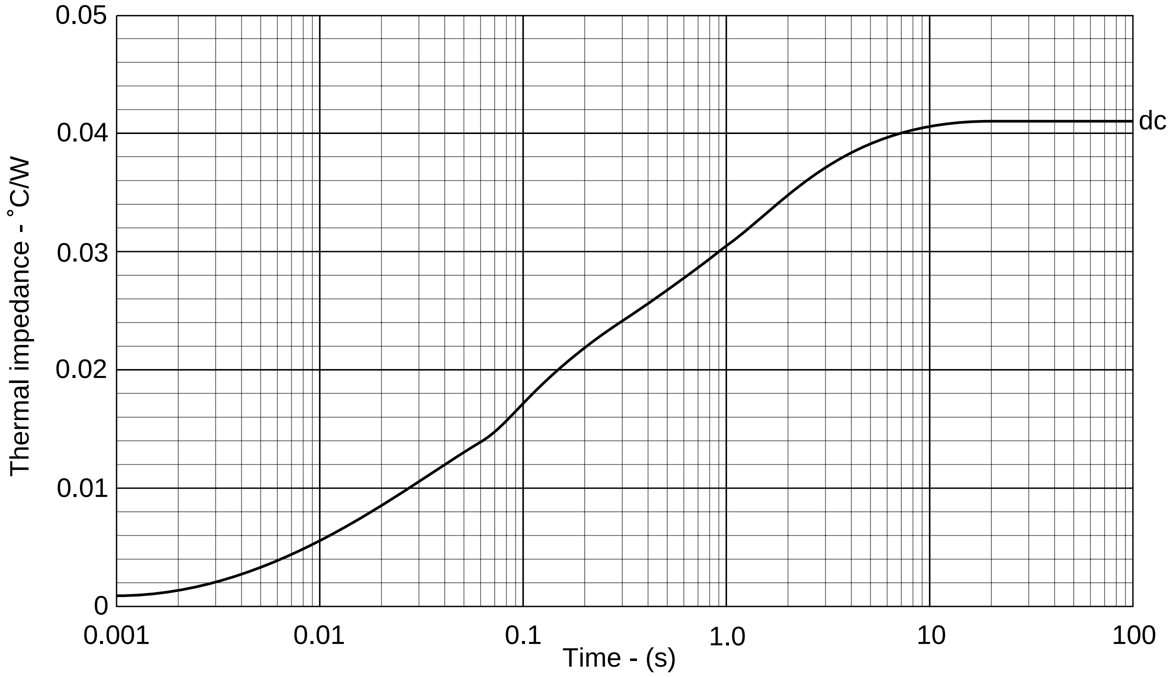


Fig.4 Maximum (limit) transient thermal impedance - double side cooled

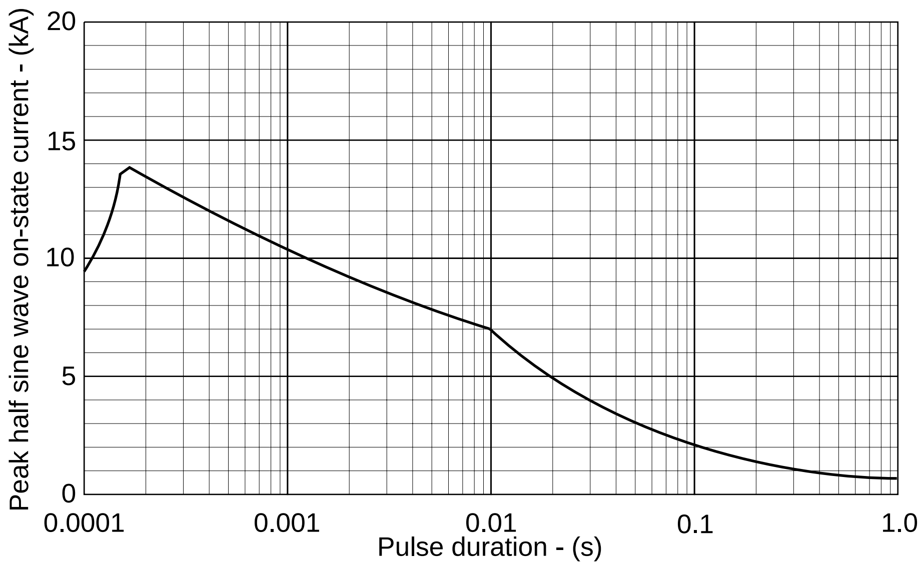


Fig.5 Surge (non-repetitive) on-state current vs time

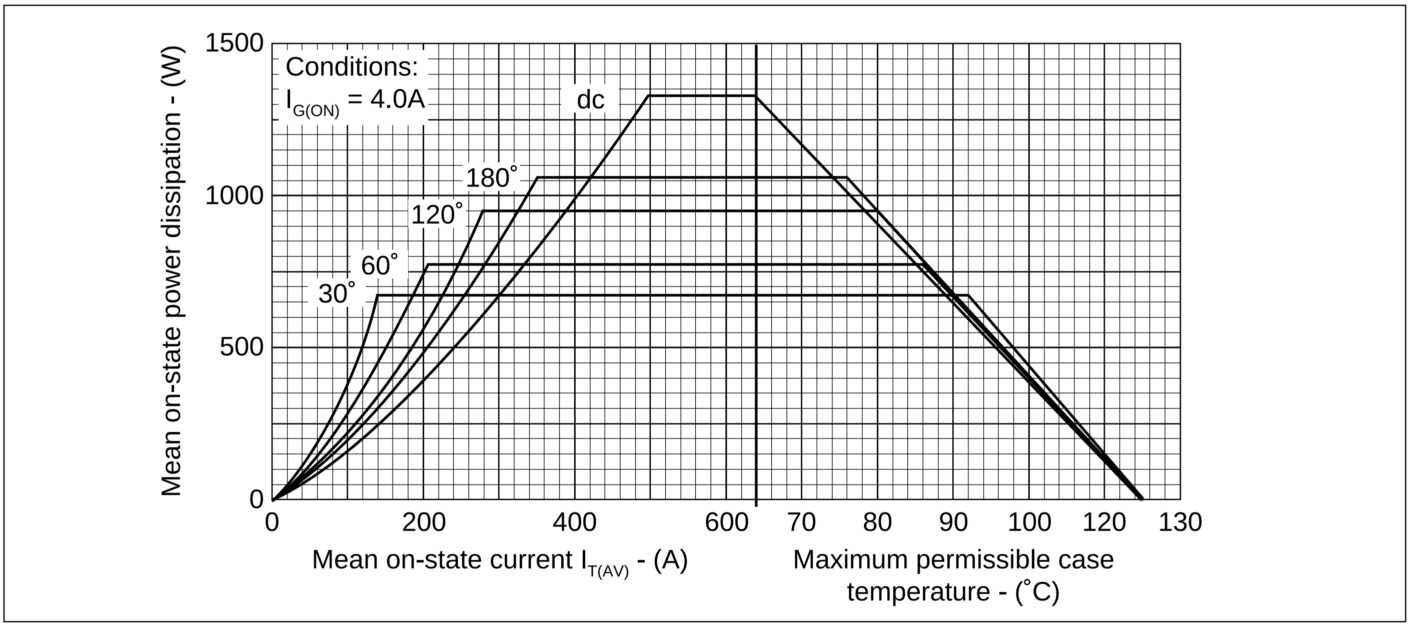


Fig.6 Steady state rectangluar wave conduction loss - double side cooled

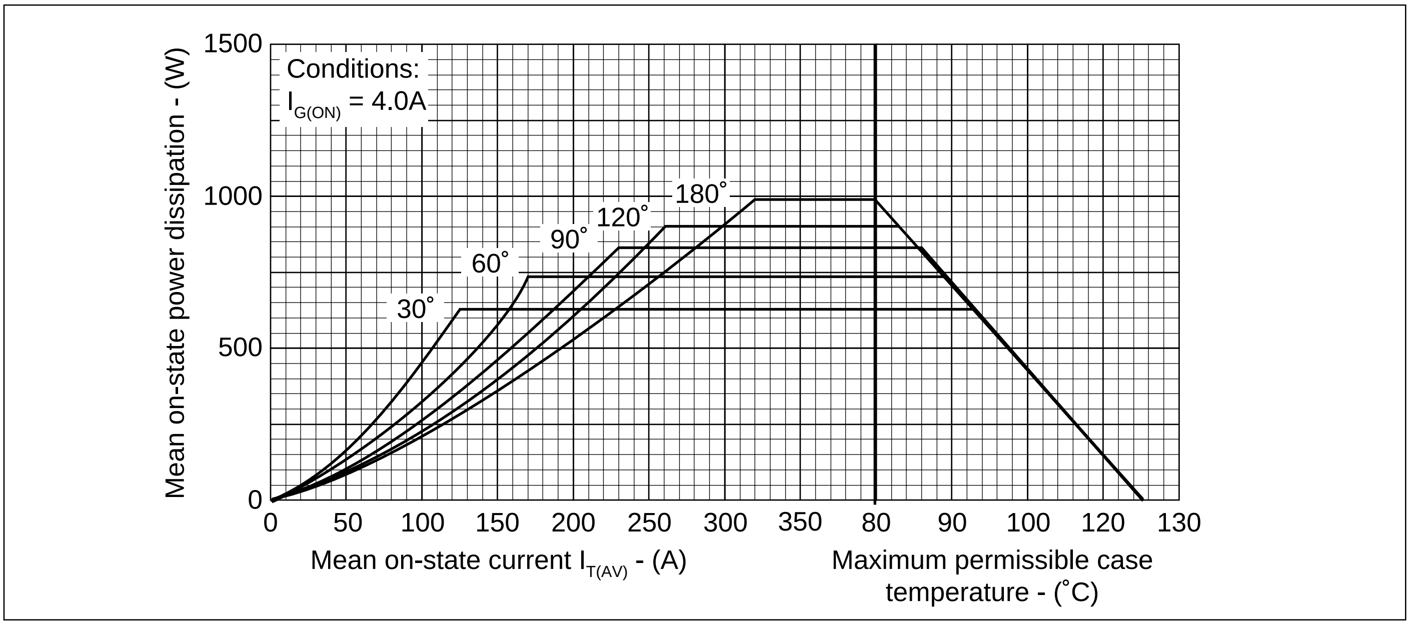


Fig.7 Steady state sinusoidal wave conduction loss - double side cooled

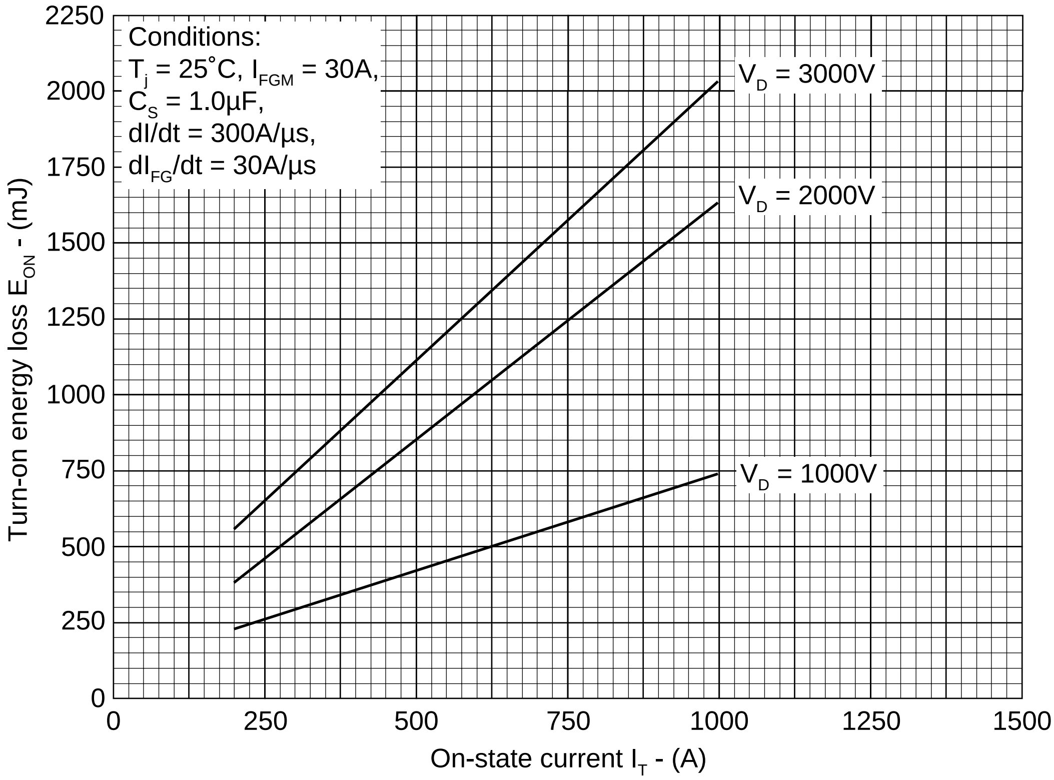


Fig.8 Turn-on energy vs on-state current

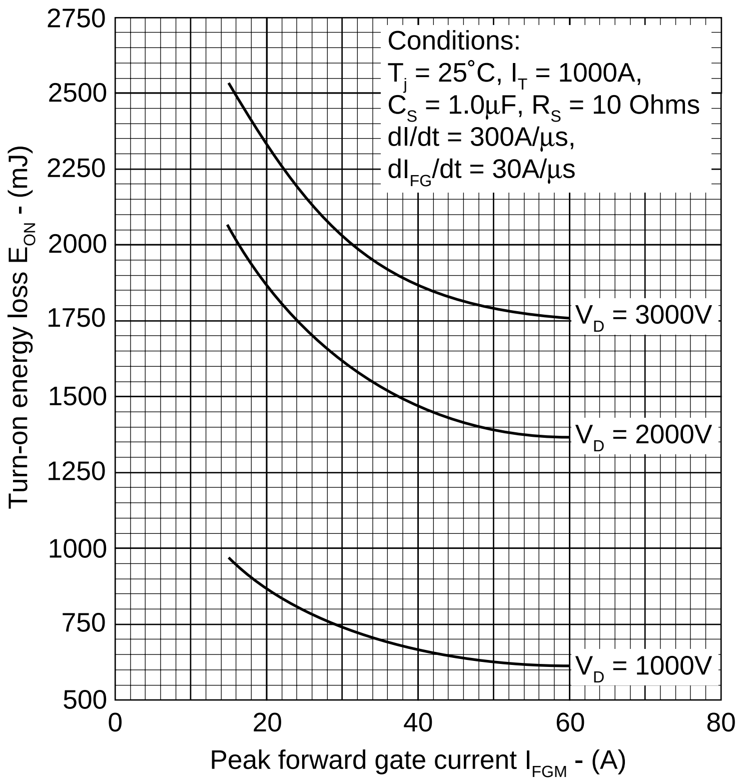


Fig.9 Turn-on energy vs peak forward gate current

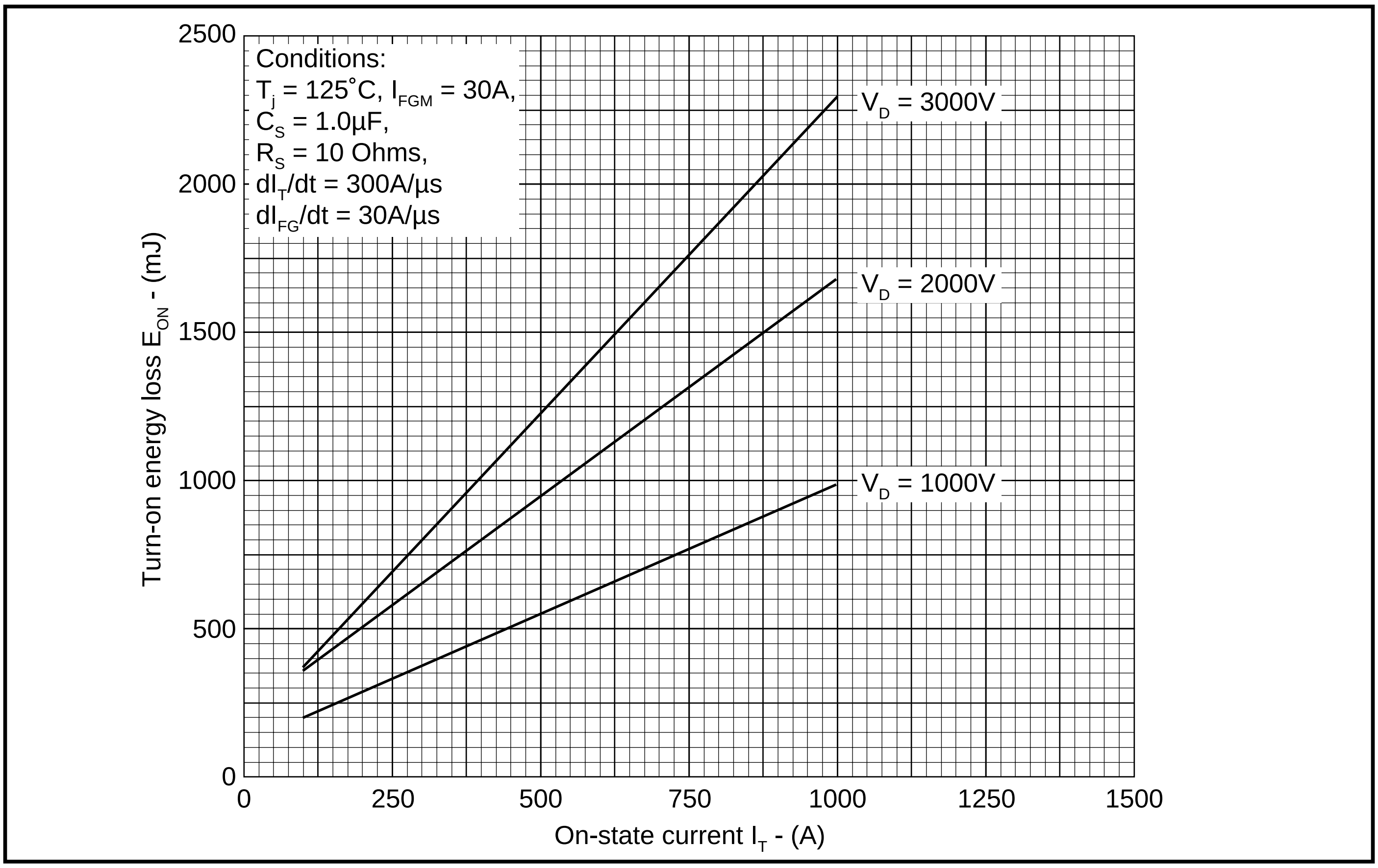


Fig.10 Turn-on energy vs on-state current

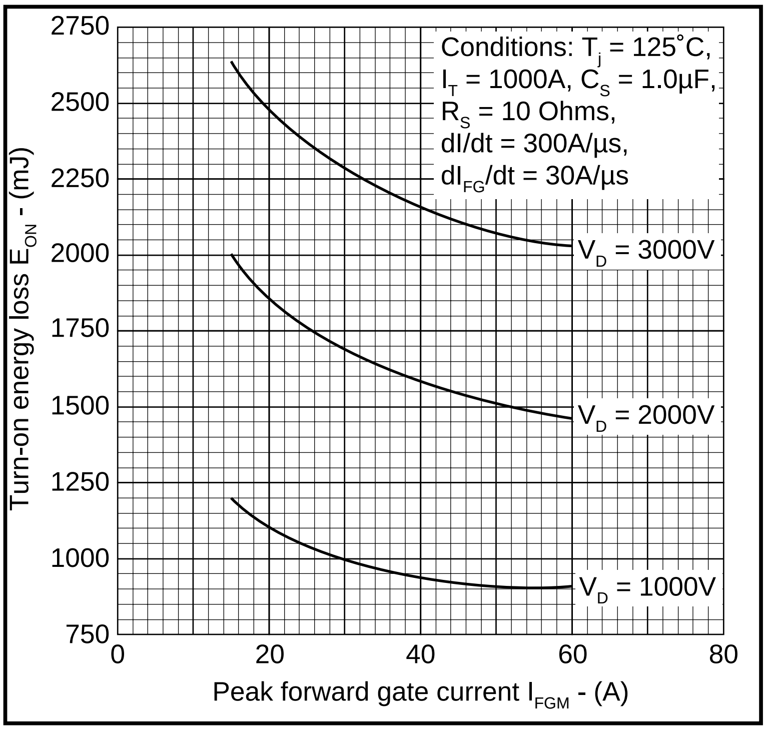


Fig.11 Turn-on energy vs peak forward gate current

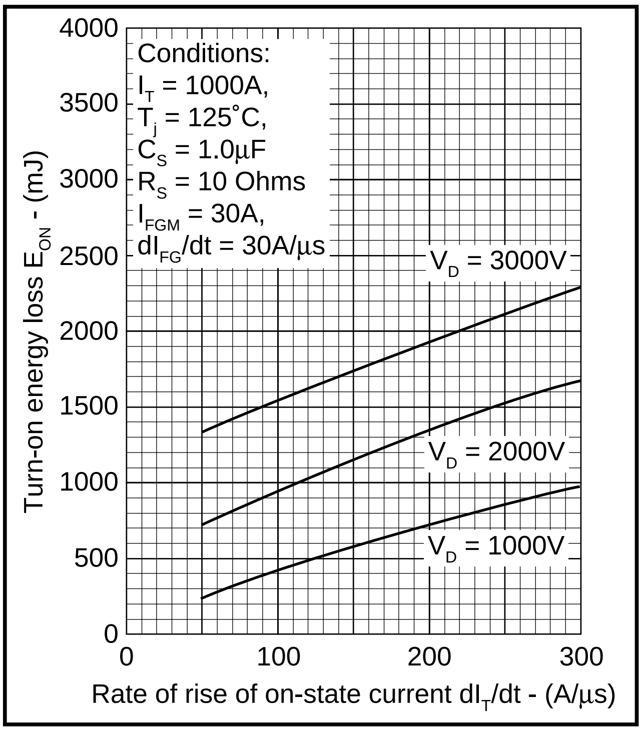


Fig.12 Turn-on energy vs rate of rise of on-state current

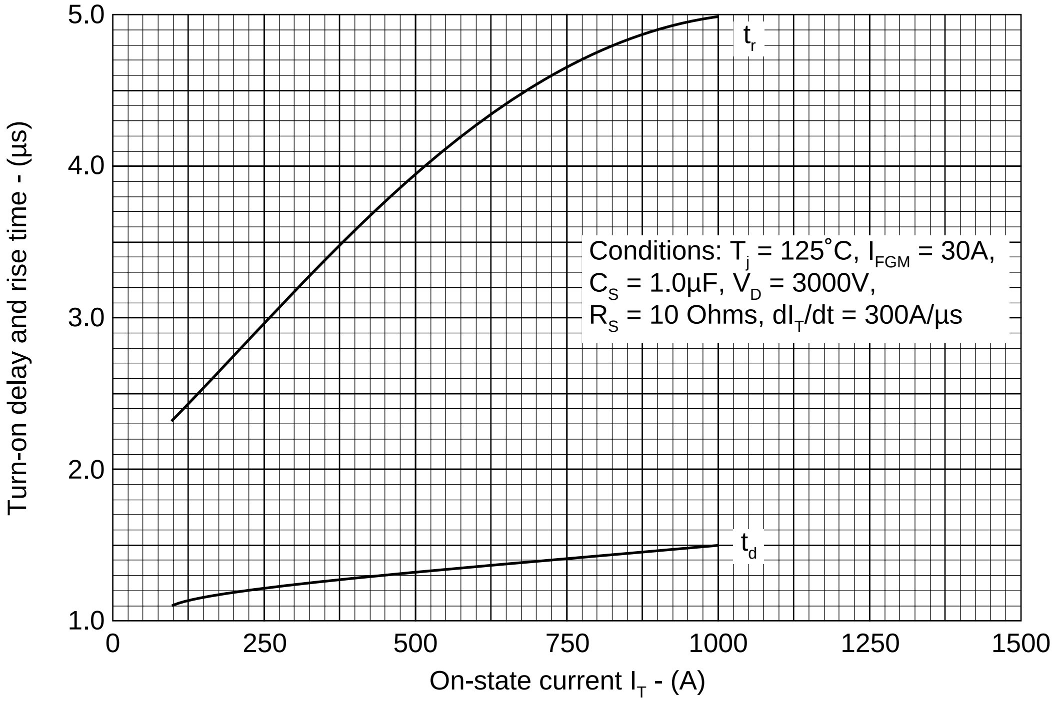


Fig.13 Delay time & rise time vs turn-on current

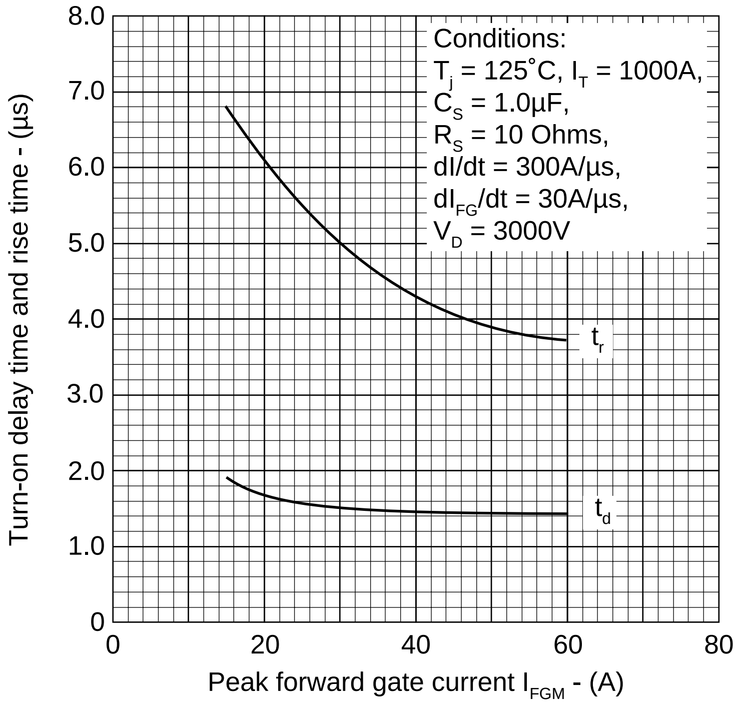


Fig.14 Delay time & rise time vs peak forward gate current

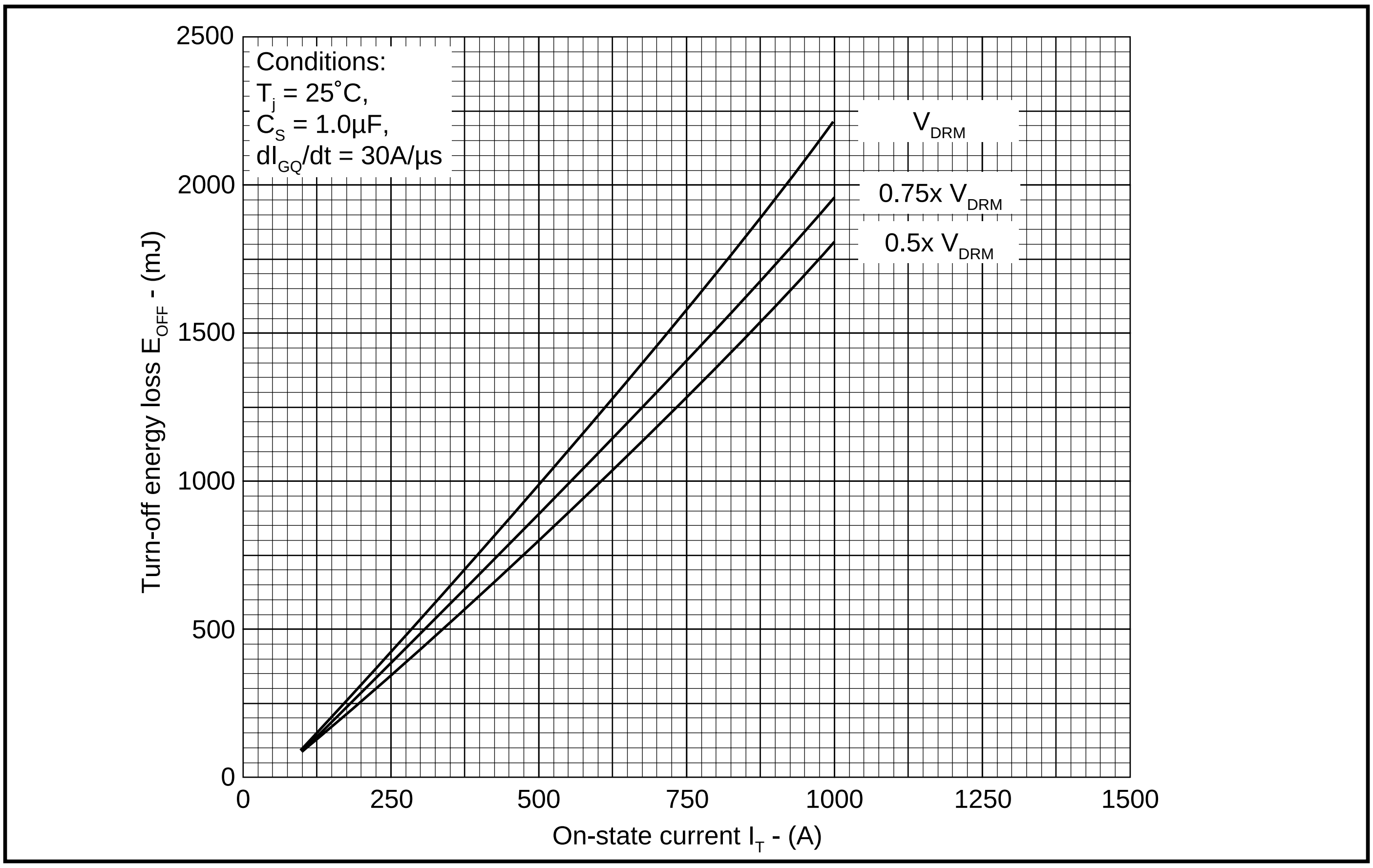


Fig.15 Turn-off energy vs on-state current

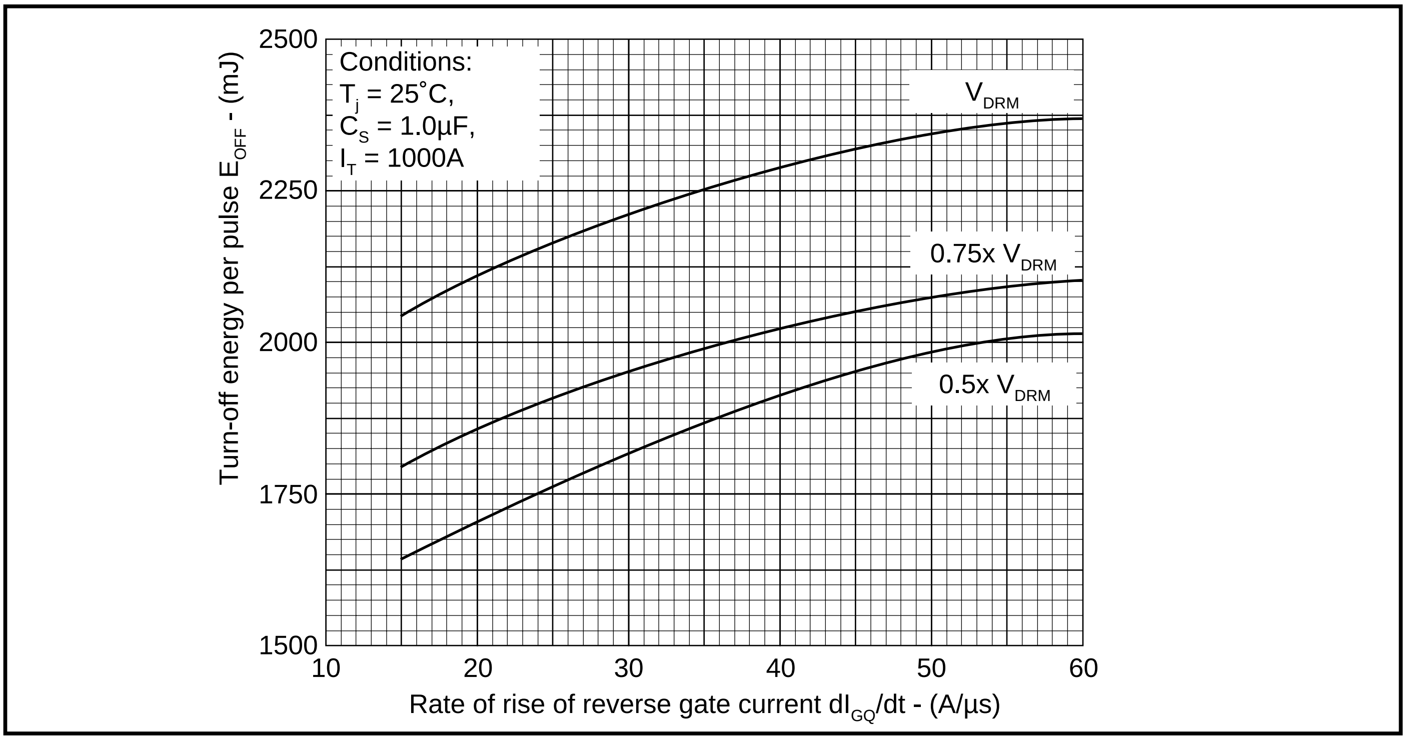


Fig.16 Turn-off energy vs rate of rise of reverse gate current

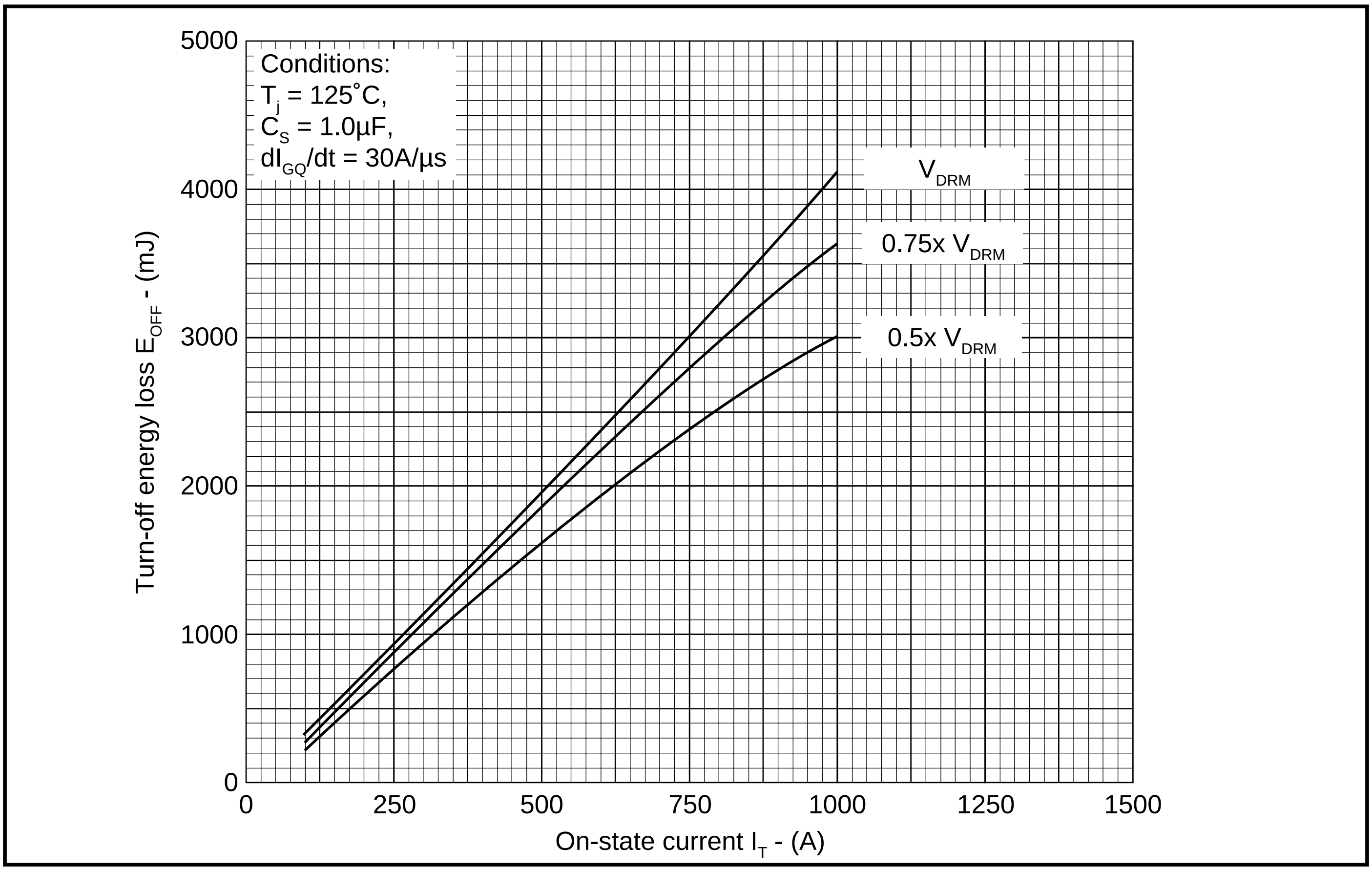


Fig.17 Turn-off energy vs on-state current

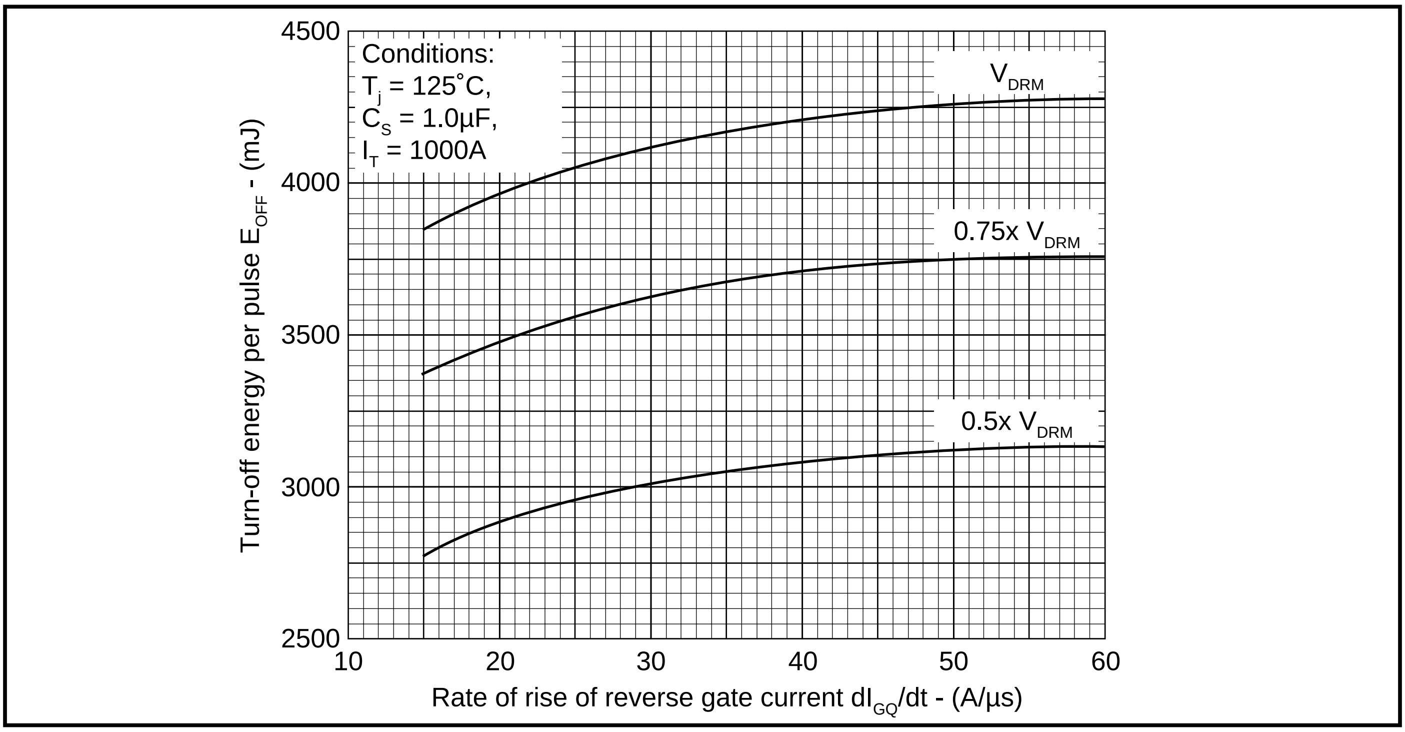


Fig.18 Turn-off energy loss vs rate of rise of reverse gate current

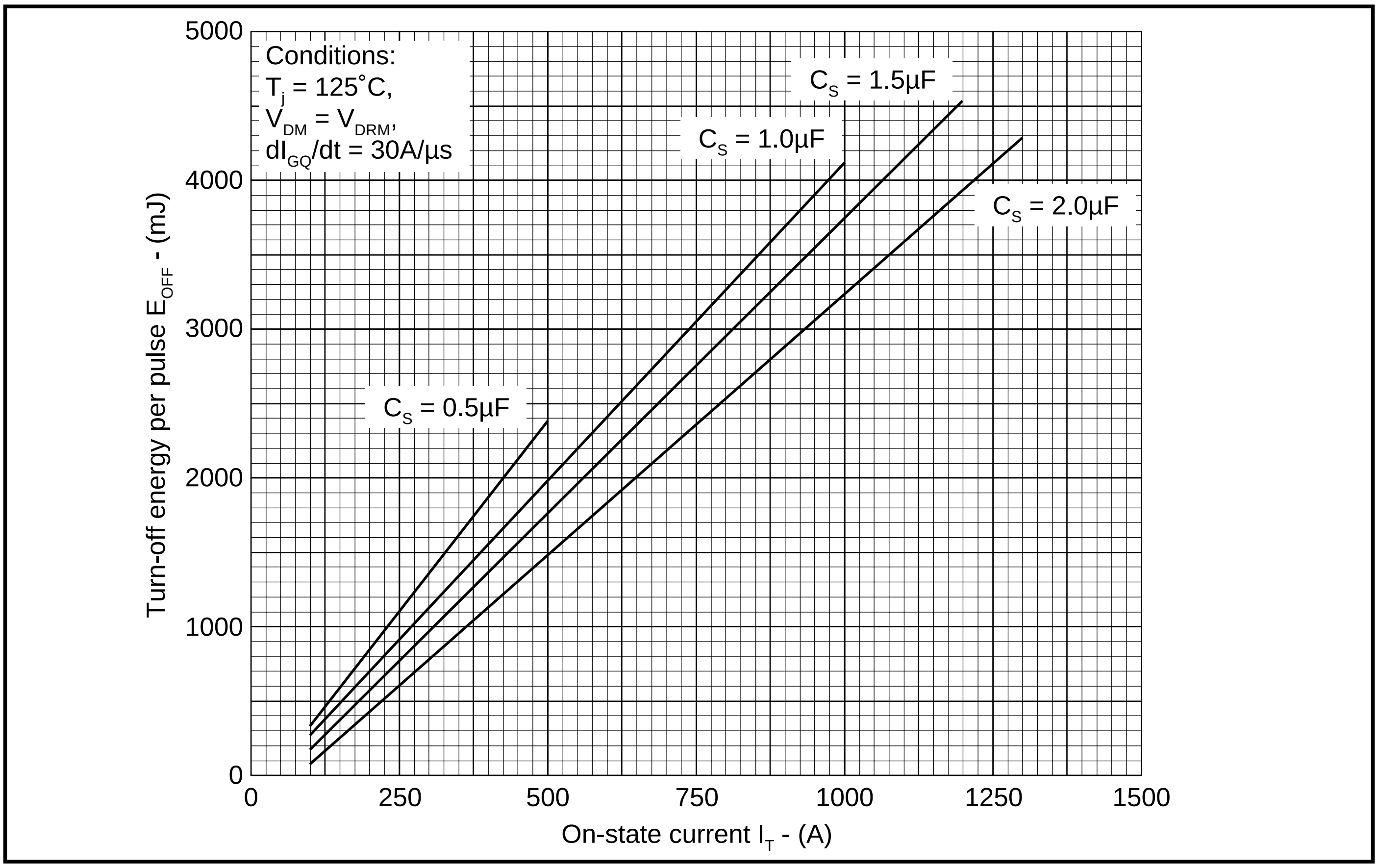


Fig.19 Turn-off energy vs on-state current

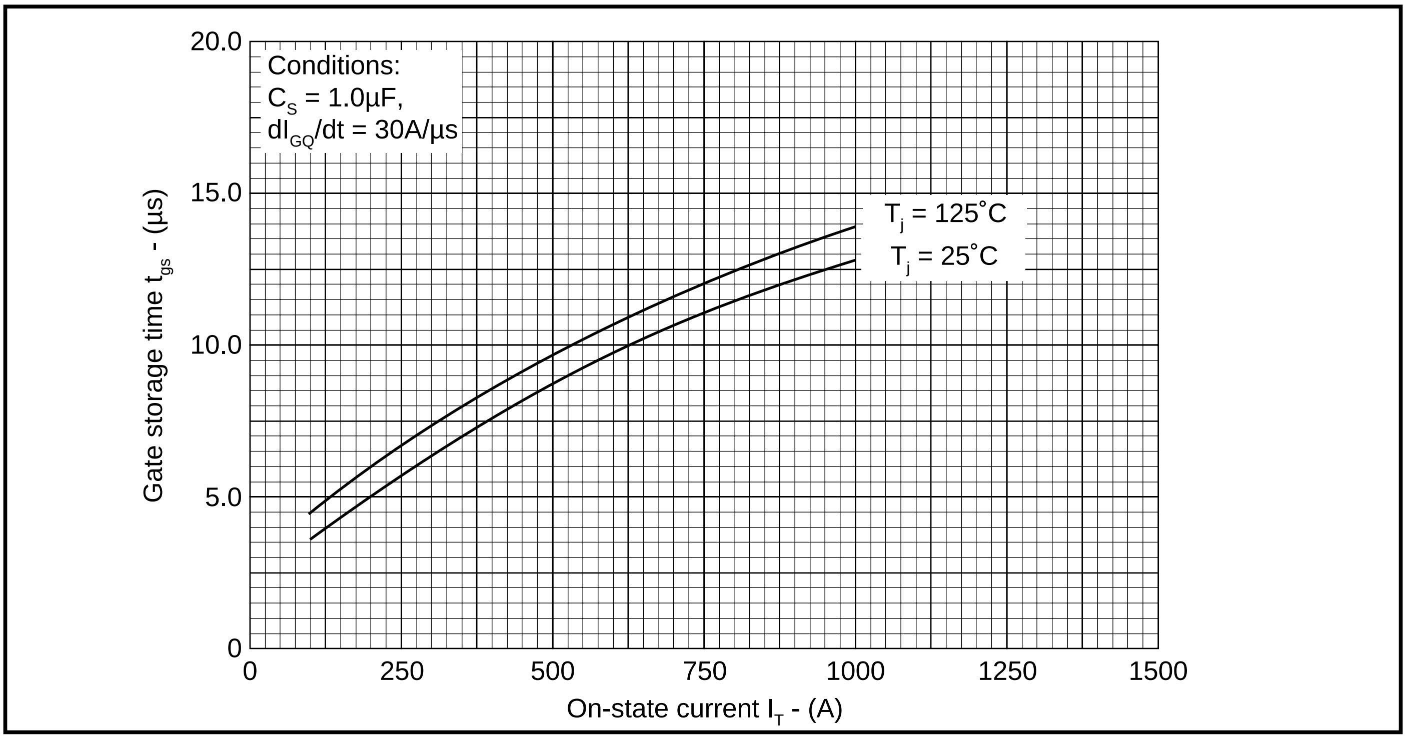


Fig.20 Gate storage time vs on-state current

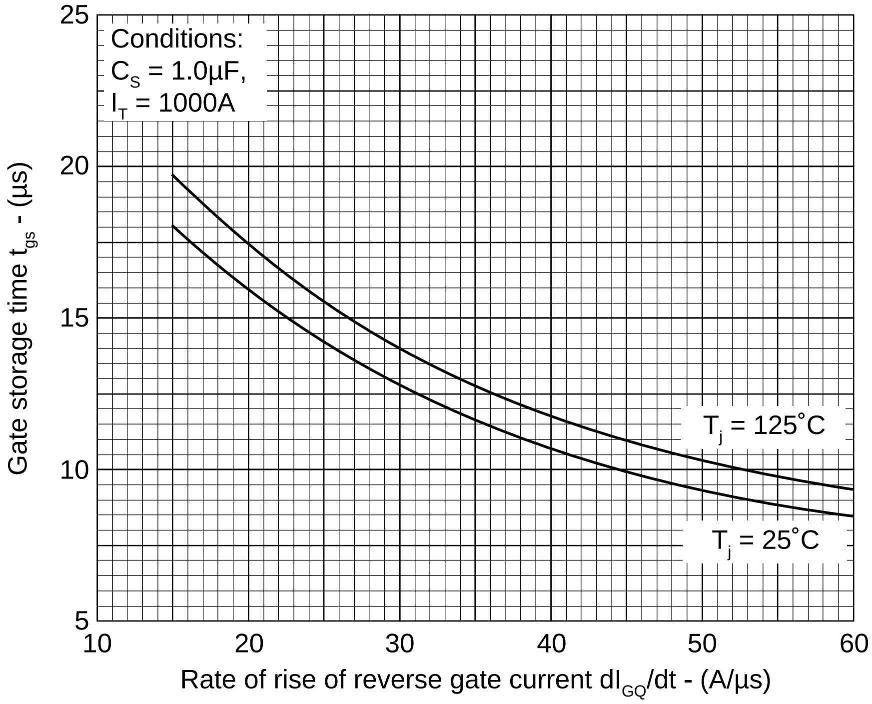


Fig.21 Gate storage time vs rate of rise of reverse gate current

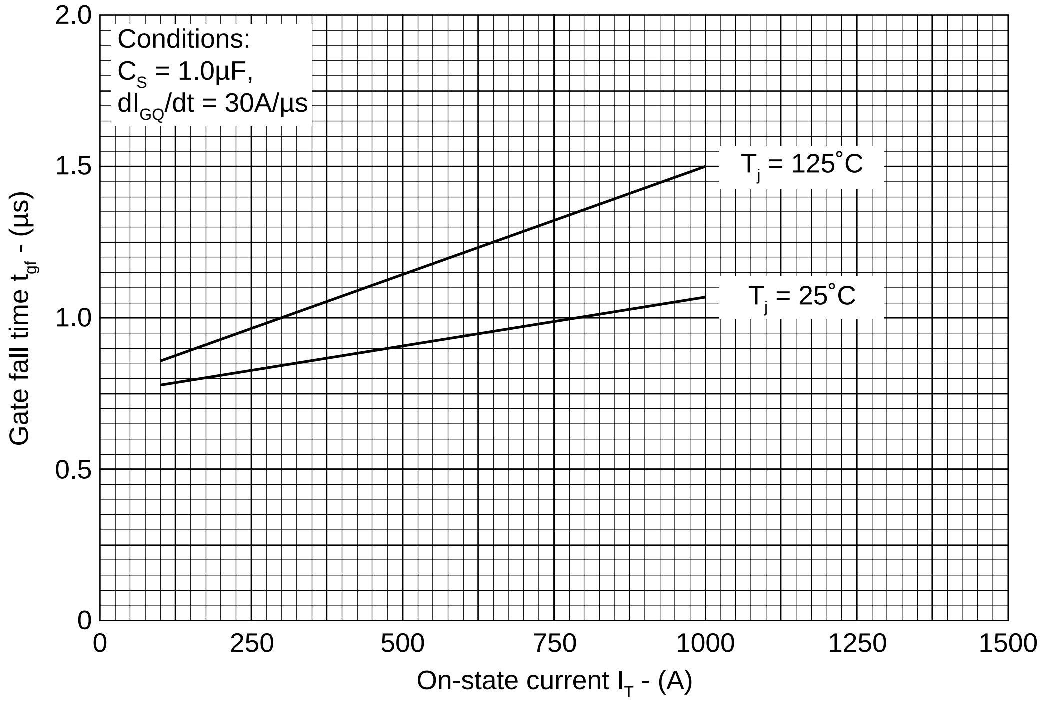


Fig.22 Gate fall time vs on-state current

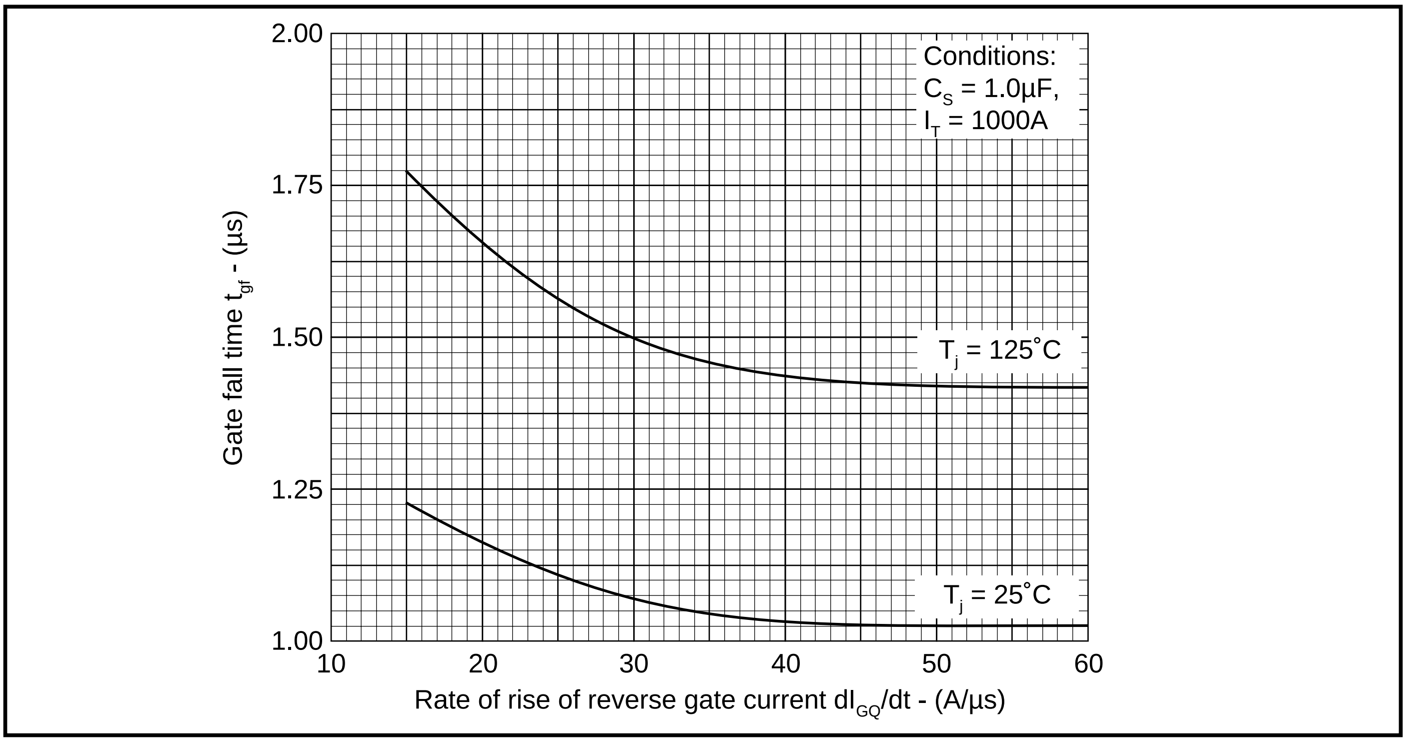


Fig.23 Gate fall time vs rate of rise of reverse gate current

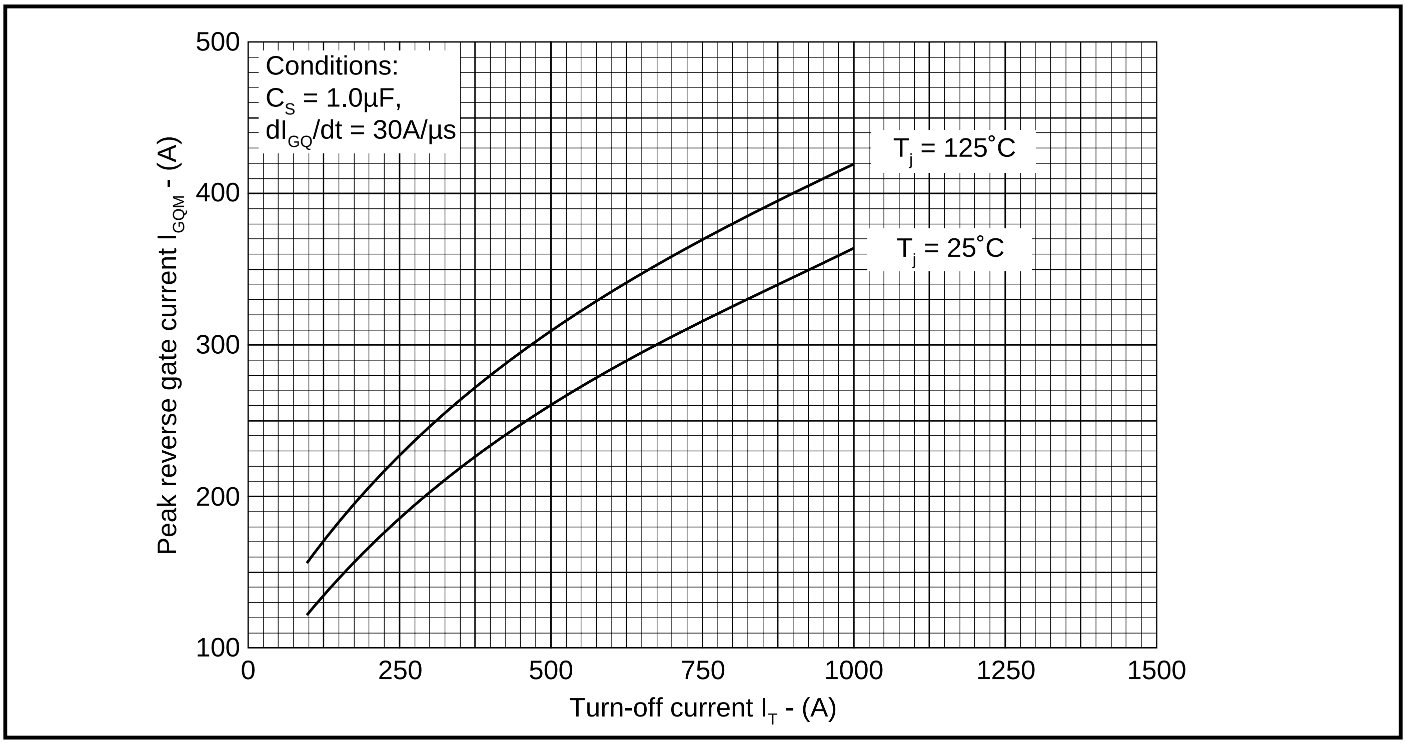


Fig.24 Peak reverse gate current vs turn-off current

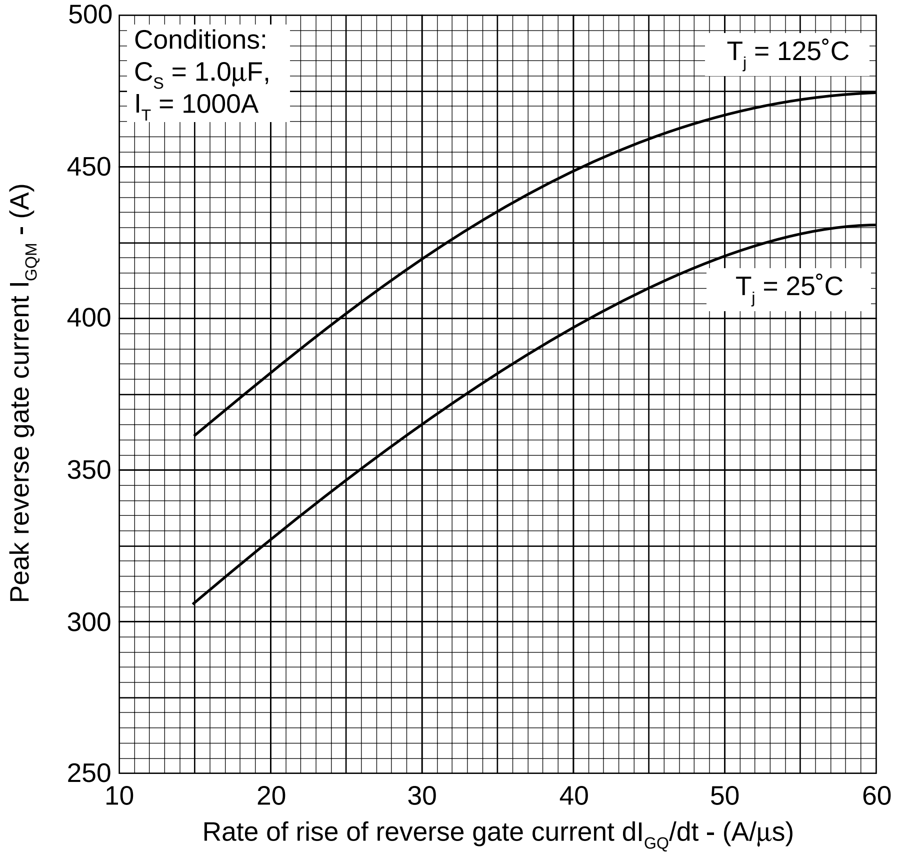


Fig.25 Peak reverse gate current vs rate of rise of reversegate current

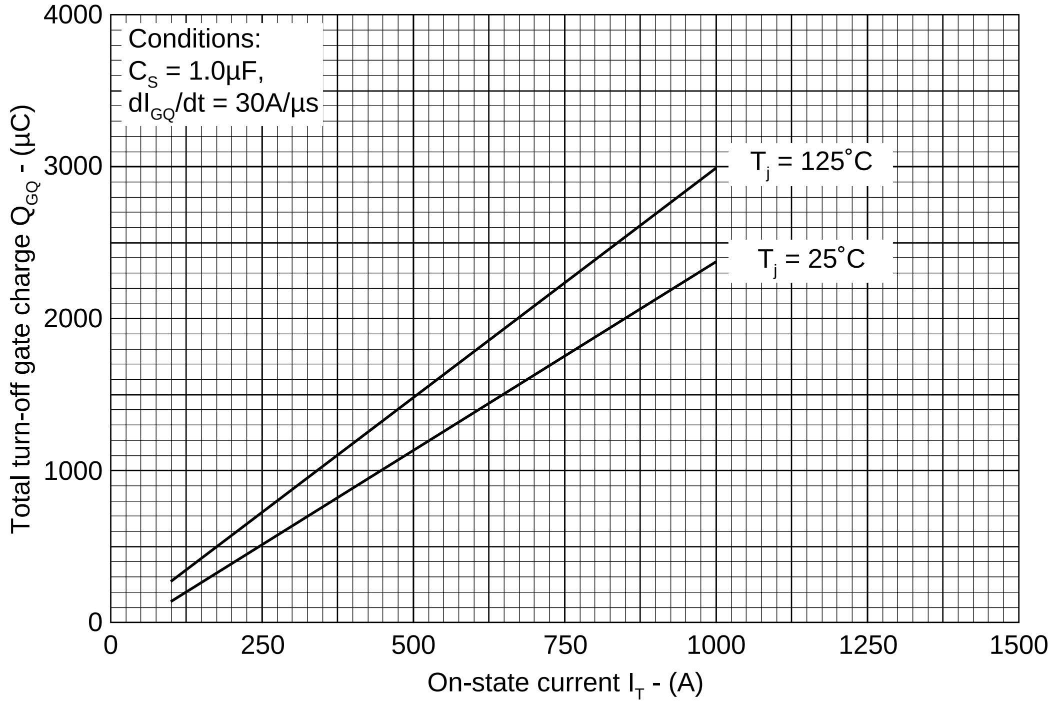


Fig.26 Turn-off gate charge vs on-state current

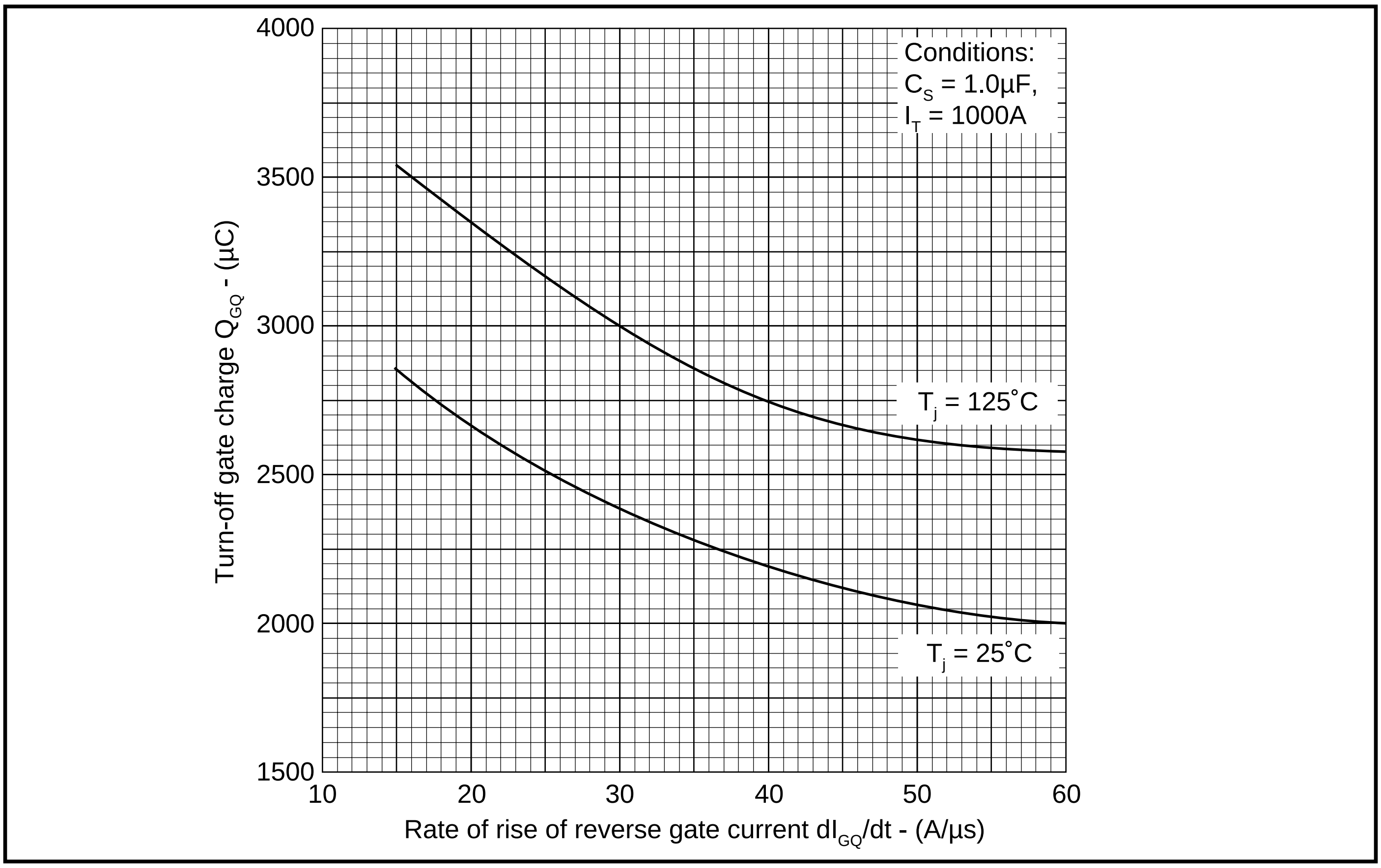


Fig.27 Turn-off gate charge vs rate of rise of reverse gate current

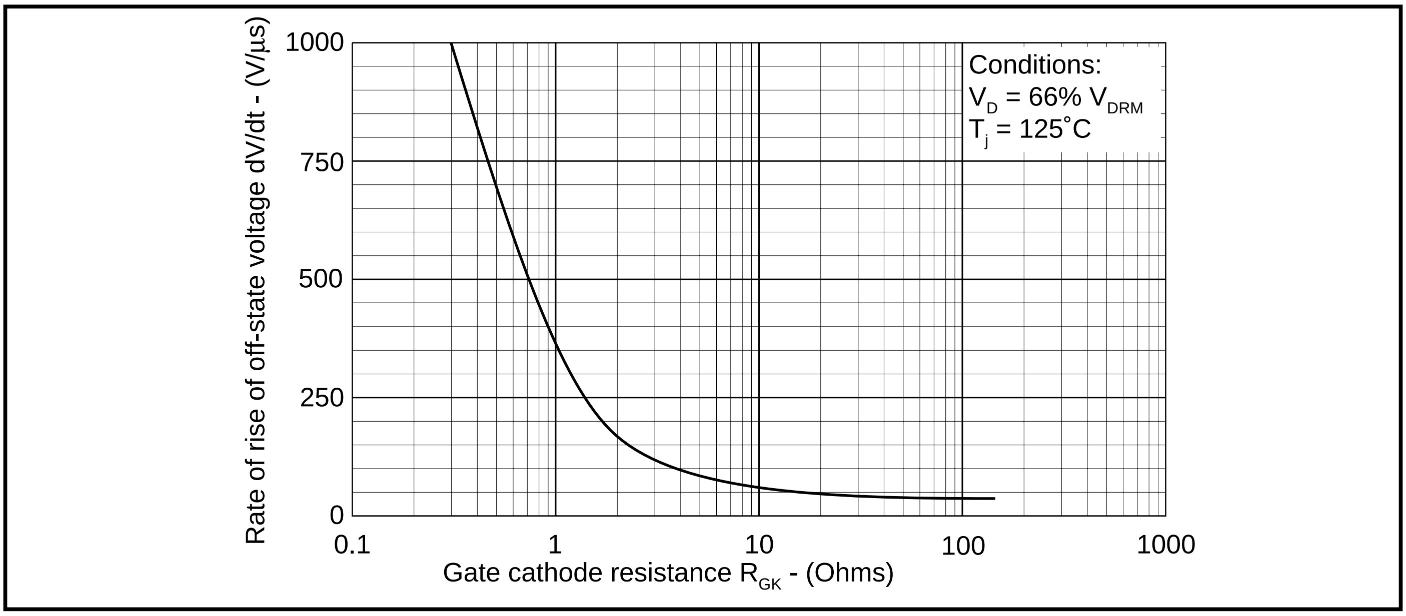
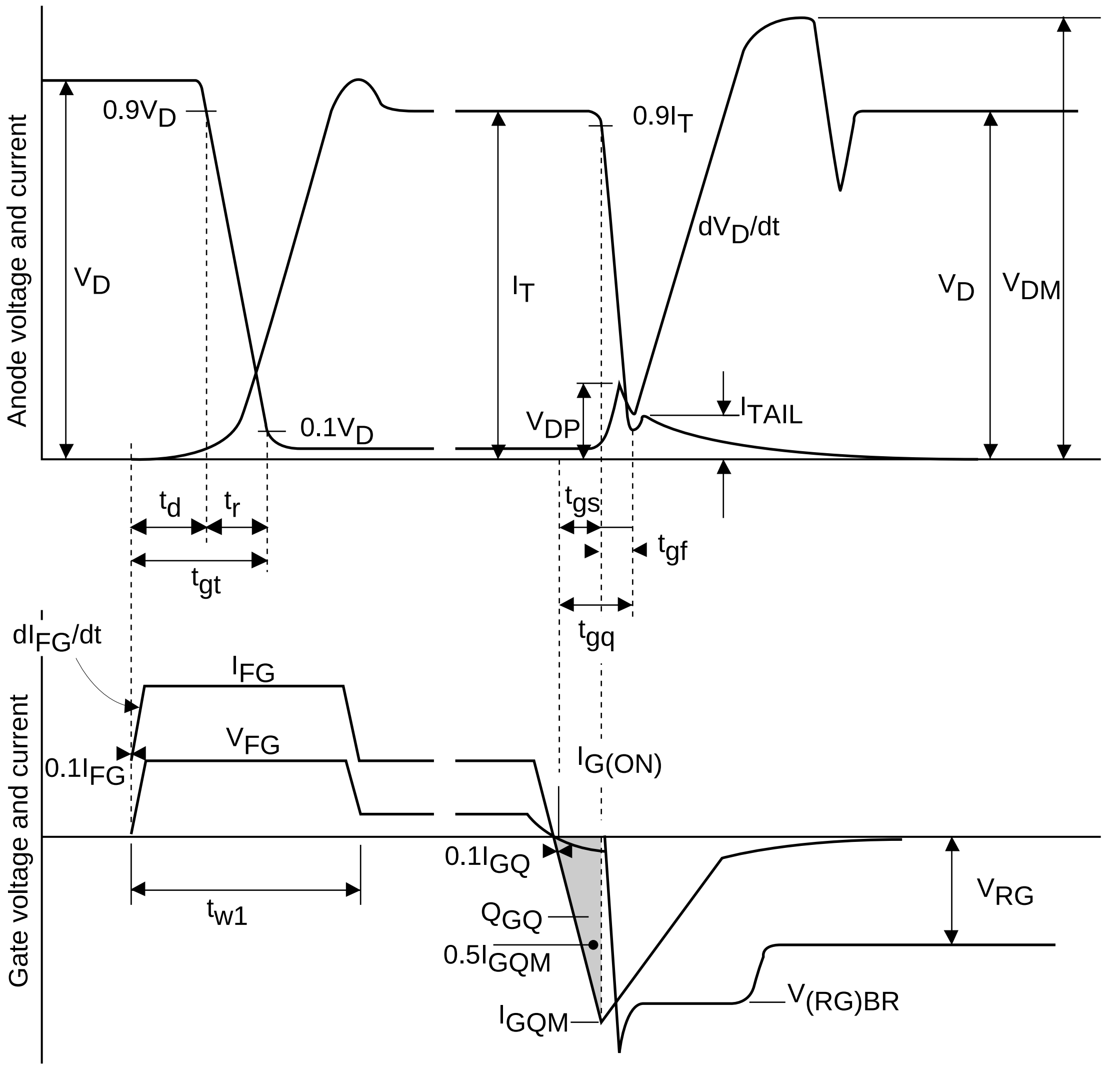


Fig.28 Rate of rise of off-state voltage vs gate cathode resistance



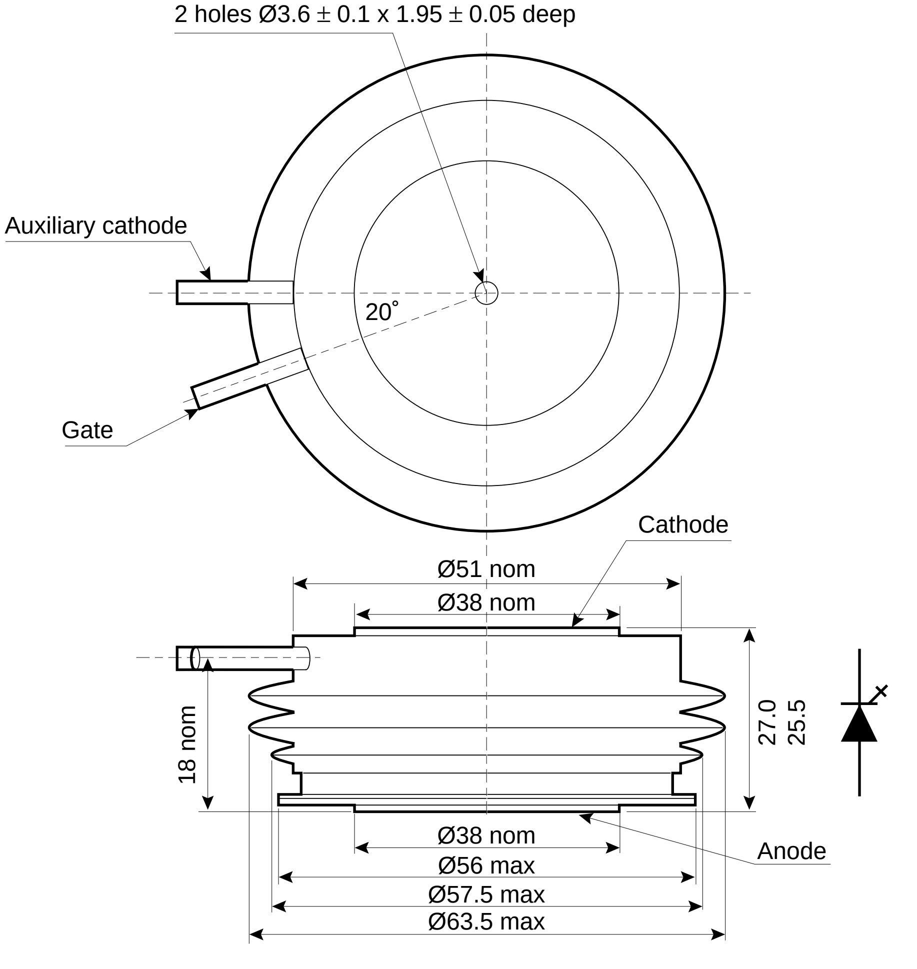
Recommended gate conditions:
I_{TCM} = 1000A
I_{FG} = 30A
$I_{G(ON)}$ = 4A d.c.
$t_{w1(min)}$ = 20μs
I_{GQM} = 420A
di_{GQ}/dt = 30A/μs
Q_{GQ} = 3000μC
$V_{RG(min)}$ = 2V
$V_{RG(max)}$ = 16V

These are recommended Dynex Semiconductor conditions. Other conditions are permitted according to users gate drive specifications.

Fig.29 General switching waveforms

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise.
DO NOT SCALE.



Nominal weight: 350g
Clamping force: 12kN ±10%
Lead length: 505mm

Package outine type code: P

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

http://www.dynexsemi.com

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