DG858BW45

Gate Turn-off Thyristor

Replaces July 1999 version, DS4096-3.0

DS4096-4.0 January 2000

FEATURES

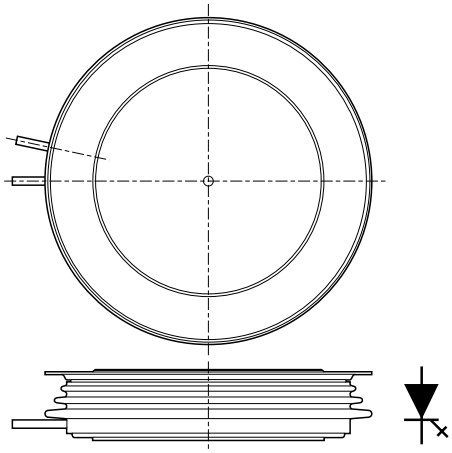
- Double Side Cooling
- High Reliability In Service
- High Voltage Capability
- Fault Protection Without Fuses
- High Surge Current Capability
- Turn-off Capability Allows Reduction In Equipment Size And Weight. Low Noise Emission Reduces Acoustic Cladding Necessary For Environmental Requirements

KEY PARAMETERS

I_{TCM}	3000A
V_{DRM}	4500V
$I_{T(AV)}$	1180A
dV_D/dt	1000V/μs
di_T/dt	300A/μs

APPLICATIONS

- Variable speed A.C. motor drive inverters (VSD-AC)
- Uninterruptable Power Supplies
- High Voltage Converters
- Choppers
- Welding
- Induction Heating
- DC/DC Converters



Package outline type code: W.
See Package Details for further information.

Figure 1. Package outline

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} V	Repetitive Peak Reverse Voltage V_{RRM} V	Conditions
DG858BW45	4500	16	T_{vj} = 125°C, I_{DM} = 100mA, I_{RRM} = 50mA

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TCM}	Repetitive peak controllable on-state current	V_D = 66% V_{DRM}, T_j = 125°C, di_{GQ}/dt = 40A/μs, Cs = 3μF	3000	A
$I_{T(AV)}$	Mean on-state current	T_{HS} = 80°C. Double side cooled, half sine 50Hz	1180	A
$I_{T(RMS)}$	RMS on-state current	T_{HS} = 80°C. Double side cooled, half sine 50Hz	1850	A

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine. T_j = 125°C	20.0	kA
I^2t	I^2t for fusing	10ms half sine. T_j =125°C	2.0×10^6	A^2s
di_T/dt	Critical rate of rise of on-state current	V_D = 3000V, I_T = 3000A, T_j = 125°C, I_{FG} > 40A, Rise time > 1.0µs	300	A/µs
dV_D/dt	Rate of rise of off-state voltage	To 66% V_{DRM}; $R_{GK} \leq 1.5\Omega$, T_j = 125°C	130	V/µs
		To 66% V_{DRM}; V_{RG} = -2V, T_j = 125°C	1000	V/µs
L_S	Peak stray inductance in snubber circuit	I_T = 3000A, V_D = V_{DRM}, T_j = 125°C, $dI/_{GQ}$ = 40A/µs, Cs = 3.0µF	200	nH

GATE RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{RGM}	Peak reverse gate voltage	This value maybe exceeded during turn-off	-	16	V
I_{FGM}	Peak forward gate current		20	100	A
$P_{FG(AV)}$	Average forward gate power		-	20	W
P_{RGM}	Peak reverse gate power		-	24	kW
di_{GQ}/dt	Rate of rise of reverse gate current		20	60	A/µs
$t_{ON(min)}$	Minimum permissable on time		50	-	µs
$t_{OFF(min)}$	Minimum permissable off time		100	-	µs

THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-hs)}$	DC thermal resistance - junction to heatsink surface	Double side cooled		-	0.011	°C/W
		Anode side cooled		-	0.017	°C/W
		Cathode side cooled		-	0.03	°C/W
$R_{th(c-hs)}$	Contact thermal resistance	Clamping force 40.0kN With mounting compound	per contact	-	0.0021	°C/W
T_{vj}	Virtual junction temperature			-40	125	°C
T_{OP}/T_{stg}	Operating junction/storage temperature range			-40	125	°C
-	Clamping force			36.0	44.0	kN

CHARACTERISTICS

T_j = 125°C unless stated otherwise					
Symbol	**Parameter**	**Conditions**	**Min.**	**Max.**	**Units**
V_{TM}	On-state voltage	At 4000A peak, $I_{G(ON)}$ = 10A d.c.	-	4.0	V
I_{DM}	Peak off-state current	V_{DRM} = 4500V, V_{RG} = 0V	-	100	mA
I_{RRM}	Peak reverse current	At V_{RRM}	-	50	mA
V_{GT}	Gate trigger voltage	V_D = 24V, I_T = 100A, T_j = 25°C	-	1.2	V
I_{GT}	Gate trigger current	V_D = 24V, I_T = 100A, T_j = 25°C	-	4.0	A
I_{RGM}	Reverse gate cathode current	V_{RGM} = 16V, No gate/cathode resistor	-	50	mA
E_{ON}	Turn-on energy	V_D = 2000V	-	2700	mJ
t_d	Delay time	I_T = 3000A, dI_T/dt = 300A/µs	-	2.0	µs
t_r	Rise time	I_{FG} = 40A, rise time < 1.0µs	-	6.0	µs
E_{OFF}	Turn-off energy		-	13500	mJ
t_{gs}	Storage time		-	25.0	µs
t_{gf}	Fall time	I_T = 3000A, V_{DM} = V_{DRM}	-	2.5	µs
t_{gq}	Gate controlled turn-off time	Snubber Cap Cs = 3.0µF,	-	27.5	µs
Q_{GQ}	Turn-off gate charge	di_{GQ}/dt = 40A/µs	-	12000	µC
Q_{GQT}	Total turn-off gate charge		-	24000	µC
I_{GQM}	Peak reverse gate current		-	950	A

CURVES

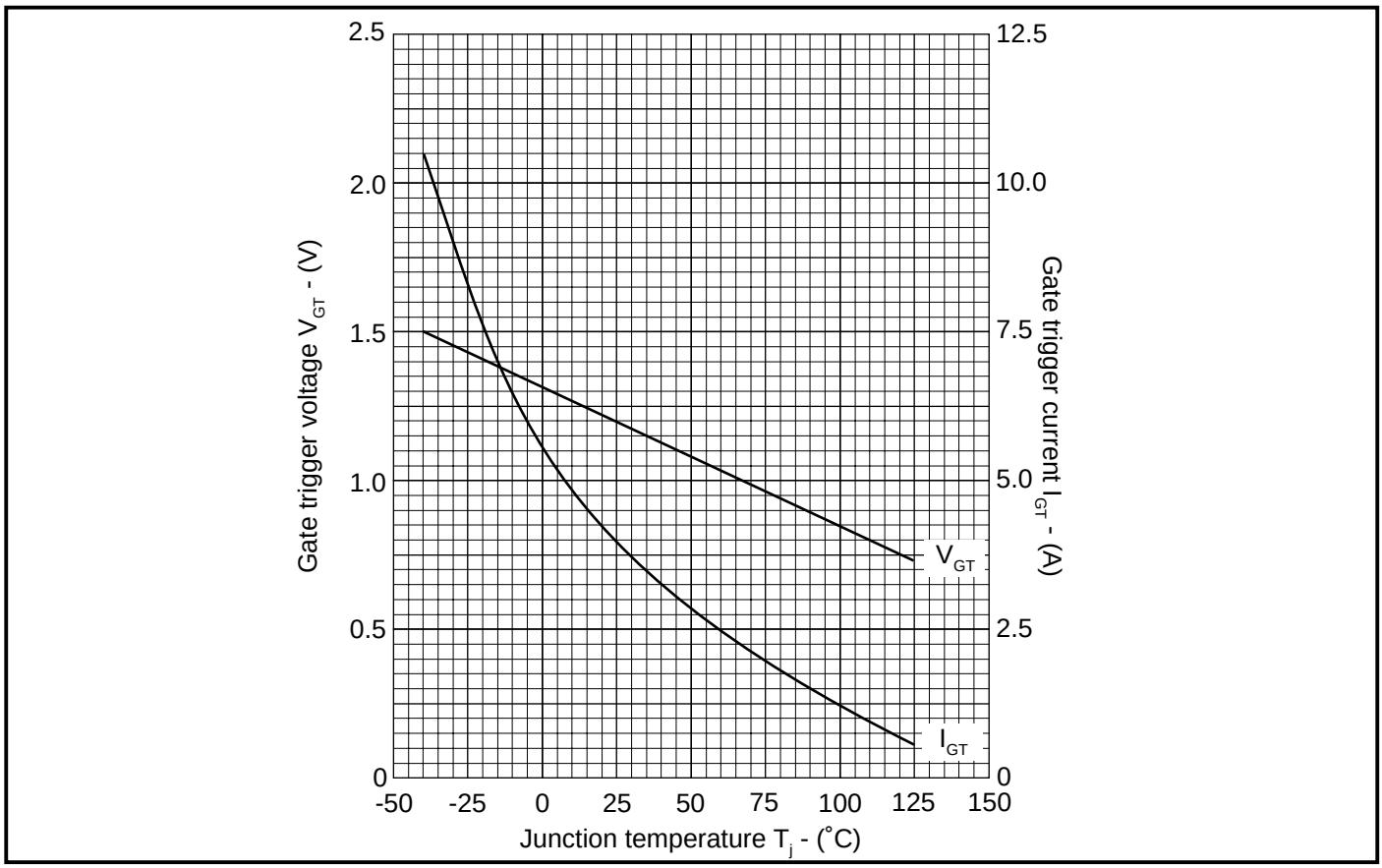


Figure 2. Maximum gate trigger voltage/current vs junction temperature

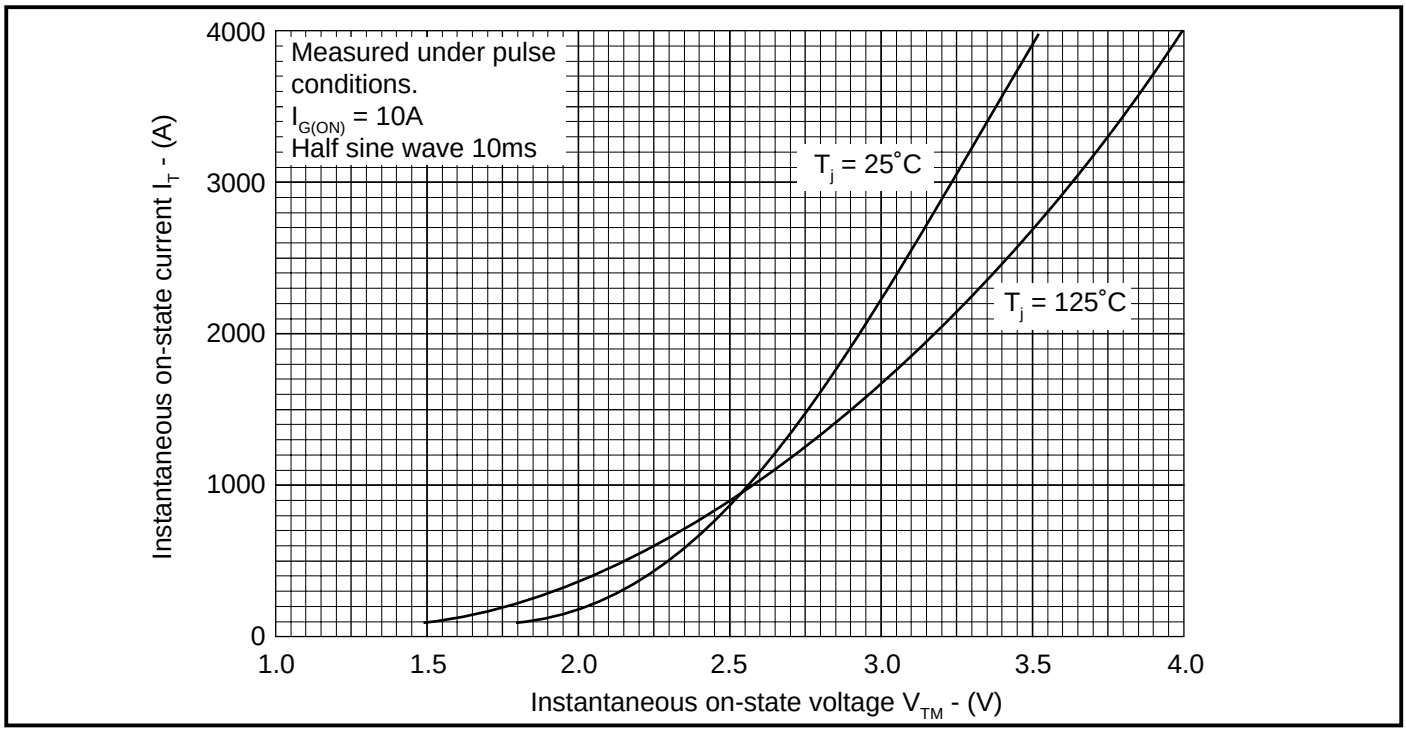


Figure 3. On-state characteristics

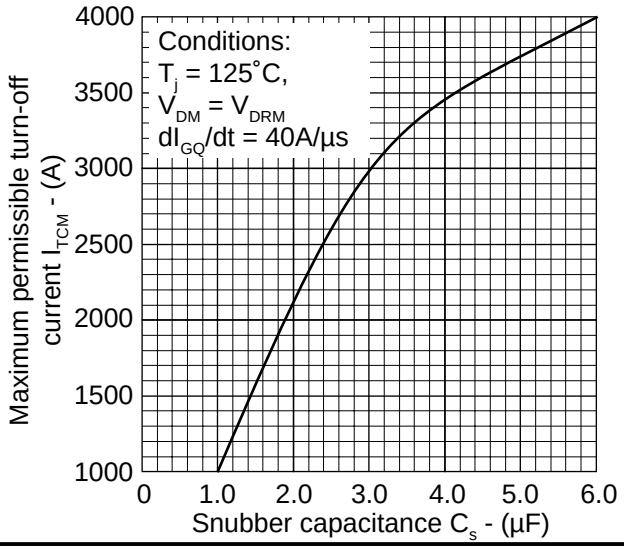


Figure 4. Maximum dependence of I_{TCM} on Cs

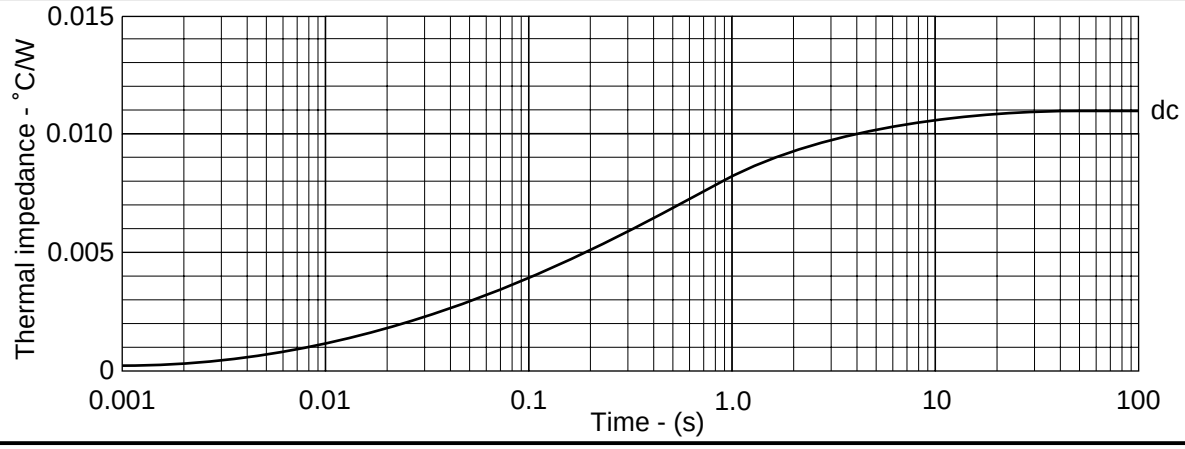


Figure 5. Maximum (limit) transient thermal impedance - double side cooled

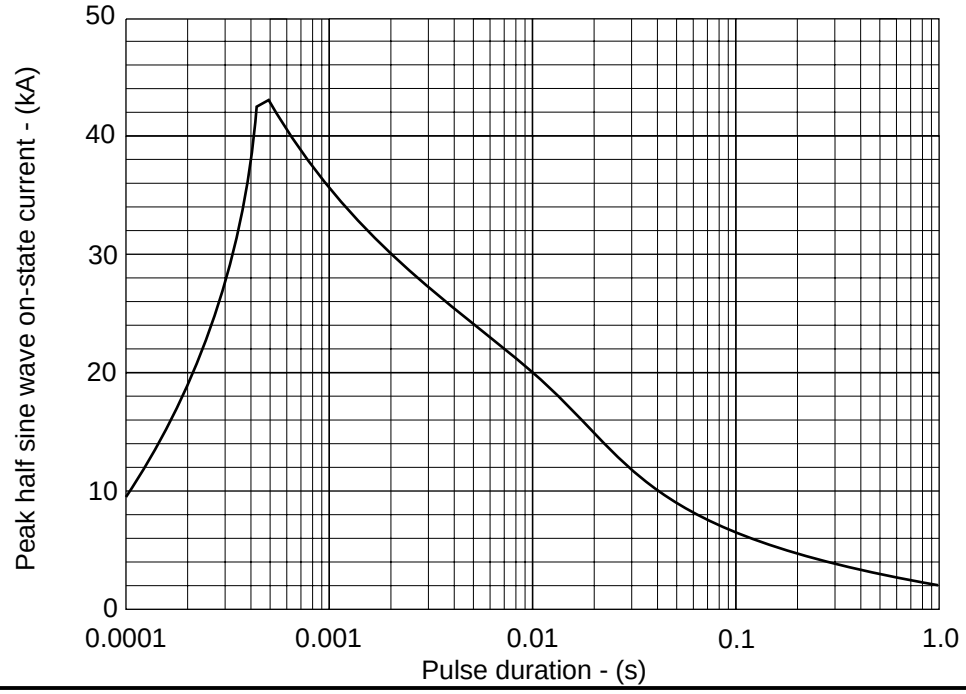


Figure 6. Surge (non-repetitive) on-state current vs time

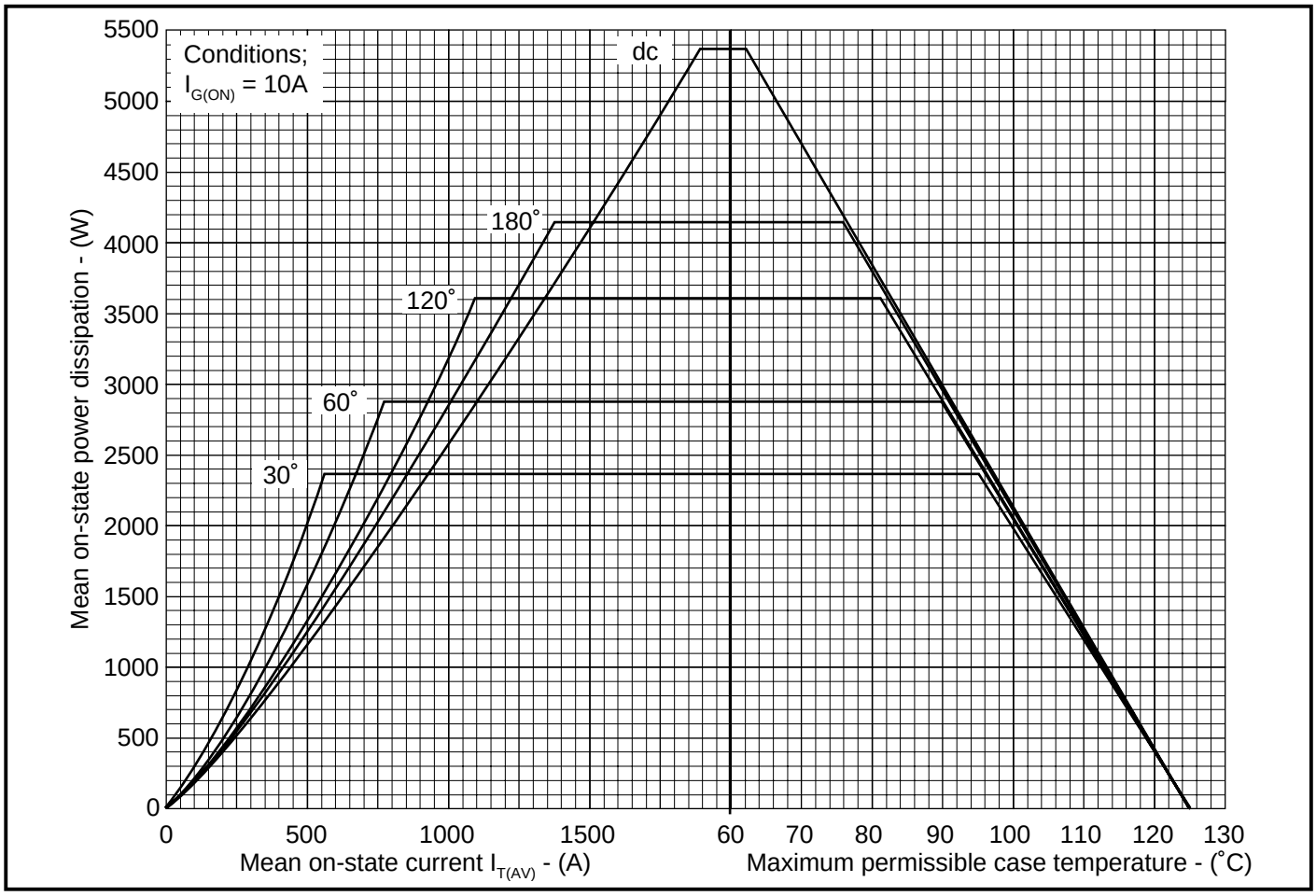


Figure 7. Steady state rectangular wave conduction loss - double side cooled

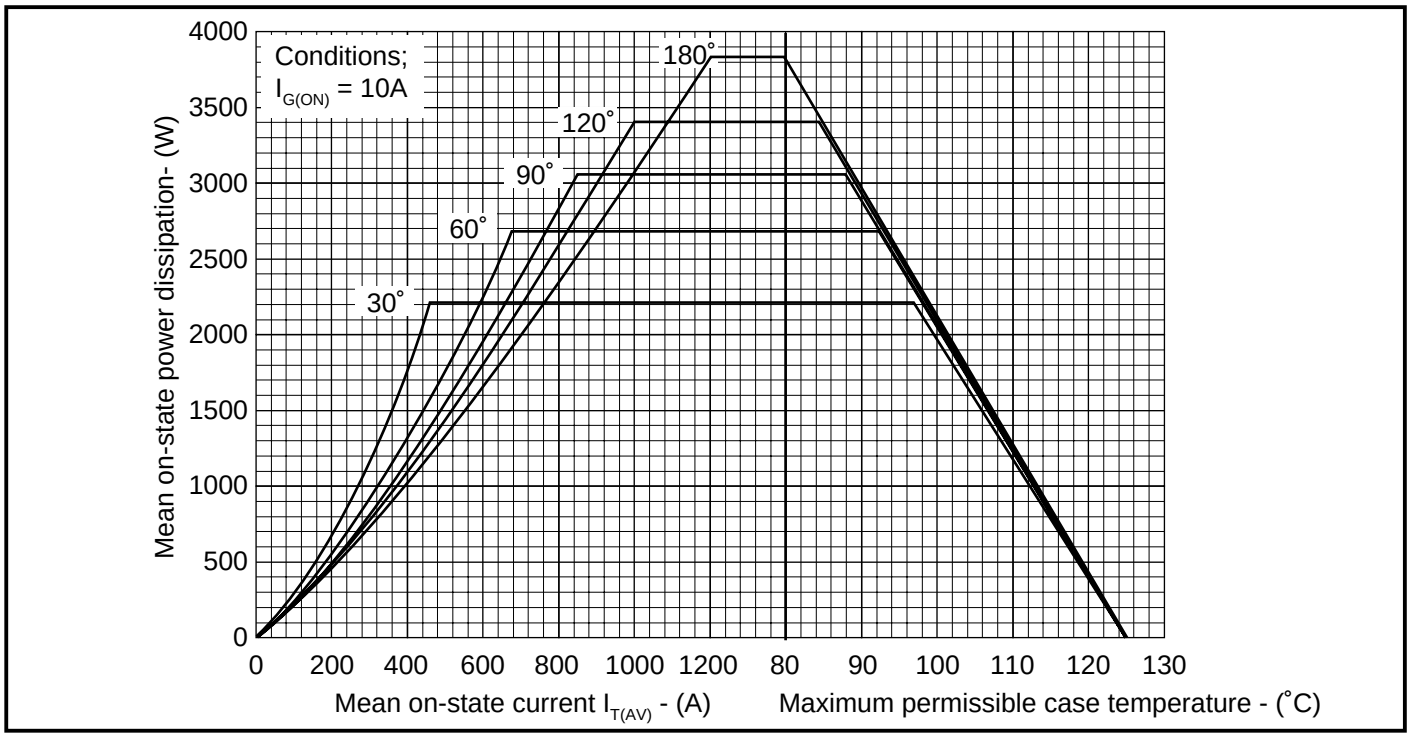


Figure 8. Steady state sinusoidal wave conduction loss - double side cooled

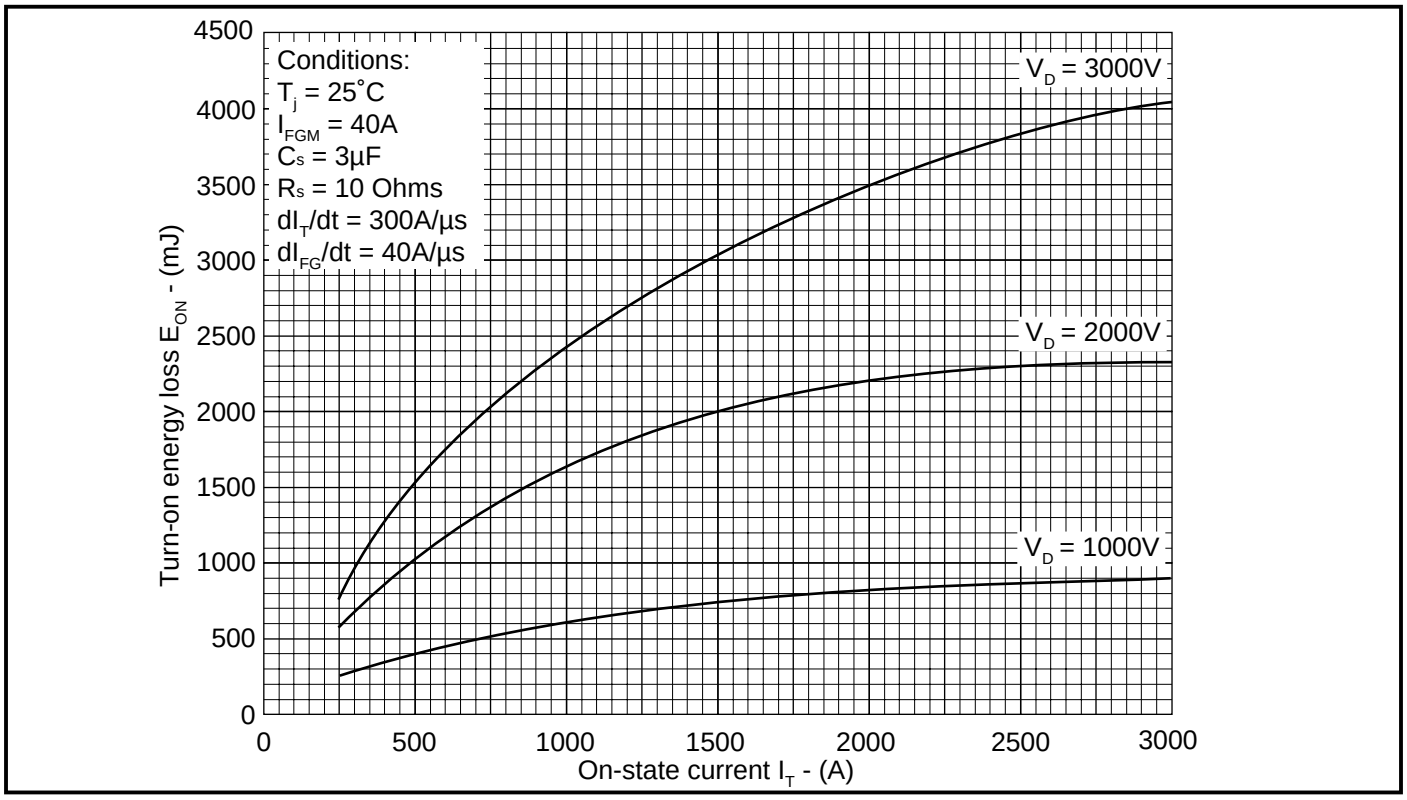


Figure 9. Turn-on energy vs on-state current

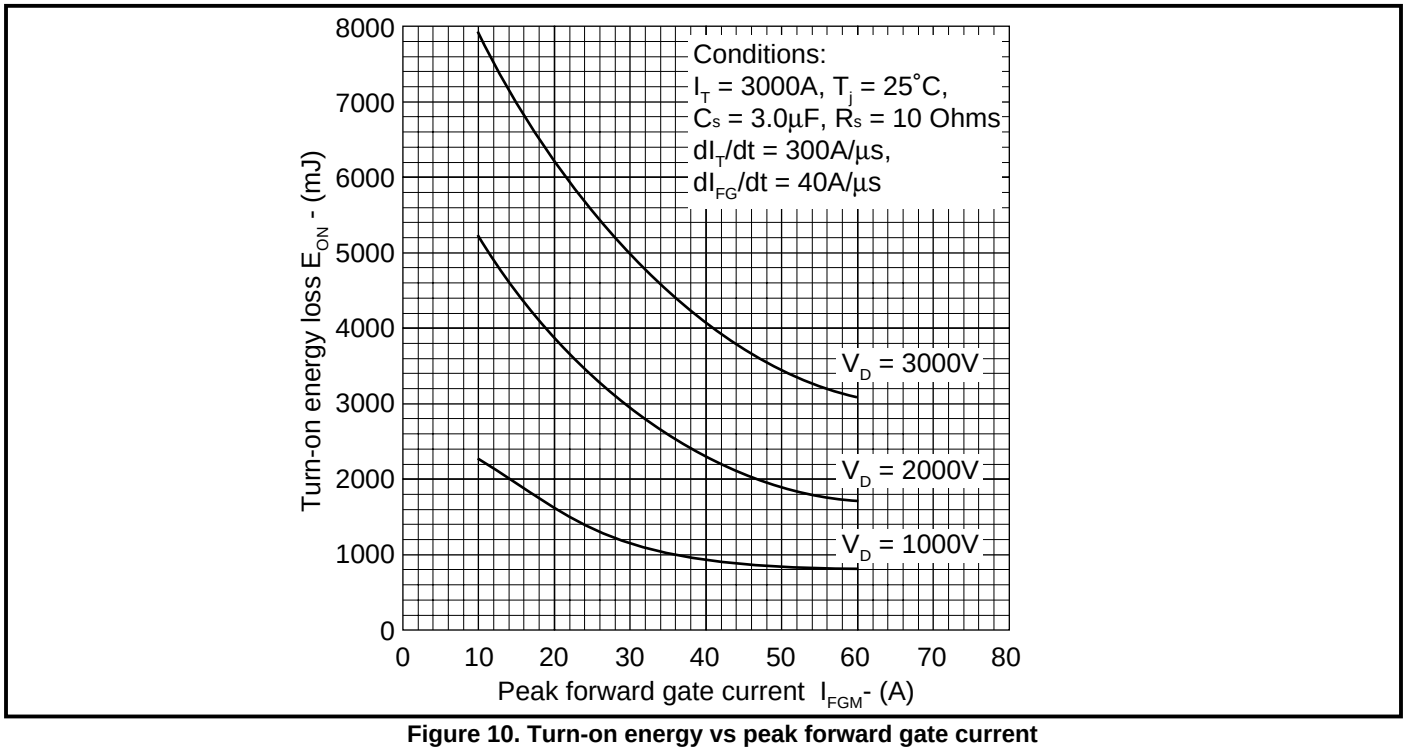


Figure 10. Turn-on energy vs peak forward gate current

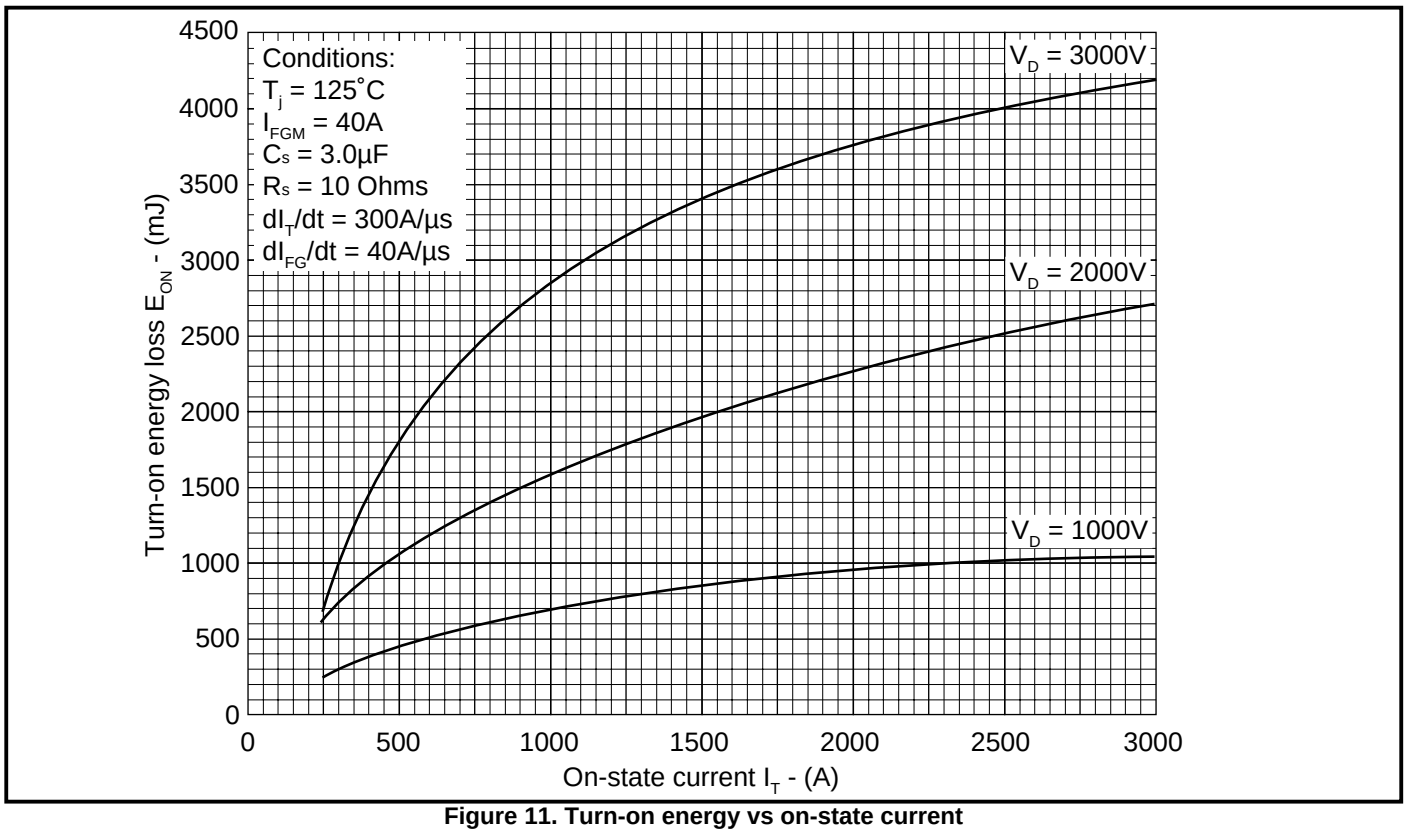


Figure 11. Turn-on energy vs on-state current

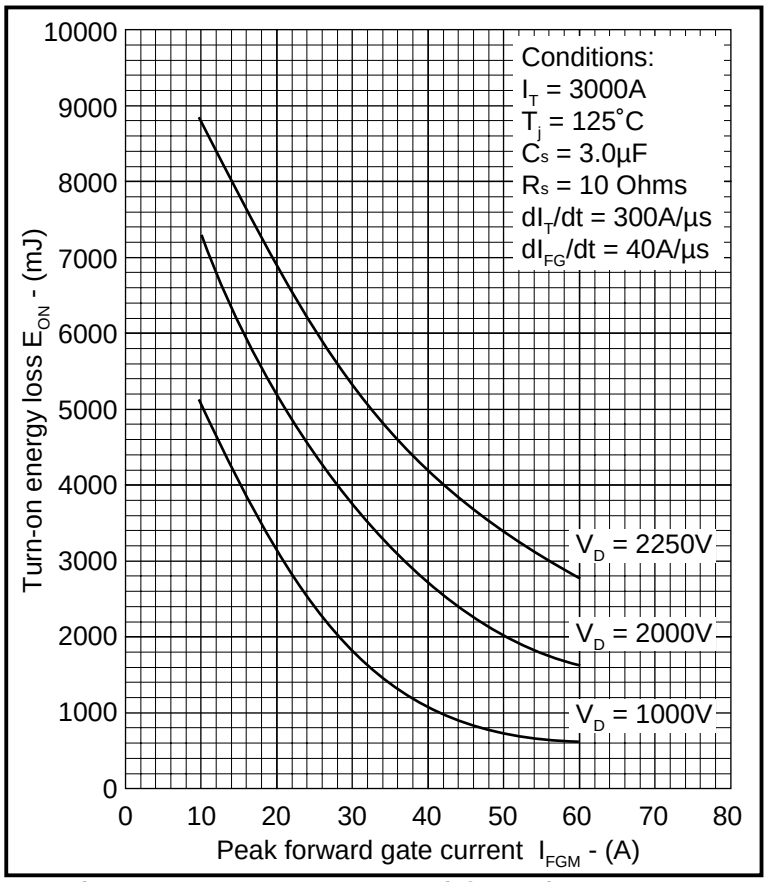


Figure 12. Turn-on energy vs peak forward gate current

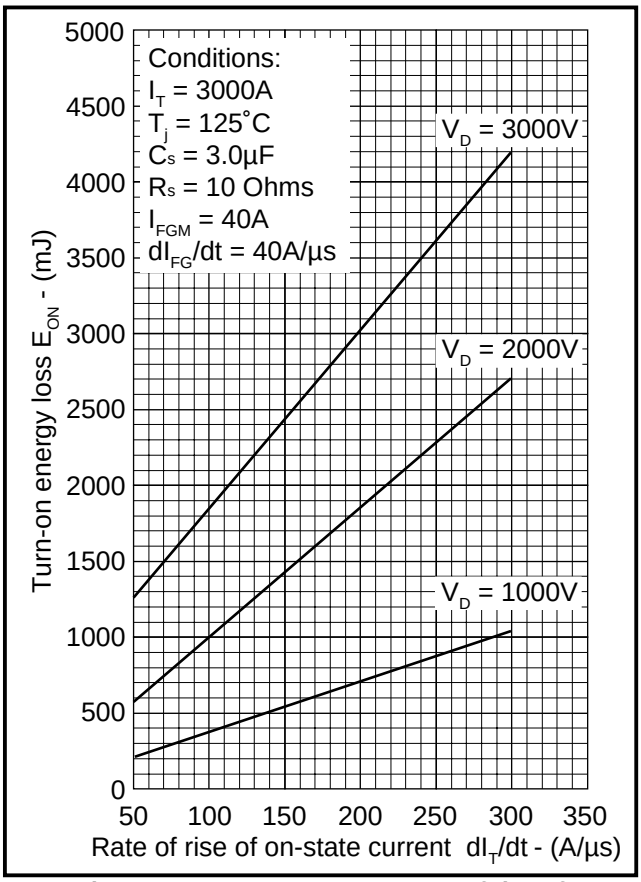


Figure 13. Turn-on energy vs rate of rise of on-state current

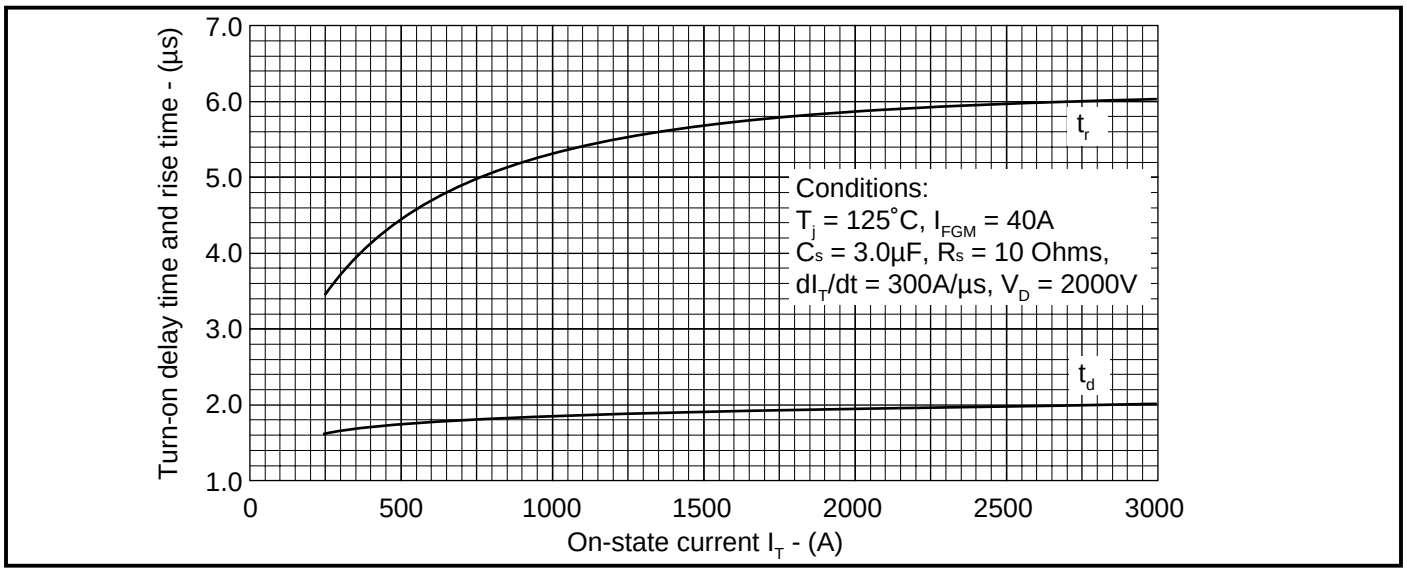


Fig.ure 14. Delay and rise time vs on-state current

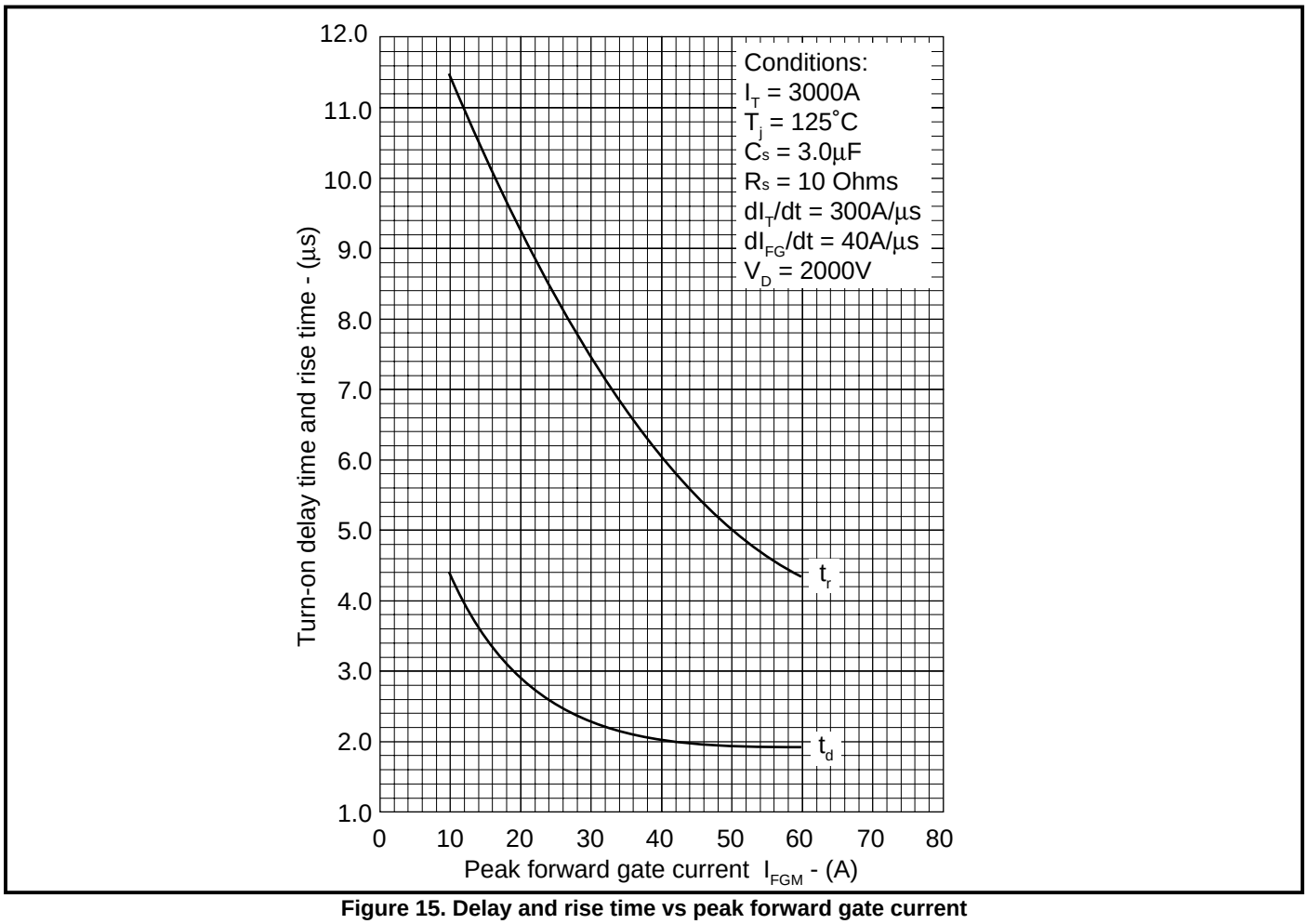


Figure 15. Delay and rise time vs peak forward gate current

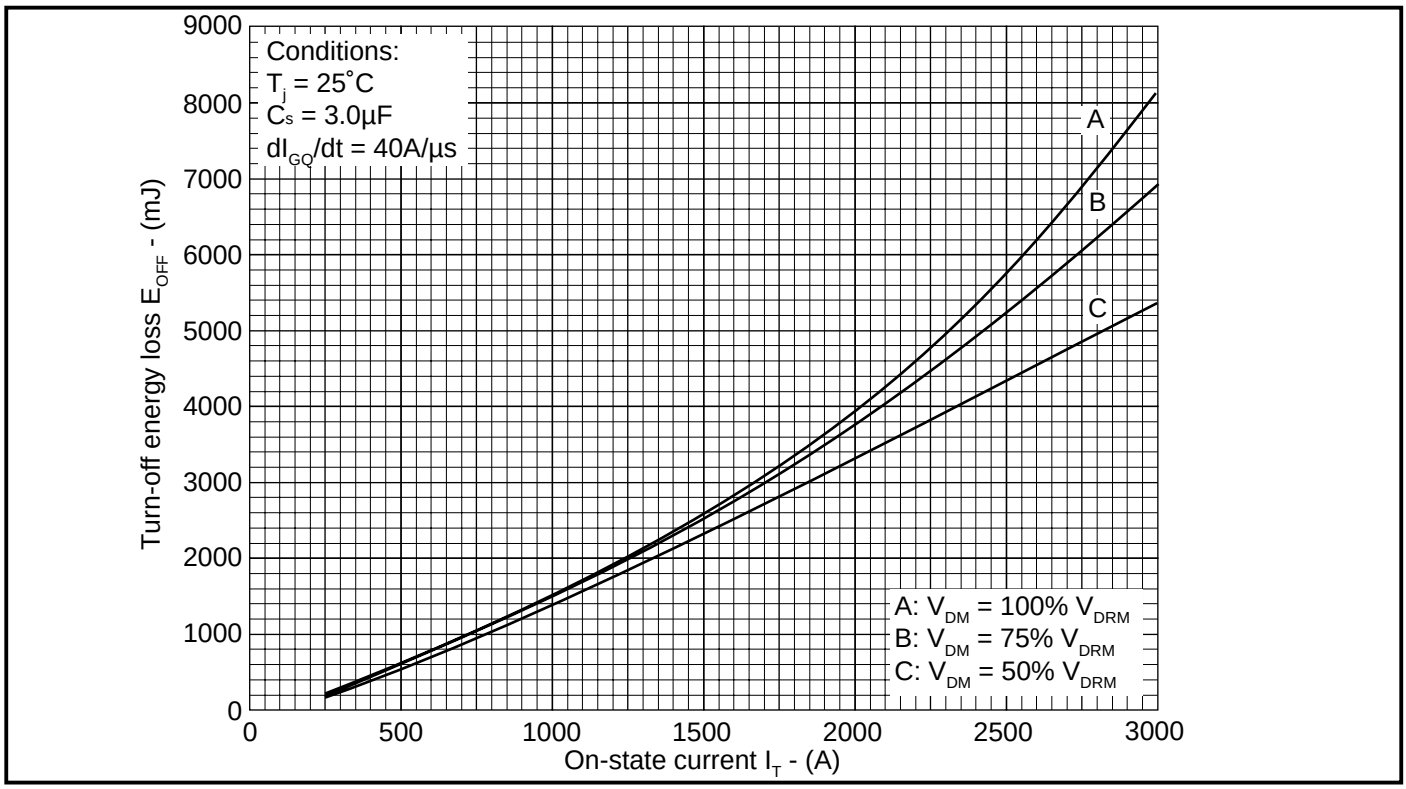


Figure 16. Turn-off energy loss vs on-state current

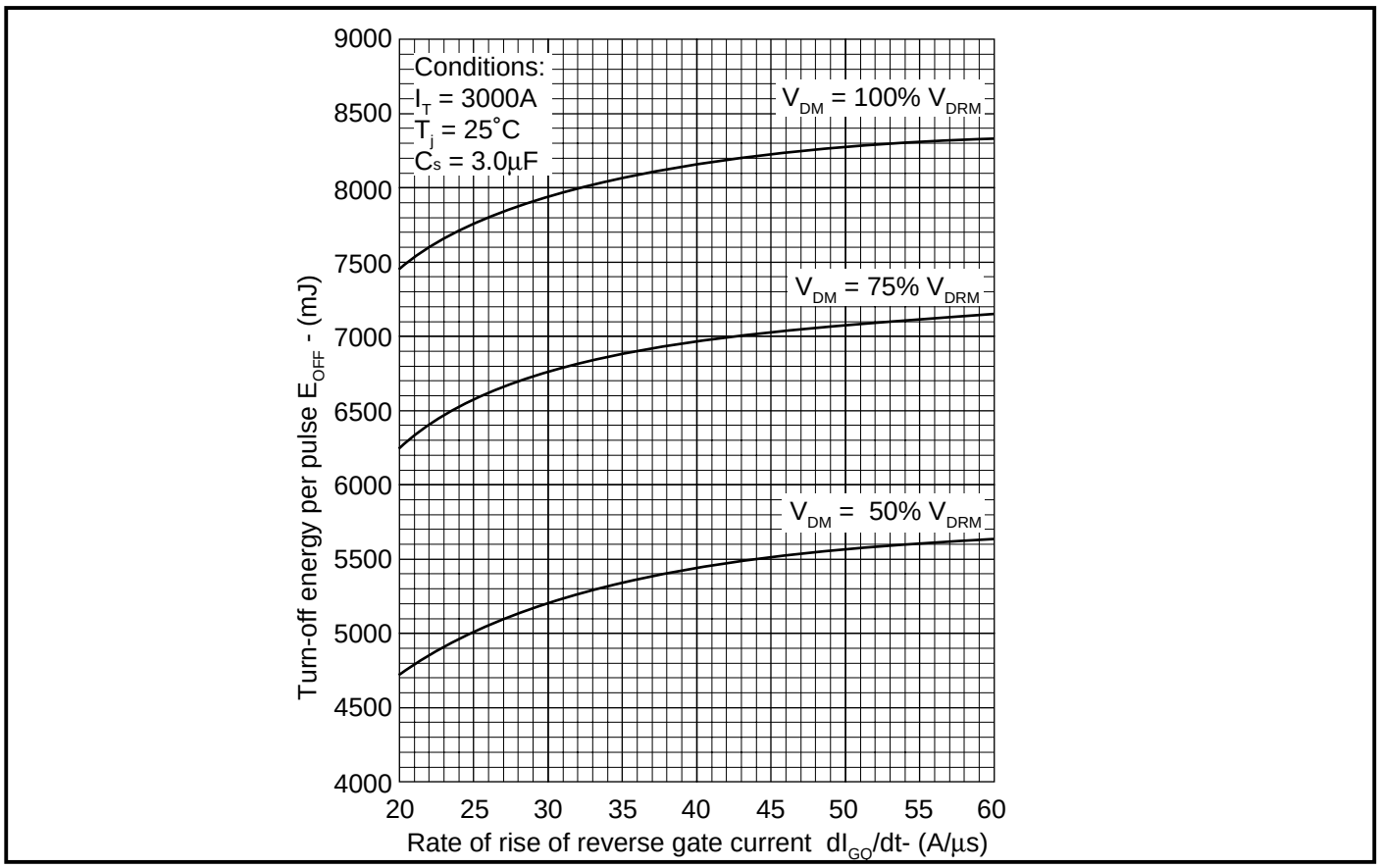


Figure 17. Turn-off energy vs rate of rise of reverse gate current

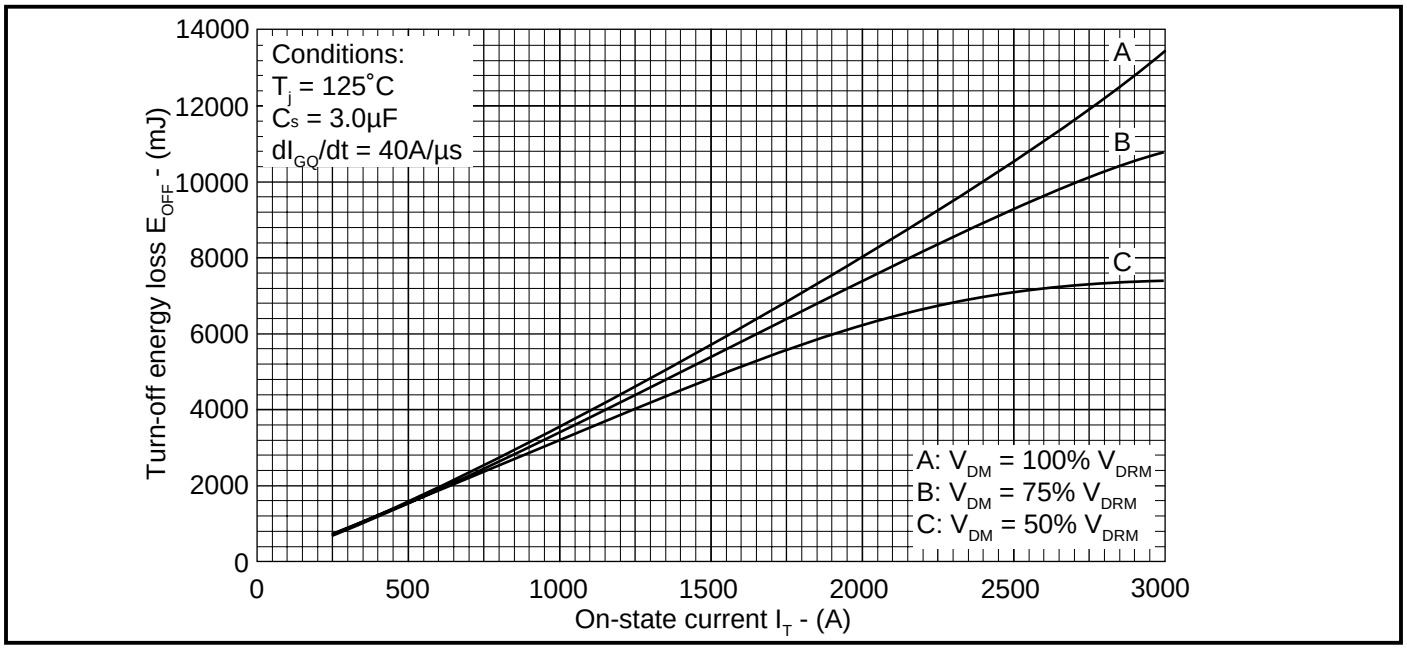


Figure 18. Turn-off energy vs on-state current

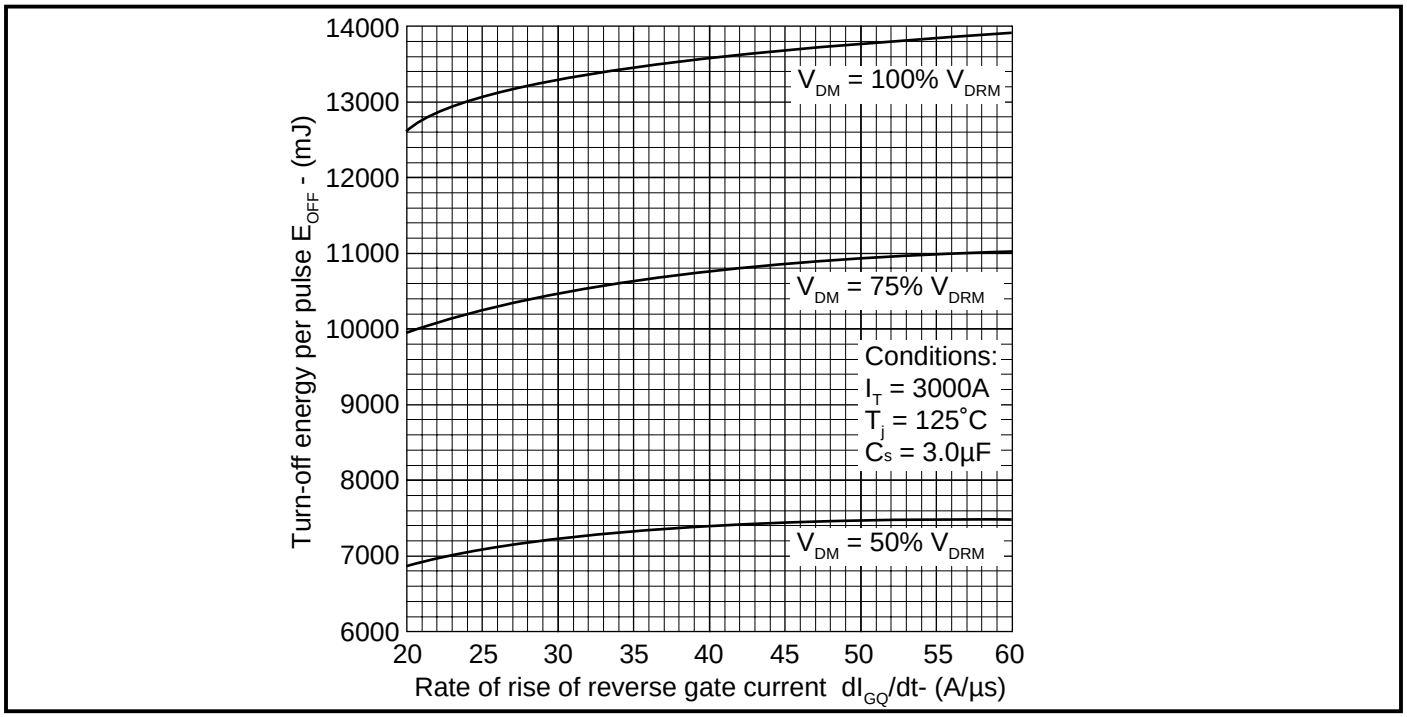


Figure 19. Turn-off energy loss vs rate of rise of reverse gate current

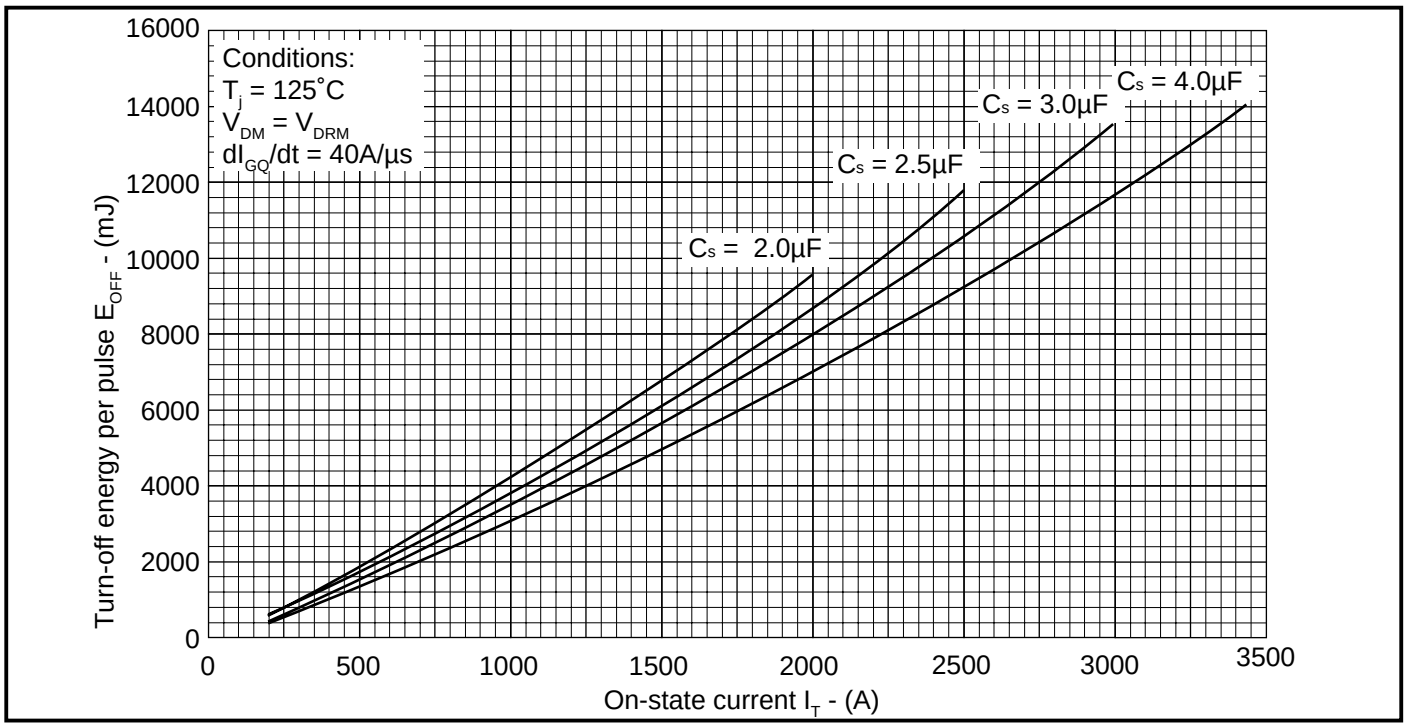


Figure 20. Turn-off energy vs on-state current

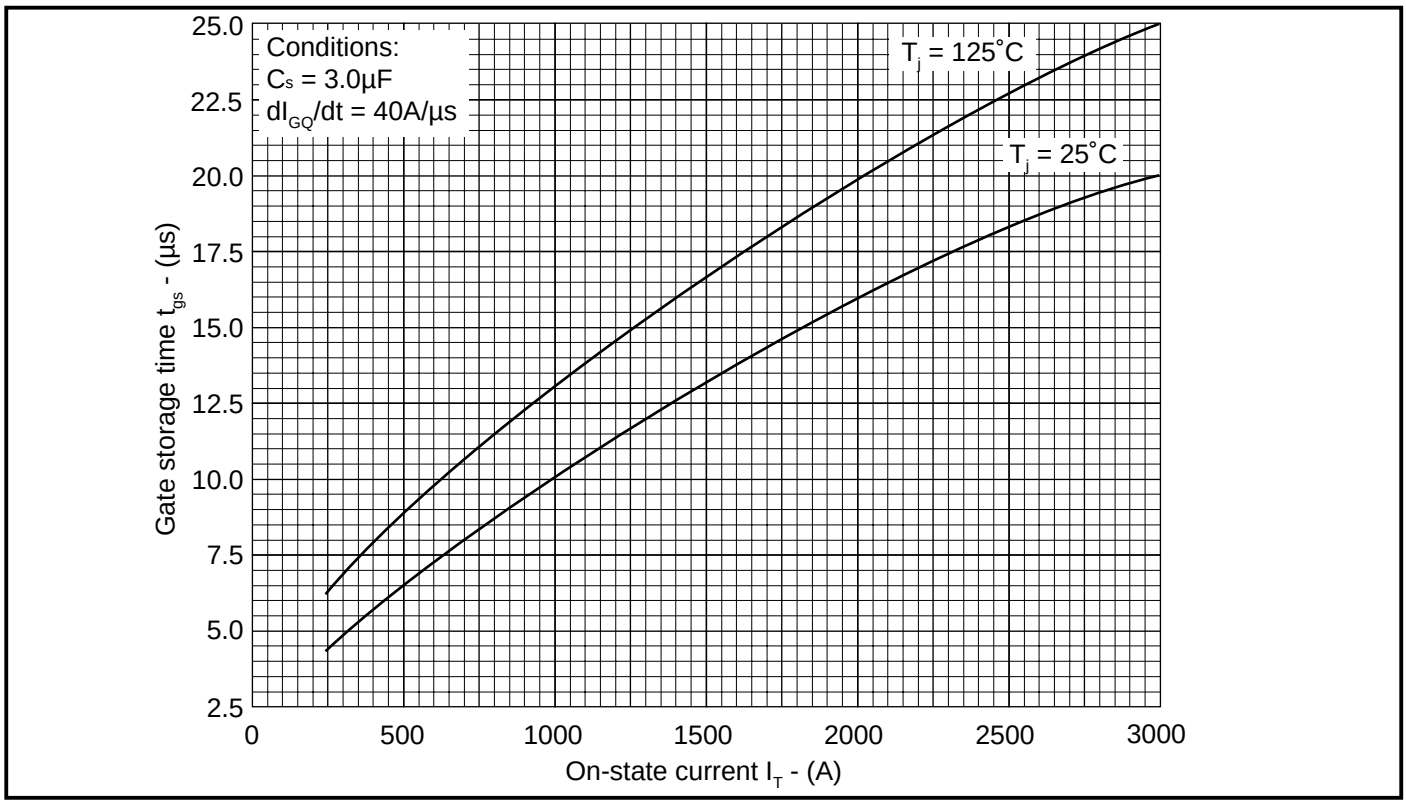


Figure 21. Gate storage time vs on-state current

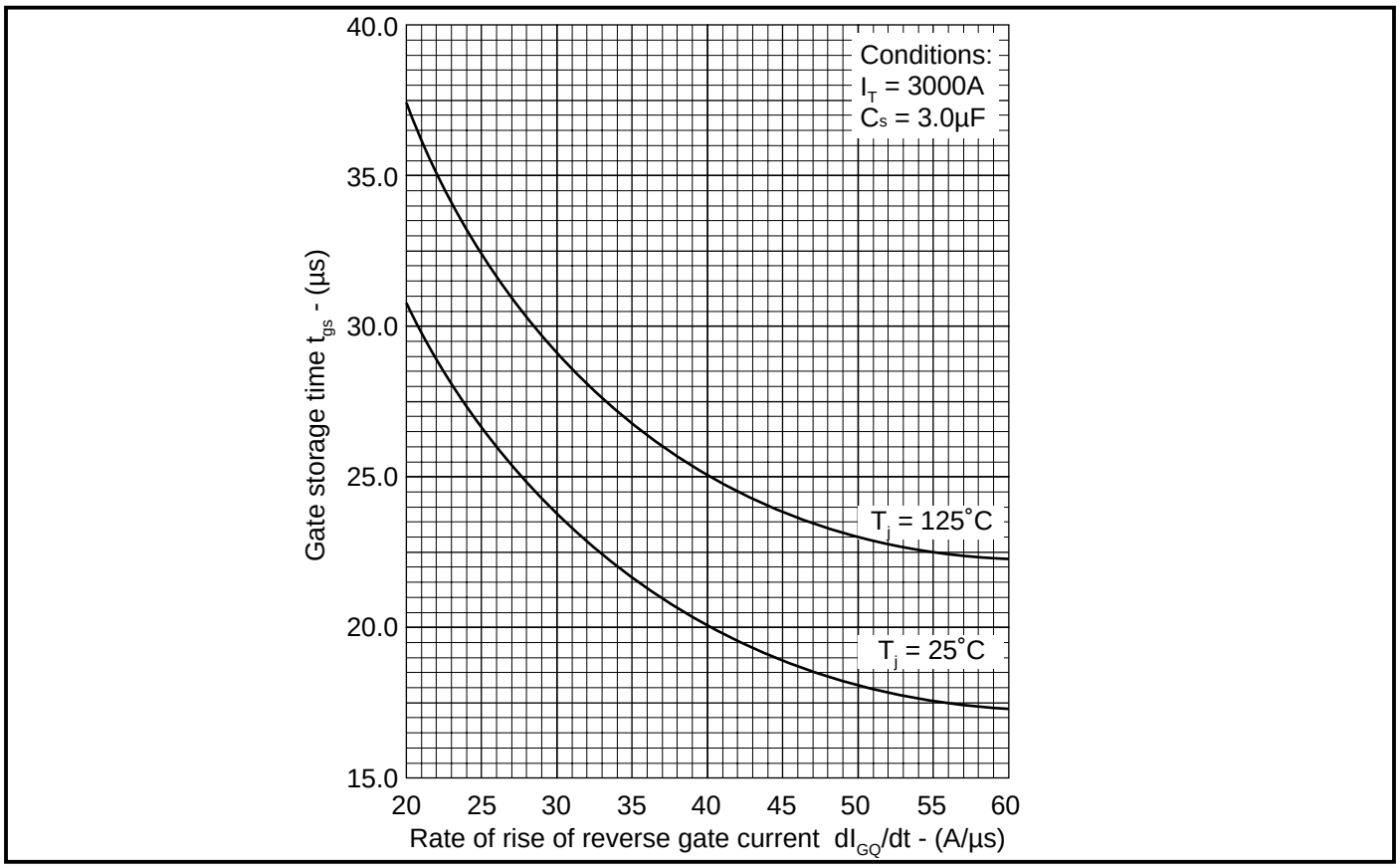


Figure 22. Gate storage time vs rate of rise of reverse gate current

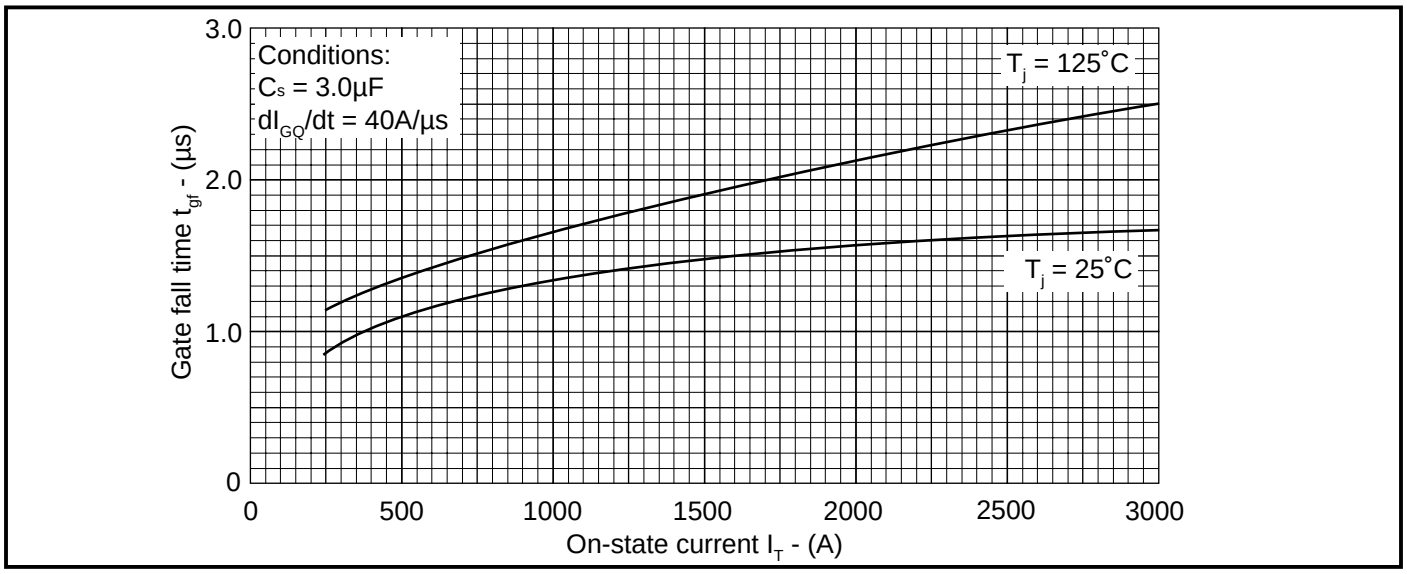


Figure 23. Gate fall time vs on-state current

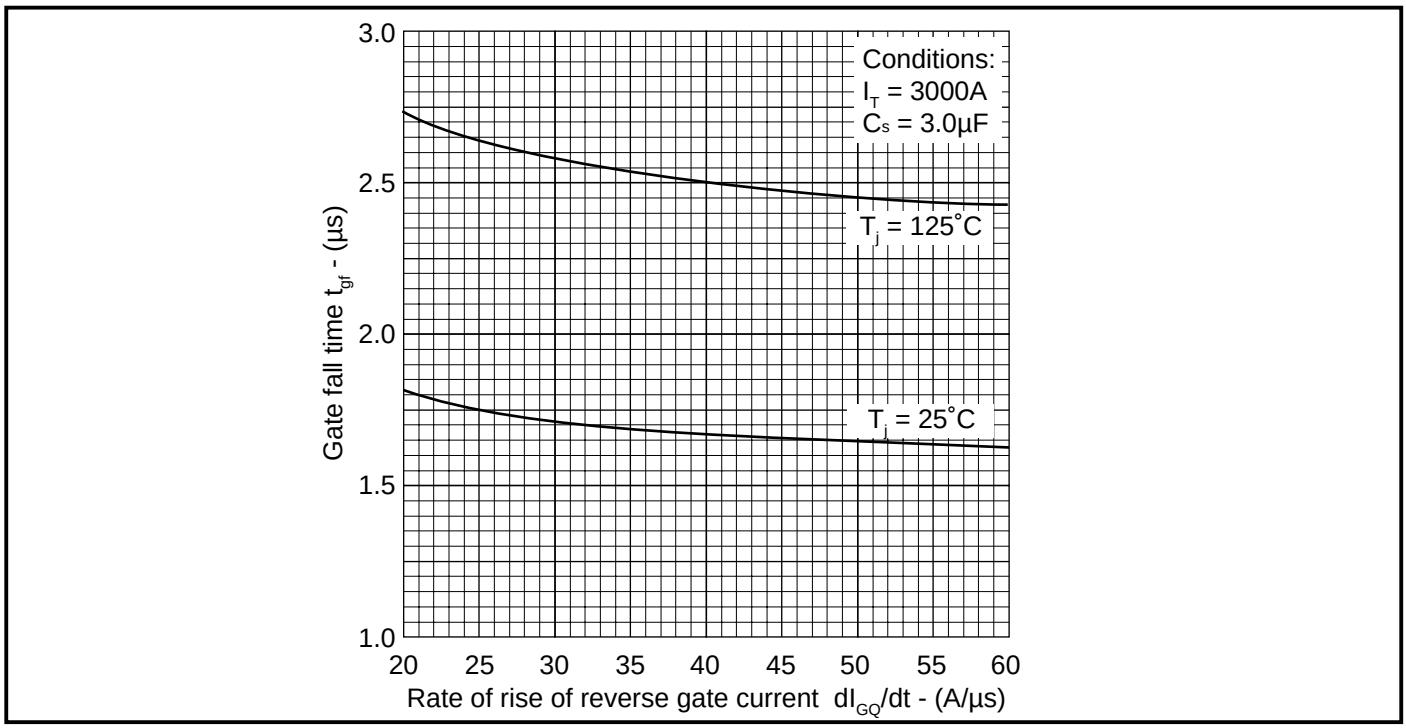


Figure 24. Gate fall time vs rate of rise of reverse gate current

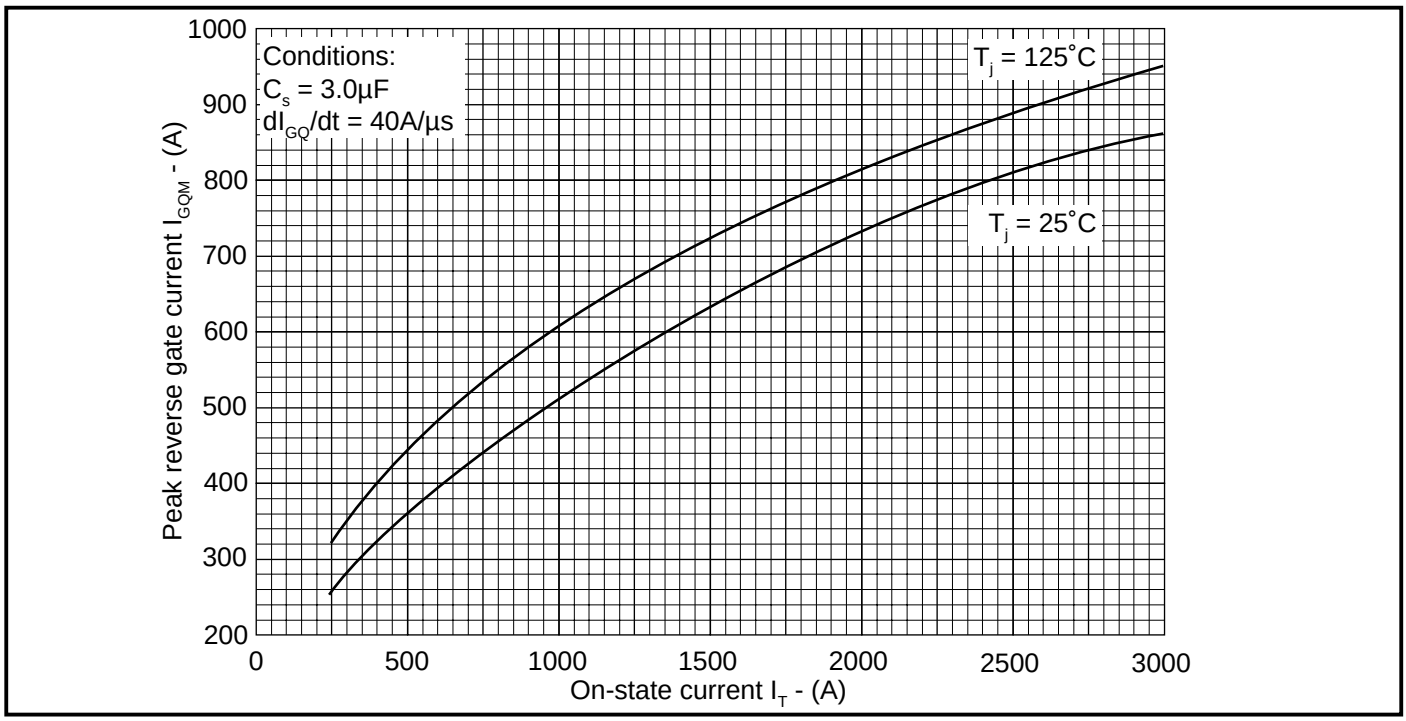


Figure 25. Peak reverse gate current vs on-state current

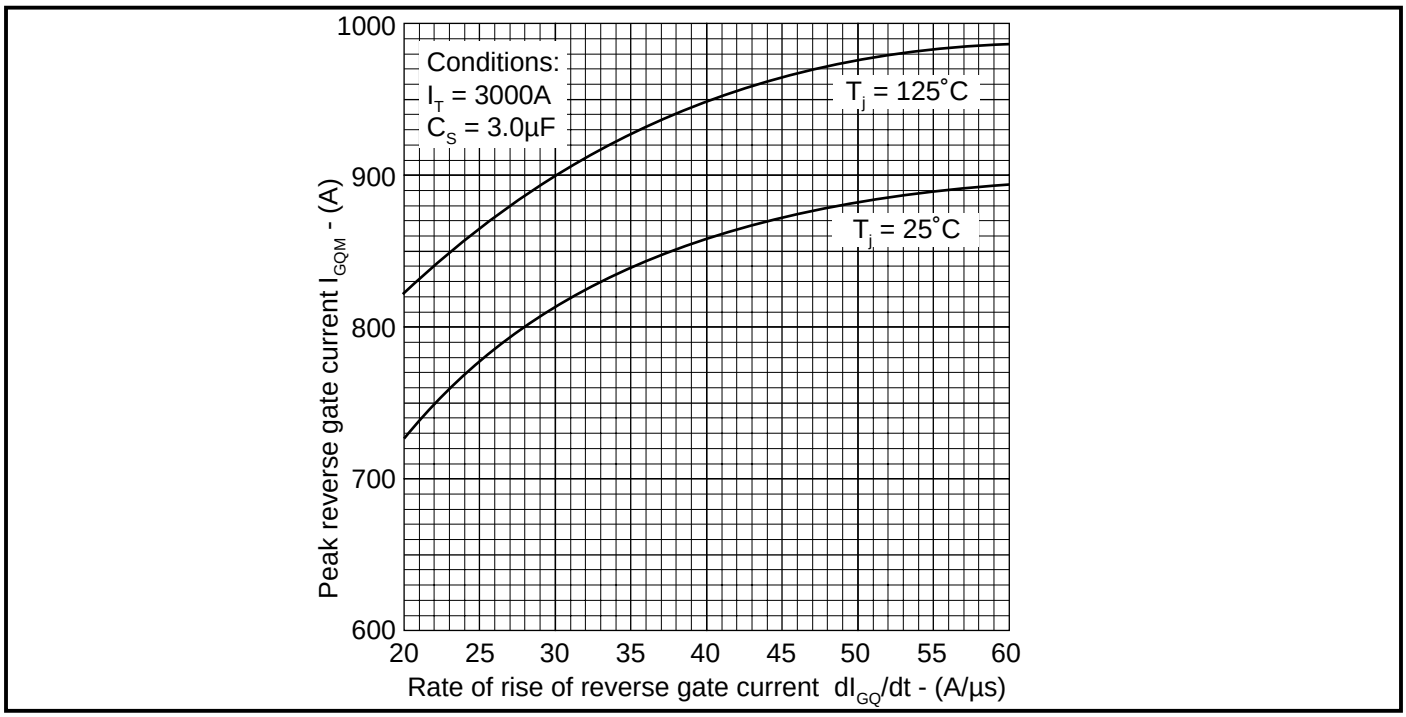


Figure 26. Reverse gate current vs rate of rise of reverse gate current

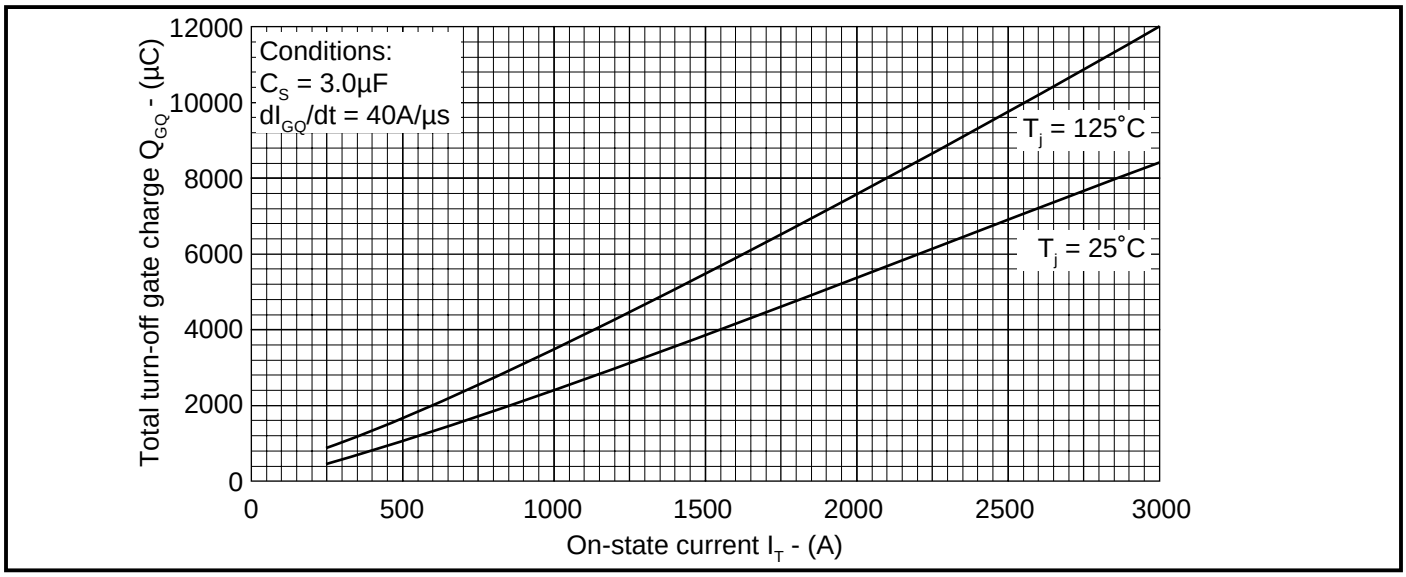


Figure 27. Turn-off gate charge vs on-state current

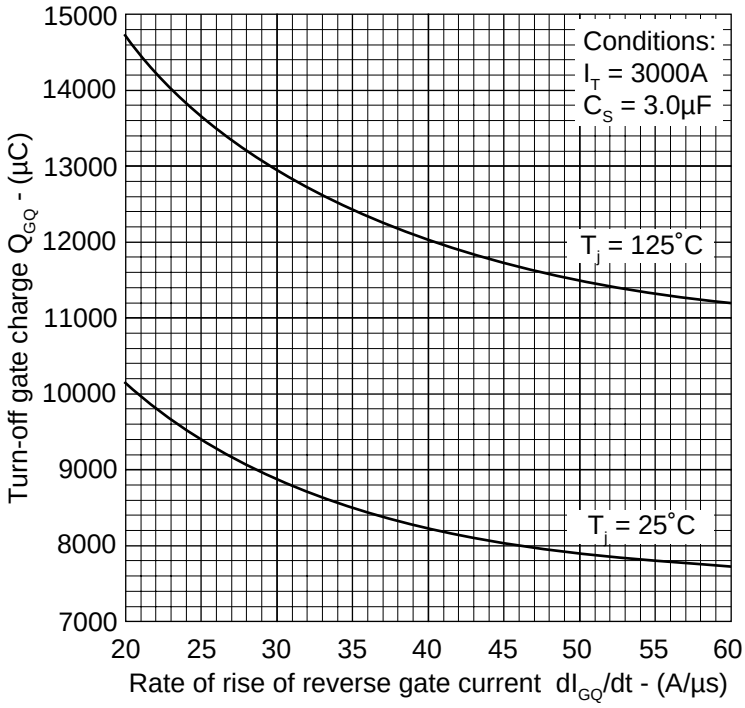


Figure 28. Turn-off gate charge vs rate of rise of reverse gate current

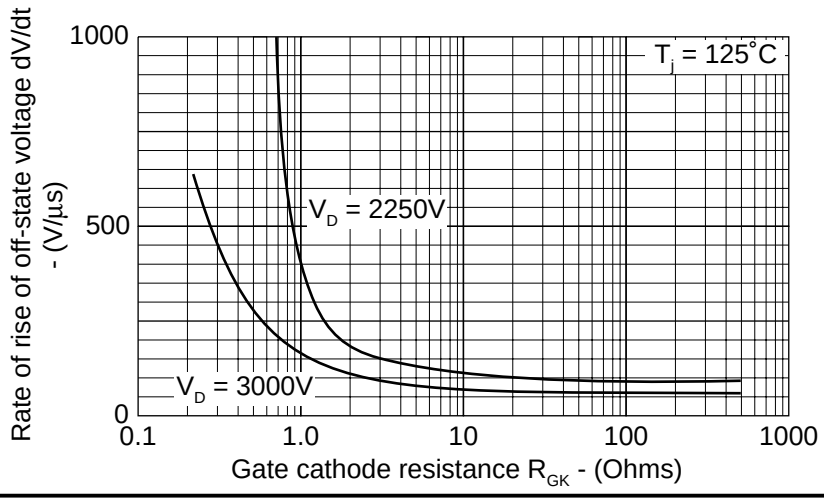
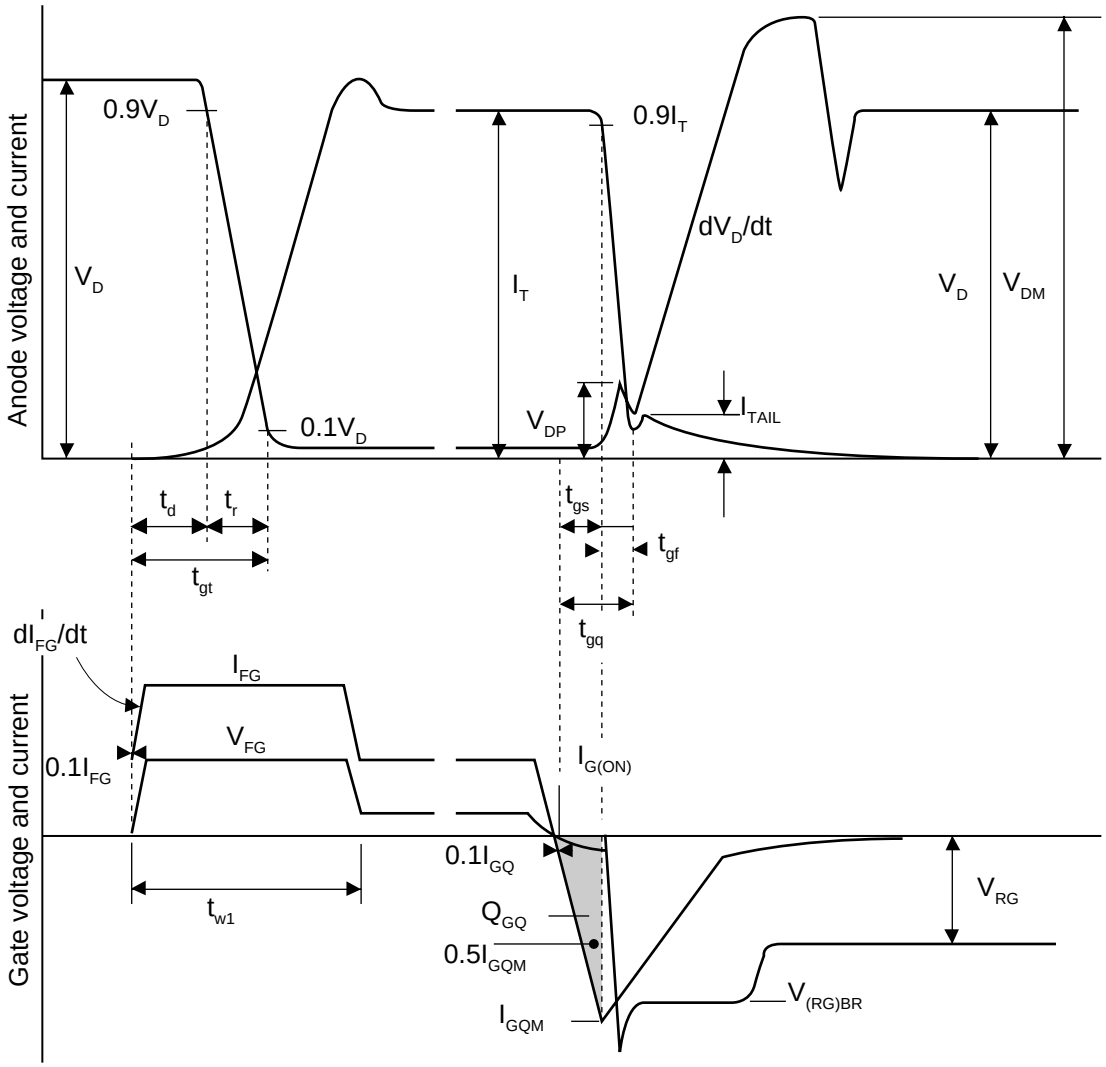


Figure 29. Rate of rise of off-state voltage vs gate cathode resistance



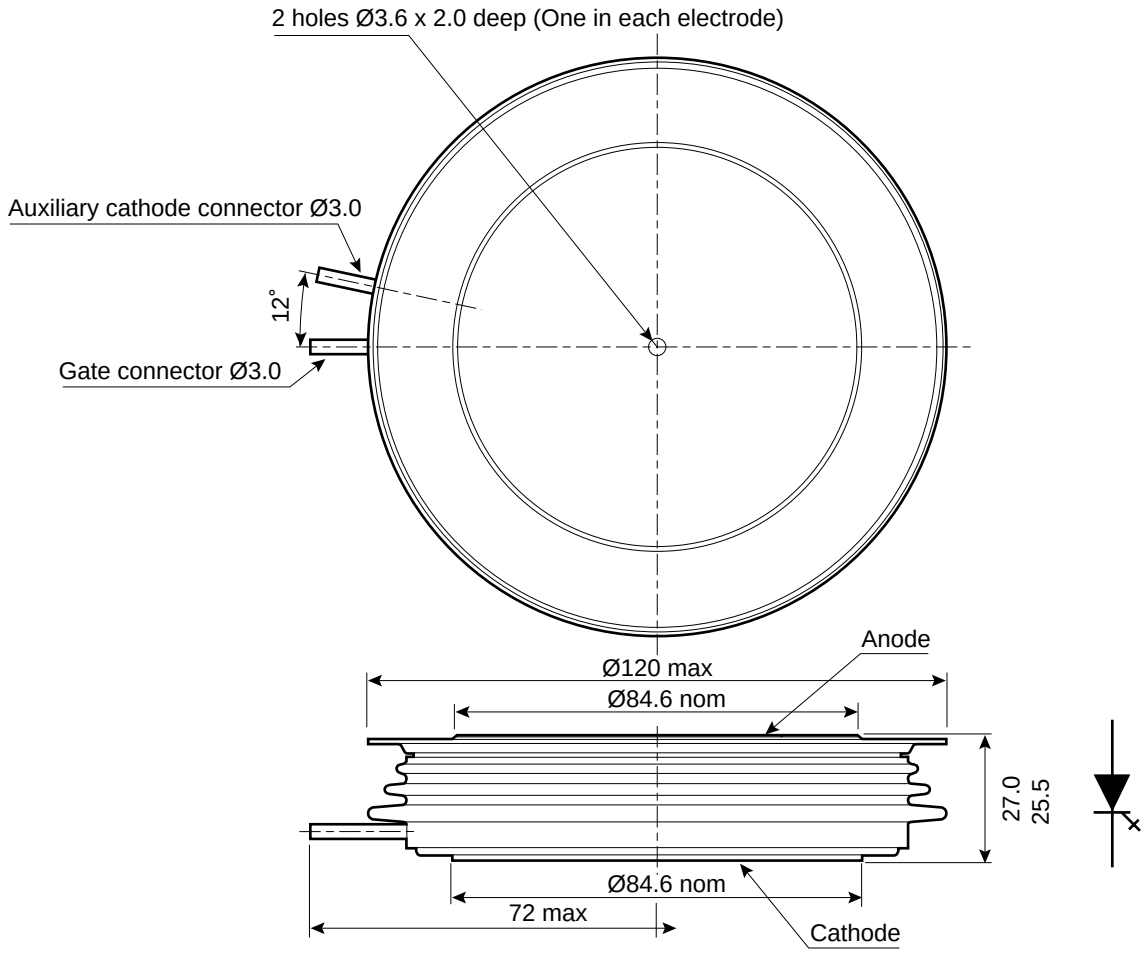
Recommended gate conditions:
I_{TCM} = 3000A
I_{FG} = 40A
$I_{G(ON)}$ = 10A d.c.
$t_{w1(min)}$ = 20µs
I_{GQM} = 950A
di_{GQ}/dt = 40A/µs
Q_{GQ} = 12000µC
$V_{RG(min)}$ = 2V
$V_{RG(max)}$ = 16V

These are recommended Dynex Semiconductor conditions. Other conditions are permitted

Figure 30. General switching waveforms

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Nominal weight: 1700g
Clamping force: 40kN ±10%
Lead length: 600mm

Package outine type code: W

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

http://www.dynexsemi.com

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