

# DCR604SE

# **Phase Control Thyristor**

Supersedes January 2000 version, DS4450-4.0

DS4450-5.0 July 2001

### **FEATURES**

- Double Side Cooling
- High Surge Capability
- High Mean Current
- Fatigue Free

### **APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- DC Motor Control

### **VOLTAGE RATINGS**

Type Number	Repetitive Peak Voltages V <sub>DRM</sub> V <sub>RRM</sub> V	Conditions
DCR604SE21	2100	$T_{v_i} = 0^{\circ} \text{ to } 125^{\circ}\text{C},$
DCR604SE20	2000	$I_{DRM}^{y} = I_{RRM} = 30 \text{mA},$
DCR604SE19	1900	$V_{DRM}$ , $V_{RRM}$ $t_p = 10ms$ ,
DCR604SE18	1800	V <sub>DSM</sub> & V <sub>RSM</sub> =
DCR604SE17	1700	$V_{DRM} \& V_{RRM} + 100V$
		respectively

Lower voltage grades available.

### **ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

#### DCR604SE20

Note: Please use the complete part number when ordering and quote this number in any future correspondance relating to your order.

#### **KEY PARAMETERS**

 $V_{DRM}$  2100V  $I_{T(AV)}$  706A  $I_{TSM}$  8100A  $dVdt^*$  1000V/ $\mu s$  dI/dt 700A/ $\mu s$ 

<sup>\*</sup>Higher dV/dt selections available

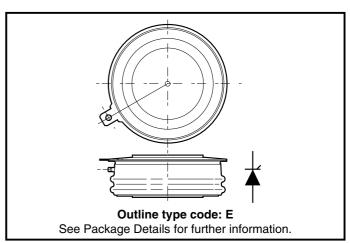


Fig. 1 Package outline



## **CURRENT RATINGS**

T<sub>case</sub> = 60°C unless stated otherwise.

Symbol	Parameter	Conditions	Max.	Units		
Double Side Cooled						
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	706	Α		
I <sub>T(RMS)</sub>	RMS value	-	1109	Α		
I <sub>T</sub>	Continuous (direct) on-state current	-	995	Α		
Single Side	e Cooled (Anode side)		ı			
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	487	Α		
I <sub>T(RMS)</sub>	RMS value	-	766	Α		
I <sub>T</sub>	Continuous (direct) on-state current	-	646	Α		

## **CURRENT RATINGS**

 $T_{case} = 80^{\circ}C$  unless stated otherwise.

Symbol	Parameter	Conditions	Max.	Units			
Double Sic	Double Side Cooled						
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	562	А			
I <sub>T(RMS)</sub>	RMS value	-	882	Α			
I <sub>T</sub>	Continuous (direct) on-state current	-	770	А			
Single Side Cooled (Anode side)							
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	380	А			
I <sub>T(RMS)</sub>	RMS value	-	595	А			
I <sub>T</sub>	Continuous (direct) on-state current	-	480	Α			



# **SURGE RATINGS**

Symbol	Parameter	Conditions	Max.	Units
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine; T <sub>case</sub> = 125°C	6.5	kA
l²t	I <sup>2</sup> t for fusing	V <sub>R</sub> = 50% V <sub>RRM</sub> - 1/4 sine	0.21 x 10 <sup>6</sup>	A²s
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine; T <sub>case</sub> = 125°C	8.1	kA
l²t	I <sup>2</sup> t for fusing	V <sub>R</sub> = 0	0.33 x 10 <sup>6</sup>	A²s

# THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	dc	-	0.041	°C/W
		Single side cooled	Anode dc	-	0.074	°C/W
			Cathode dc	-	0.092	°C/W
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 8.0kN with mounting compound	Double side	-	0.018	°C/W
			Single side	-	0.036	°C/W
$T_{v_{j}}$	Virtual junction temperature	On-state (conducting)		-	135	°C
		Reverse (blocking)		-	125	°C
T <sub>stg</sub>	Storage temperature range			-55	125	°C
-	Clamping force			7.2	8.8	kN



# **DYNAMIC CHARACTERISTICS**

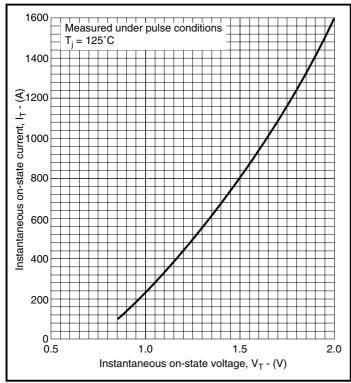
Symbol	Parameter	Conditions		Тур.	Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C		-	30	mA
dV/dt	Maximum linear rate of rise of off-state voltage	To 67% $V_{DRM}$ $T_j$ = 125°C. Gate open circuit.		-	1000	V/μs
-11 / -14		Gate source 20V, 20Ω	Repetitive 50Hz	-	350	A/μs
dl/dt	Rate of rise of on-state current		Non-repetitive	-	700	A/μs
V <sub>T(TO)</sub>	Threshold voltage	At T <sub>vj</sub> = 125°C		-	0.93	V
r <sub>T</sub>	On-state slope resistance	At T <sub>vj</sub> = 125°C		-	0.667	mΩ
t <sub>gd</sub>	Delay time	$V_D = 67\% V_{DRM}$ , Gate source 10V, 5Ω $t_r = 0.5\mu s$ , $T_j = 25$ °C		-	1.5	μs
I <sub>L</sub>	Latching current	$T_{j} = 25^{\circ}C, V_{D} = 5V$		-	500	mA
I <sub>H</sub>	Holding current	$T_{j} = 25^{\circ}C, V_{D} = 5V$		-	70	mA
t <sub>q</sub>	Turn-off time	$I_T = 500A$ , $t_p = 1ms$ , $T_j = 125^{\circ}C$ , $V_R = 50V$ , $dI_{RR}/dt = 20A/\mu s$ , $V_{DR} = 67\%$ $V_{DRM}$ , $dV_{DR}/dt = 20V/\mu s$ linear		300	400	μs

# **GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	3.0	٧
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	150	mA
$V_{\sf GD}$	Gate non-trigger voltage	At 67% V <sub>DRM</sub> T <sub>case</sub> = 125°C	0.25	٧
$V_{FGM}$	Peak forward gate voltage	Anode positive with respect to cathode	30	V
$V_{FGN}$	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
V <sub>RGM</sub>	Peak reverse gate voltage		5	٧
I <sub>FGM</sub>	Peak forward gate current	Anode positive with respect to cathode	10	Α
$P_{GM}$	Peak gate power	See table, gate characteristics curve	100	W
$P_{G(AV)}$	Mean gate power		5	W



## **CURVES**



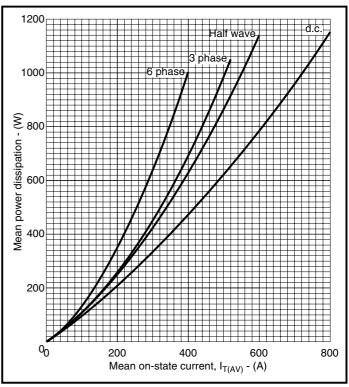


Fig.2 Maximum (limit) on-state characteristics

Fig.3 Dissipation curves

 $V_{\rm TM}$  Equation:-

 $V_{TM} = A + Bln (I_T) + C.I_T + D.\sqrt{I_T}$ 

Where A = 1.086551

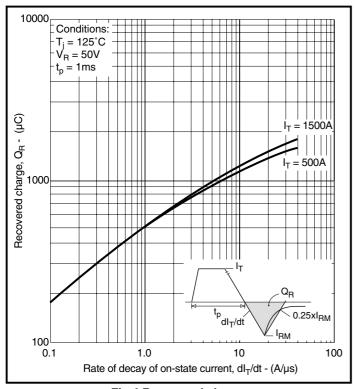
B = -0.173031

 $C = -3.307461 \times 10^{-5}$ 

D = 0.056345

these values are valid for  $T_j = 125^{\circ}C$  for  $I_T 500A$  to 1600A





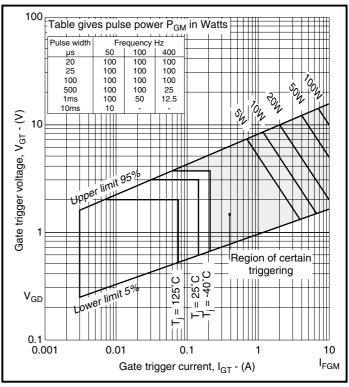
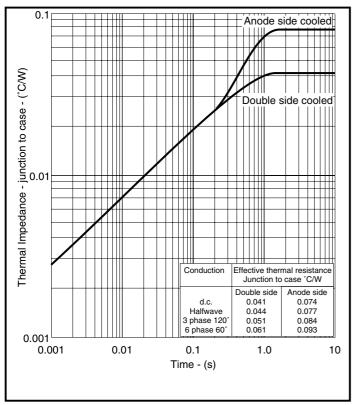
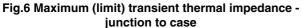


Fig.4 Recovered charge

Fig.5 Gate characteristics





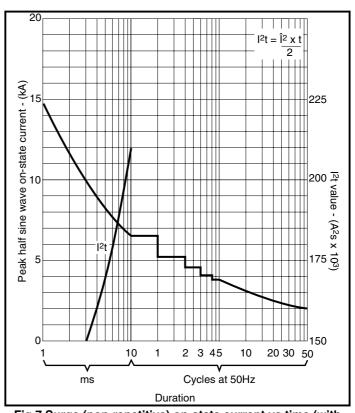
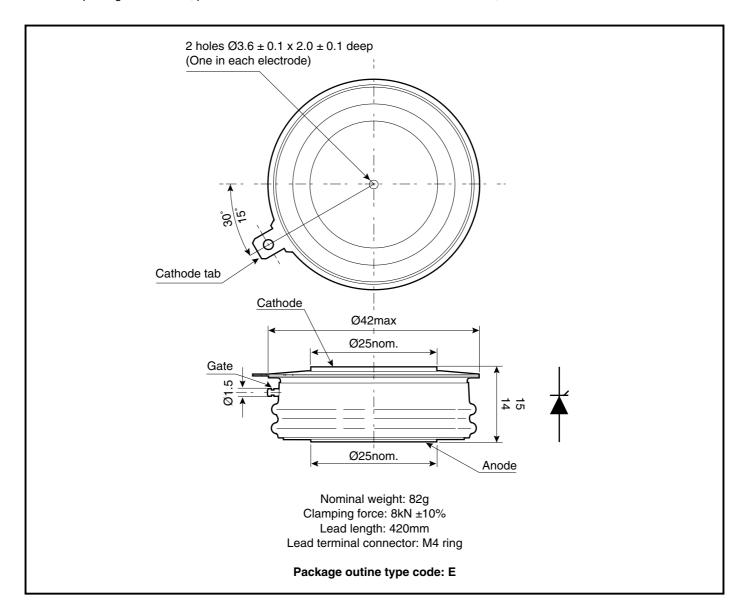


Fig.7 Surge (non-repetitive) on-state current vs time (with 50%  $\rm V_{RRM}$  at  $\rm T_{case}\,125^{\circ}C)$ 



### **PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



#### POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

#### **HEATSINKS**

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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