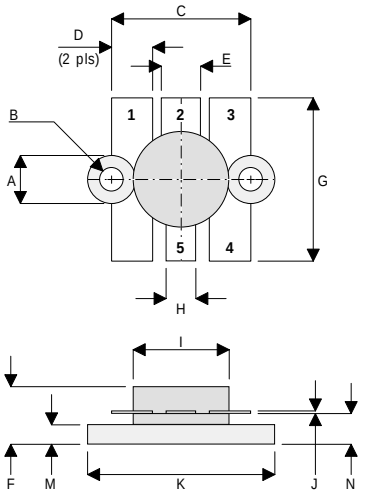
D1004UK

ROHS COMPLIANT METAL GATE RF SILICON FET

MECHANICAL DATA



DT

PIN 1 SOURCE (COMMON) PIN 2 GATE

PIN 3 SOURCE (COMMON) PIN 4 SOURCE (COMMON)

PIN 5 DRAIN

DIM	mm	Tol.	Inches	Tol.
A	6.35 DIA	0.13	0.250 DIA	0.005
B	3.17 DIA	0.13	0.125 DIA	0.005
C	18.41	0.25	0.725	0.010
D	5.46	0.13	0.215	0.005
E	5.21	0.13	0.205	0.005
F	7.62	MAX	0.300	MAX
G	21.59	0.38	0.850	0.015
H	3.94	0.13	0.155	0.005
I	12.70	0.13	0.500	0.005
J	0.13	0.03	0.005	0.001
K	24.76	0.13	0.975	0.005
M	2.59	0.13	0.102	0.005
N	4.06	0.25	0.160	0.010

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 80W – 28V – 175MHz SINGLE ENDED

FEATURES

- **SIMPLIFIED AMPLIFIER DESIGN**
- **SUITABLE FOR BROAD BAND APPLICATIONS**
- **LOW C_{rss}**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN – 16 dB MINIMUM**

APPLICATIONS

- HF/VHF COMMUNICATIONS from 1 MHz to 175 MHz

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

P_D	Power Dissipation	175W
BV_{DSS}	Drain – Source Breakdown Voltage	70V
BV_{GSS}	Gate – Source Breakdown Voltage	±20V
$I_{D(sat)}$	Drain Current	20A
T_{stg}	Storage Temperature	–65 to 150°C
T_j	Maximum Operating Junction Temperature	200°C

Semelab Plc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.

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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0	I_D = 100mA	70			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 28V	V_{GS} = 0			4	mA
I_{GSS}	Gate Leakage Current	V_{GS} = 20V	V_{DS} = 0			1	µA
$V_{GS(th)}$	Gate Threshold Voltage *	I_D = 10mA	V_{DS} = V_{GS}	1		7	V
g_{fs}	Forward Transconductance *	V_{DS} = 10V	I_D = 4A	3.2			S
G_{PS}	Common Source Power Gain	P_O = 80W		16			dB
η	Drain Efficiency	V_{DS} = 28V	I_{DQ} = 0.4A	50			%
VSWR	Load Mismatch Tolerance	f = 175MHz		20:1			—
C_{iss}	Input Capacitance	V_{DS} = 28V	V_{GS} = –5V f = 1MHz			240	pF
C_{oss}	Output Capacitance	V_{DS} = 28V	V_{GS} = 0 f = 1MHz			120	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 28V	V_{GS} = 0 f = 1MHz			10	pF

* Pulse Test: Pulse Duration = 300 µs , Duty Cycle ≤ 2%

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

$R_{THj–case}$	Thermal Resistance Junction – Case	Max. 1.0°C / W

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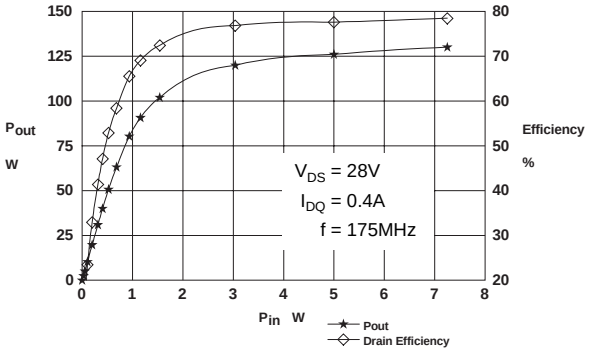

Figure 1 – Power Output and Efficiency vs. Power Input.

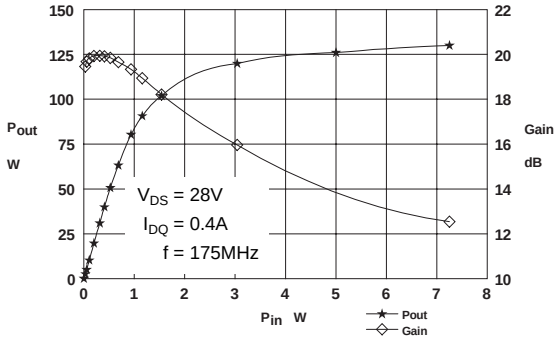

Figure 2 – Power Output & Gain vs. Power Input.

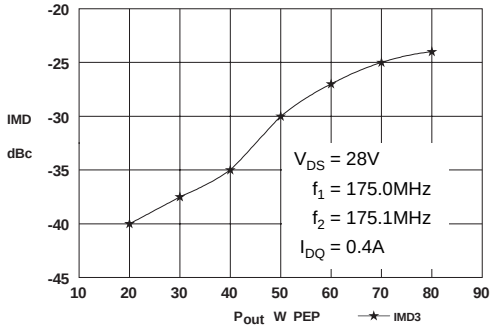

Figure 3 – IMD vs. Output Power.

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OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
175MHz	2.2 + j1.9	3.2 - j0.5

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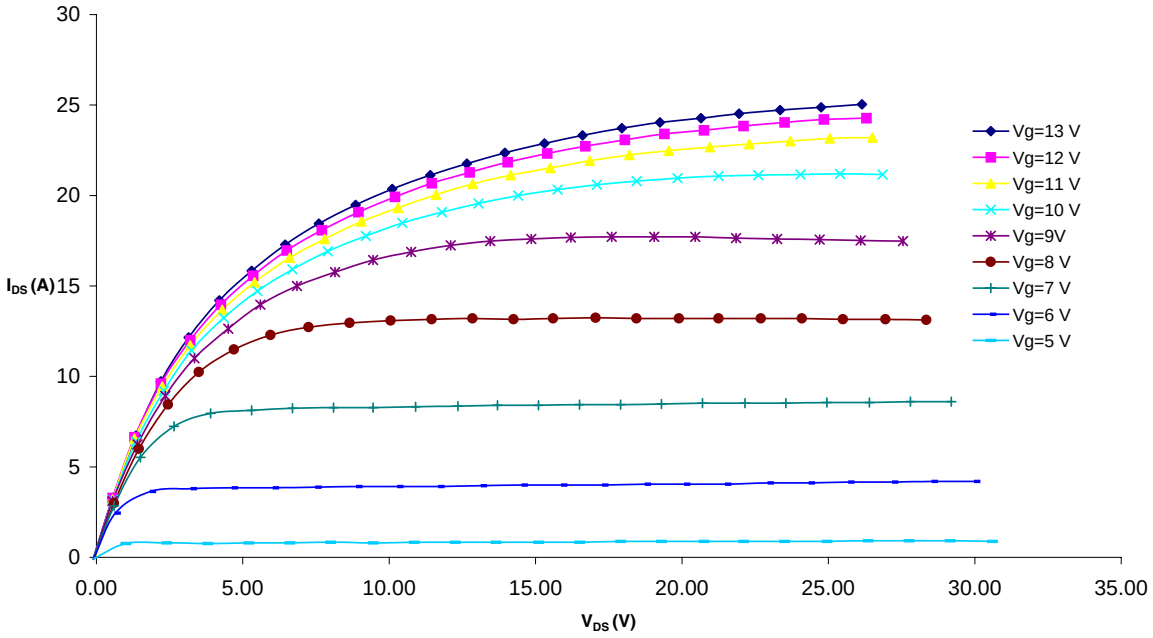

Figure 4 – Typical IV Characteristics.

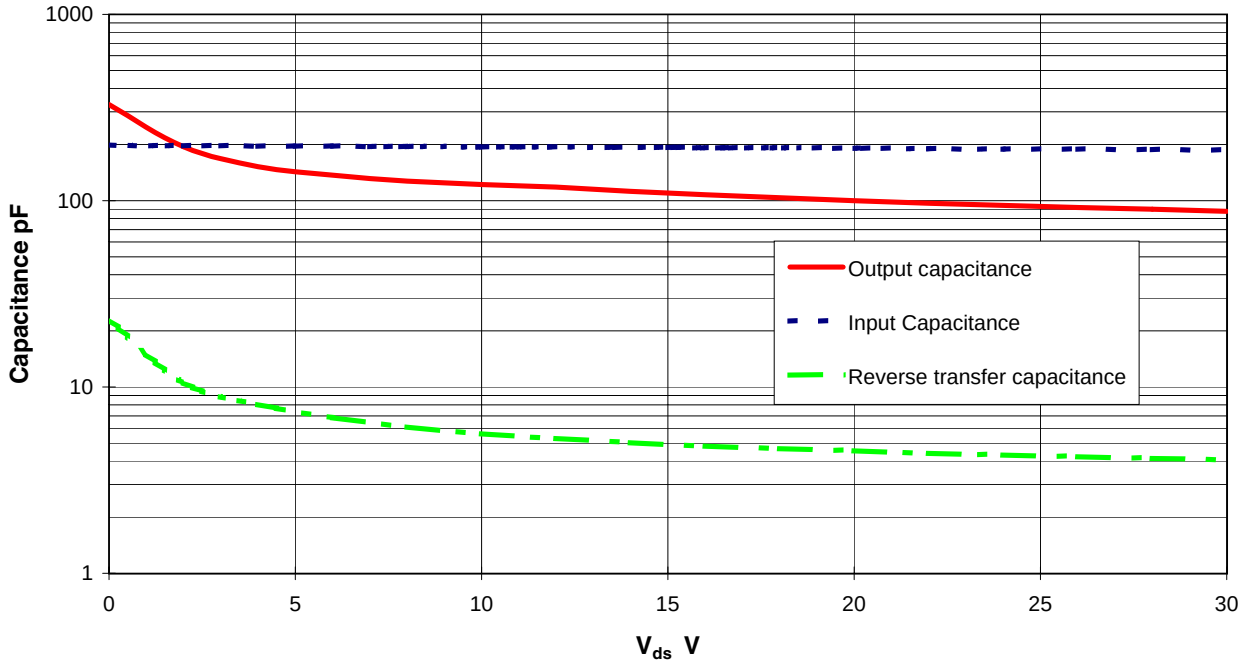

Figure 5 – Typical CV Characteristics.

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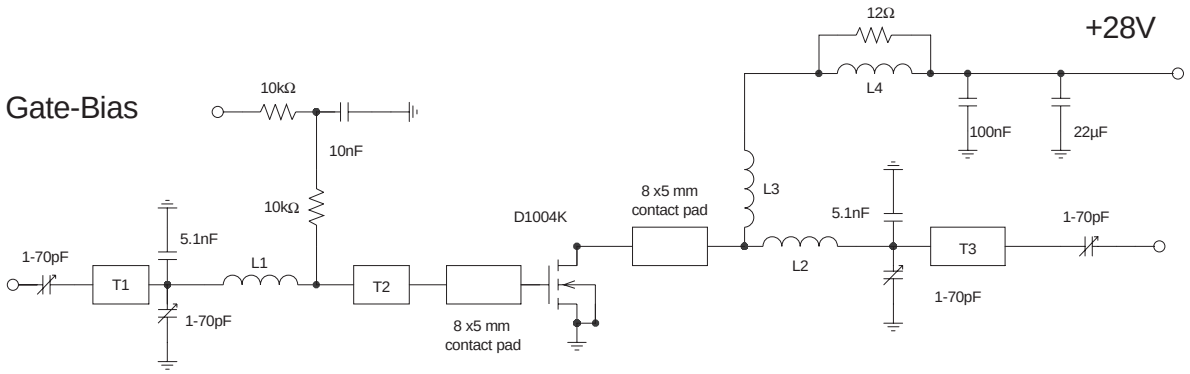

D1004UK 175MHz TEST FIXTURE

Substrate 1.6mm PTFE/ glass, Er= 2.5
All microstrip lines W=4.4mm

T1	7.5mm
T2	6mm
T3	8mm

L1	Hairpin loop 16swg 13mm dia
L2	Hairpin loop 16swg 11mm dia
L3	10 turns 18swg enamelled copper wire, 4mm i.d.
L4	12 turns 18swg enamelled copper wire on 22.7mm o.d. ferrite core

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