Freescale Semiconductor
Technical Data

Document Number: MRF8S21172H
Rev. 1, 3/2012

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF8S21172HR3
MRF8S21172HSR3

2110-2170 MHz, 42 W AVG., 28 V
W-CDMA, LTE
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for W-CDMA and LTE base station applications with frequencies from 2110 to 2170 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

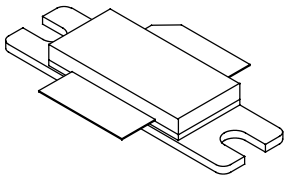
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1350 mA, P_{out} = 42 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	17.3	31.6	5.9	-35.8
2140 MHz	17.4	31.0	6.0	-35.9
2170 MHz	17.5	30.6	5.9	-35.0

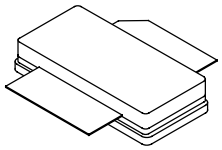
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 2140 MHz, 193 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out})
- Typical P_{out} @ 1 dB Compression Point ≃ 132 Watts CW

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- In Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13 inch Reel. For R5 Tape and Reel option, see p. 13.



CASE 465-06, STYLE 1
NI-780
MRF8S21172HR3



CASE 465A-06, STYLE 1
NI-780S
MRF8S21172HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	196 0.98	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 71°C, 42 W CW, 28 Vdc, I_{DQ} = 1350 mA, 2170 MHz Case Temperature 84°C, 160 W CW(4), 28 Vdc, I_{DQ} = 1350 mA, 2170 MHz	$R_{\theta JC}$	 0.41 0.41	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 258 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 1350 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (1) (V_{DD} = 28 Vdc, I_D = 1350 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.5	5.4	6.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	$V_{DS(on)}$	0.1	0.24	0.3	Vdc

Functional Tests (2) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1350 mA, P_{out} = 42 W Avg., f = 2170 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Power Gain	G_{ps}	16.5	17.5	19.5	dB
Drain Efficiency	η_D	29.2	30.6	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.6	5.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	-35.0	-33.2	dBc
Input Return Loss	IRL	—	-13	-8	dB

Typical Broadband Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1350 mA, P_{out} = 42 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	17.3	31.6	5.9	-35.8	-14
2140 MHz	17.4	31.0	6.0	-35.9	-14
2170 MHz	17.5	30.6	5.9	-35.0	-13

1. V_{GG} = 2 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
2. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1350 mA, 2110–2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	132	—	W
IMD Symmetry @ 104 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	20	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	58	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 42 W Avg.	G_F	—	0.25	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.017	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.003	—	dB/°C

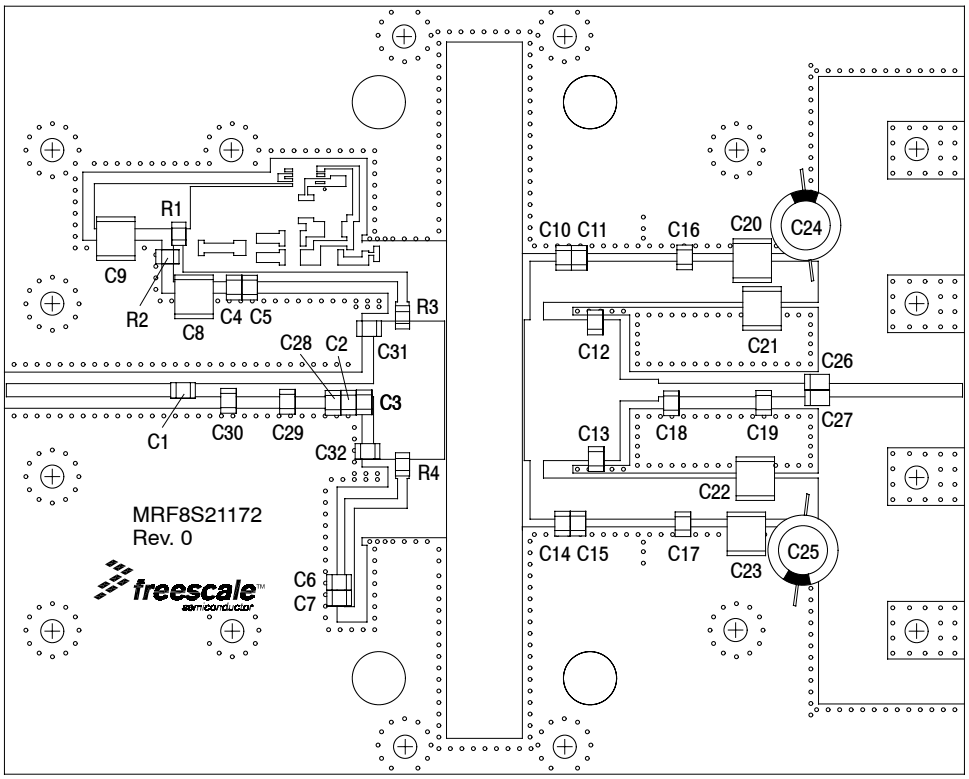


Figure 1. MRF8S21172HR3(HSR3) Test Circuit Component Layout

Table 5. MRF8S21172HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C5, C7, C11, C15, C16, C17, C26, C27	68 pF Chip Capacitors	ATC800B680JT500XT	ATC
C2	1.3 pF Chip Capacitor	ATC800B1R3BT500XT	ATC
C3	1.5 pF Chip Capacitor	ATC800B1R5BT500XT	ATC
C4, C6, C10, C12, C13, C14	0.8 pF Chip Capacitors	ATC800B0R8BT500XT	ATC
C8, C9, C20, C21, C22, C23	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C18, C19	1.1 pF Chip Capacitors	ATC800B1R1BT500XT	ATC
C24, C25	330 μF, 63 V Electrolytic Capacitors	MCRH63V337M13X21-RH	Multicomp
C28, C29	0.9 pF Chip Capacitors	ATC800B0R9BT500XT	ATC
C30	0.6 pF Chip Capacitor	ATC800B0R6BT500XT	ATC
C31, C32	0.5 pF Chip Capacitors	ATC800B0R5BT500XT	ATC
R1, R2	2 kΩ, 1/4 W Chip Resistors	CRCW12062K00FKEA	Vishay
R3, R4	2.37 Ω, 1/4 W Chip Resistors	CRCW12062R37FNEA	Vishay
PCB	0.030″, ε_r = 3.55	RF-35A2	Taconic

TYPICAL CHARACTERISTICS

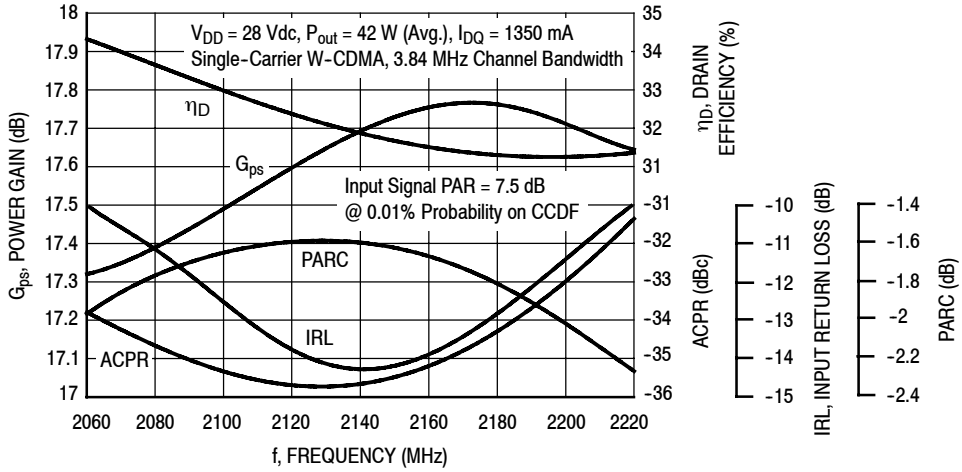


Figure 2. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 42 Watts Avg.

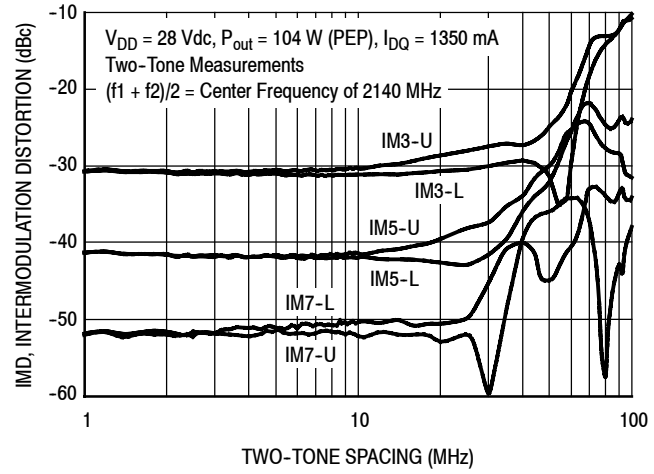


Figure 3. Intermodulation Distortion Products versus Two-Tone Spacing

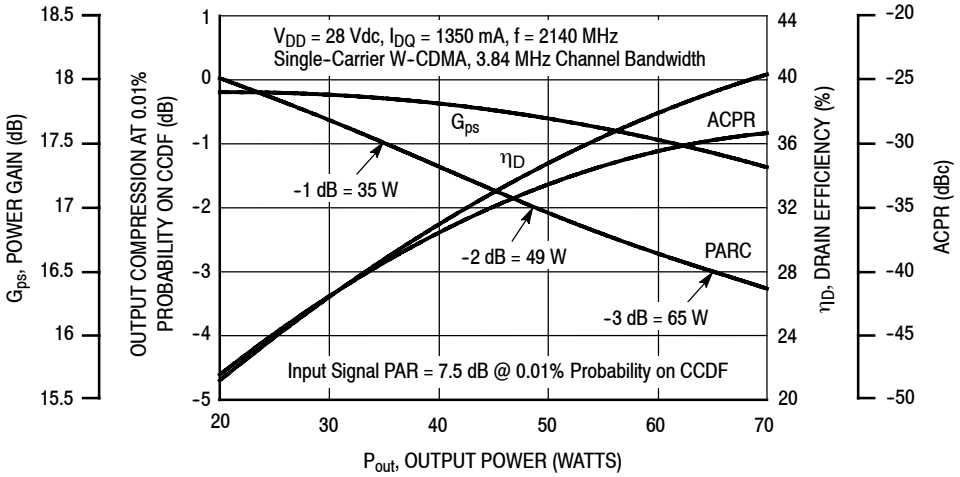


Figure 4. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

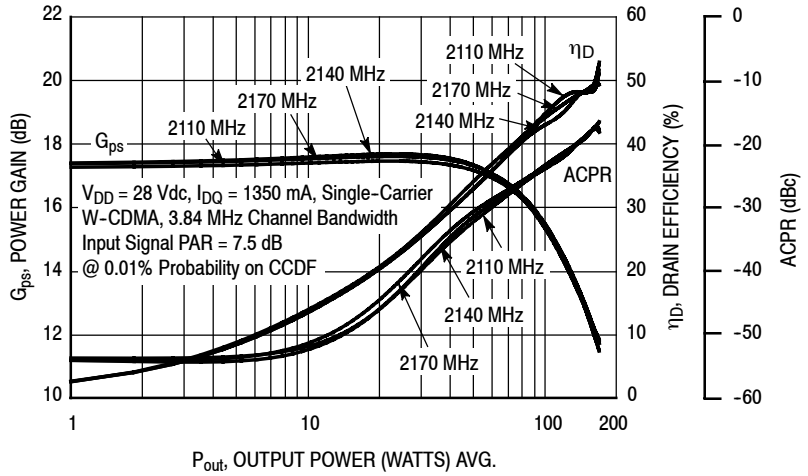


Figure 5. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

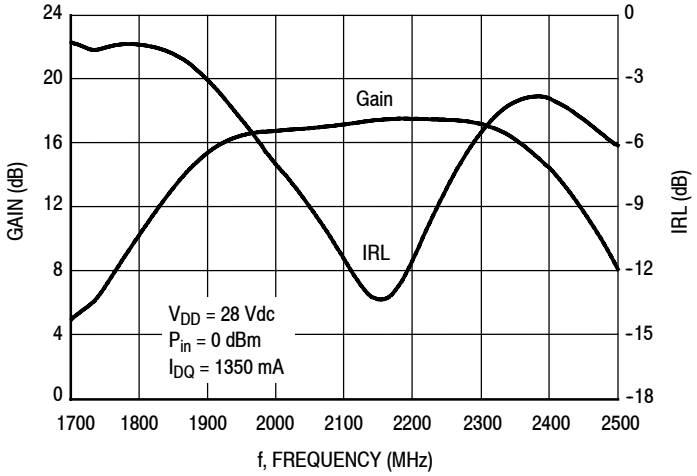


Figure 6. Broadband Frequency Response

W-CDMA TEST SIGNAL

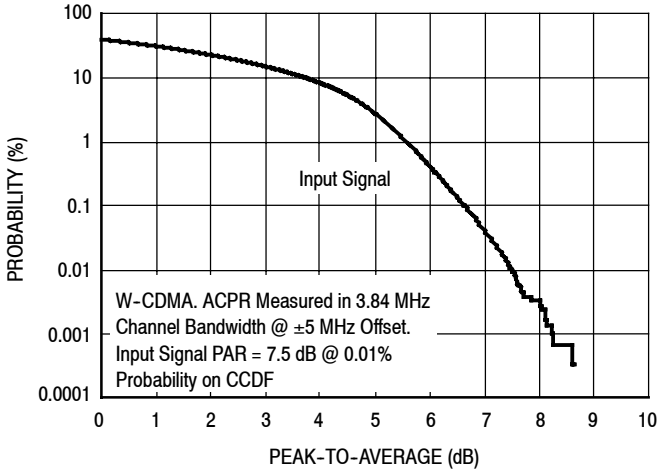


Figure 7. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

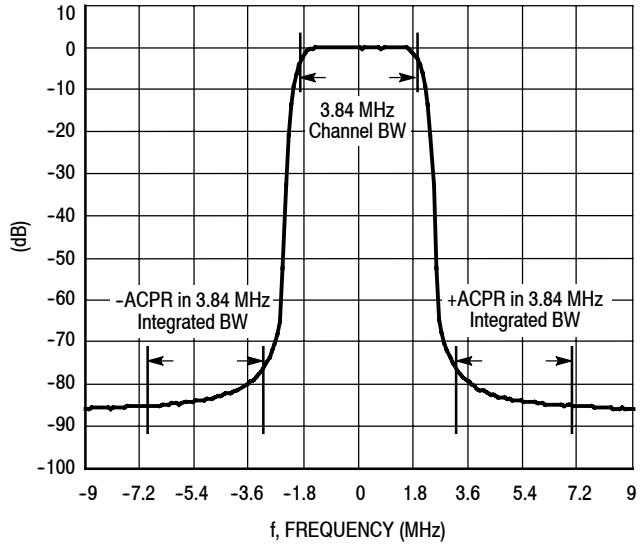


Figure 8. Single-Carrier W-CDMA Spectrum

V_{DD} = 28 Vdc, I_{DQ} = 1350 mA, P_{out} = 42 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
2060	7.06 – j2.80	0.74 – j2.83
2080	6.94 – j2.81	0.84 – j3.41
2100	6.79 – j2.83	0.96 – j4.04
2120	6.65 – j2.84	1.08 – j4.72
2140	6.50 – j2.84	1.23 – j5.42
2160	6.35 – j2.86	1.44 – j6.17
2180	6.19 – j2.88	1.73 – j6.99
2200	6.02 – j2.90	2.13 – j7.91
2220	5.84 – j2.92	2.66 – j8.95

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

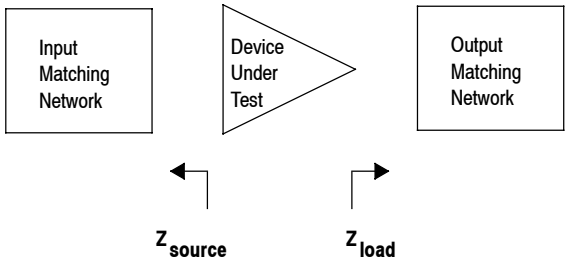


Figure 9. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

V_{DD} = 28 Vdc, I_{DQ} = 1350 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{load} (1) (Ω)	Max Output Power					
			P1dB			P3dB		
			(dBm)	(W)	η_D (%)	(dBm)	(W)	η_D (%)
2110	5.81 – j7.39	1.52 – j3.75	52.9	195	50.3	53.7	234	50.9
2140	7.36 – j5.98	1.60 – j3.97	52.8	191	49.0	53.7	234	50.7
2170	9.91 – j3.25	1.43 – j4.22	52.8	191	49.1	53.7	234	51.1

(1) Load impedance for optimum P1dB power.

Z_{source} = Impedance as measured from gate contact to ground.

Z_{load} = Impedance as measured from drain contact to ground.

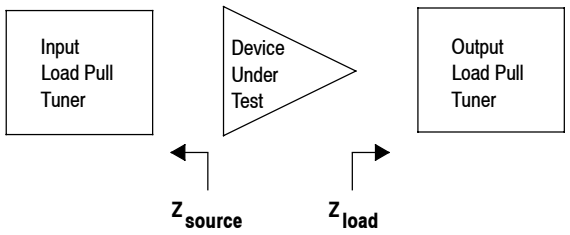


Figure 10. Load Pull Performance — Maximum P1dB Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1350 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{load} (1) (Ω)	Max Drain Efficiency					
			P1dB			P3dB		
			(dBm)	(W)	η_D (%)	(dBm)	(W)	η_D (%)
2110	5.81 – j7.39	3.31 – j2.75	51.4	138	57.9	52.1	162	60.6
2140	7.36 – j5.98	3.06 – j2.54	51.7	148	57.6	52.2	166	60.4
2170	9.91 – j3.25	2.96 – j2.98	51.8	151	57.0	52.4	174	60.4

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Impedance as measured from gate contact to ground.

Z_{load} = Impedance as measured from drain contact to ground.

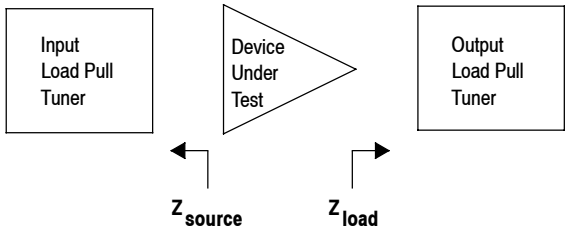
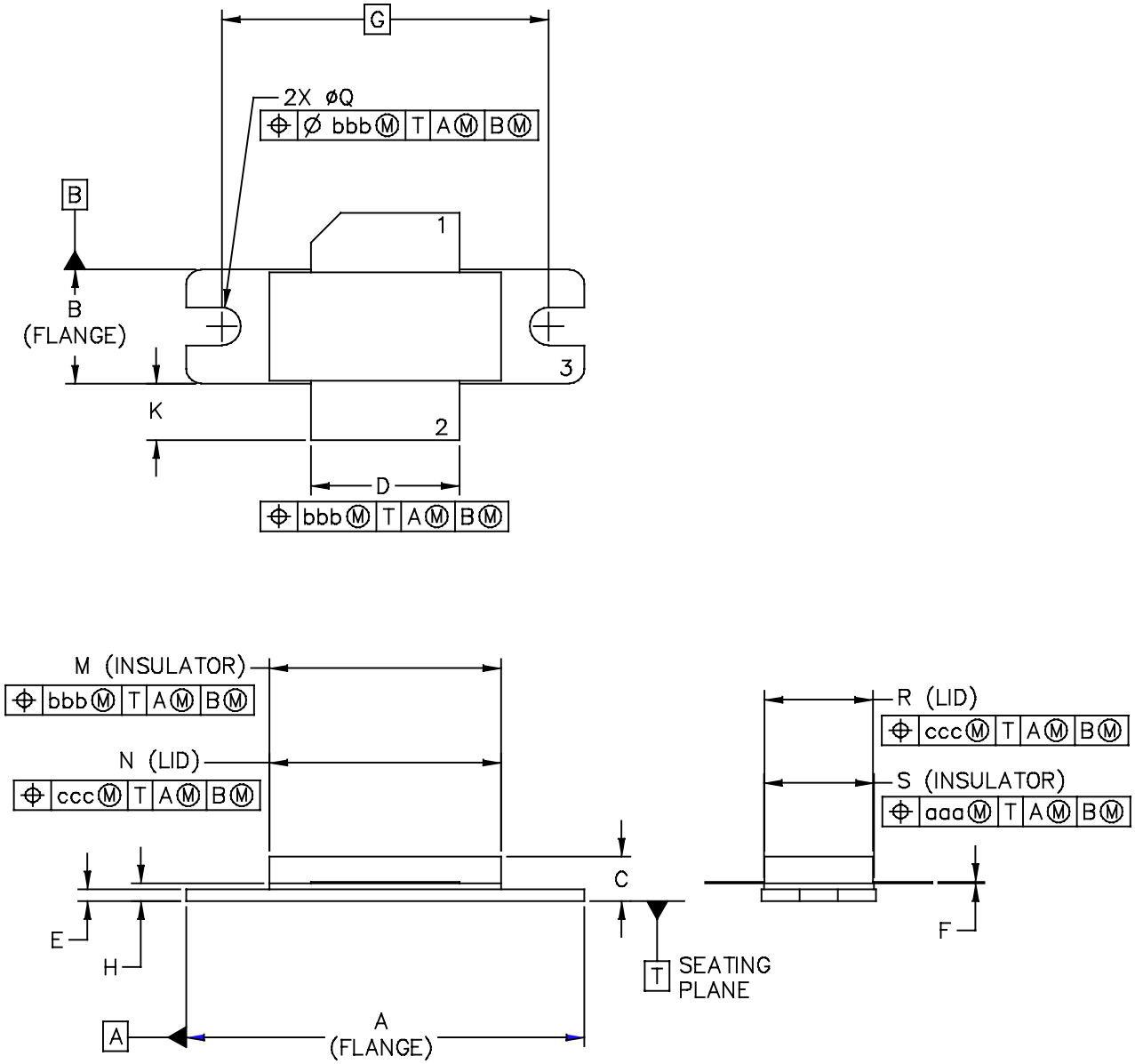


Figure 11. Load Pull Performance — Maximum Efficiency Tuning

PACKAGE DIMENSIONS



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NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	1.335	1.345	33.91	34.16	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.52
C	.125	.170	3.18	4.32	aaa	—	.005	—	0.127
D	.495	.505	12.57	12.83	bbb	—	.010	—	0.254
E	.035	.045	0.89	1.14	ccc	—	.015	—	0.381
F	.003	.006	0.08	0.15	—	—	—	—	—
G	1.100 BSC		27.94 BSC		—	—	—	—	—
H	.057	.067	1.45	1.7	—	—	—	—	—
K	.170	.210	4.32	5.33	—	—	—	—	—
M	.774	.786	19.66	19.96	—	—	—	—	—
N	.772	.788	19.6	20	—	—	—	—	—
Q	ø.118	ø.138	ø3	ø3.51	—	—	—	—	—

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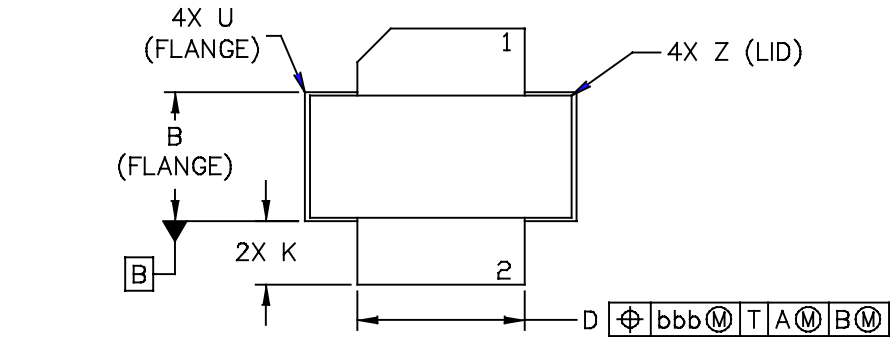

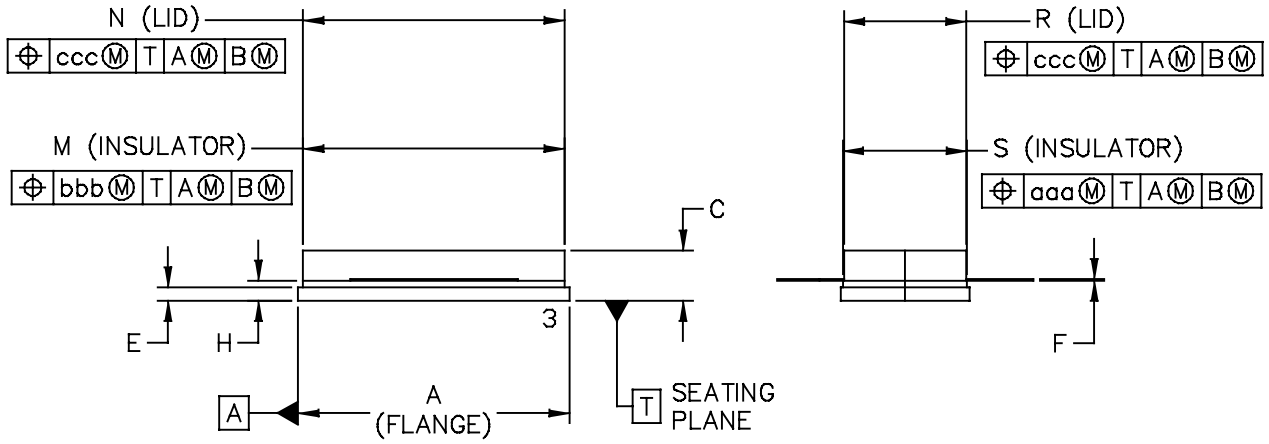

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STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.805	.815	20.45	20.7	U	–	.040	–	1.02
B	.380	.390	9.65	9.91	Z	–	.030	–	0.76
C	.125	.170	3.18	4.32	aaa	–	.005	–	0.127
D	.495	.505	12.57	12.83	bbb	–	.010	–	0.254
E	.035	.045	0.89	1.14	ccc	–	.015	–	0.381
F	.003	.006	0.08	0.15	–	–	–	–	–
H	.057	.067	1.45	1.7	–	–	–	–	–
K	.170	.210	4.32	5.33	–	–	–	–	–
M	.774	.786	19.61	20.02	–	–	–	–	–
N	.772	.788	19.61	20.02	–	–	–	–	–
R	.365	.375	9.27	9.53	–	–	–	–	–
S	.365	.375	9.27	9.52	–	–	–	–	–

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DOCUMENT NO: 98ASB16718C | REV: H

CASE NUMBER: 465A–06 | 31 MAR 2005

STANDARD: NON–JEDEC

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

R5 TAPE AND REEL OPTION

R5 Suffix = 50 Units, 56 mm Tape Width, 13 inch Reel.

The R5 tape and reel option for MRF8S21172H and MRF8S21172HS parts will be available for 2 years after release of MRF8S21172H and MRF8S21172HS. Freescale Semiconductor, Inc. reserves the right to limit the quantities that will be delivered in the R5 tape and reel option. At the end of the 2 year period customers who have purchased these devices in the R5 tape and reel option will be offered MRF8S21172H and MRF8S21172HS in the R3 tape and reel option.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2011	• Initial Release of Data Sheet
1	Mar. 2012	• Table 3, ESD Protection Characteristics, removed the word “Minimum” after the ESD class rating. ESD ratings are characterized during new product development but are not 100% tested during production. ESD ratings provided in the data sheet are intended to be used as a guideline when handling ESD sensitive devices, p. 2 • Typical Single-Carrier W-CDMA Performance table: drain efficiency typical values lowered by 1% point for all frequencies due to manufacturing capability, p. 1 • Functional Test table: changed drain efficiency minimum test limit from 30.4% to 29.2% due to manufacturing capability, p. 2 • Typical Broadband Performance table: drain efficiency typical values lowered by 1% point for all frequencies due to manufacturing capability p. 2

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