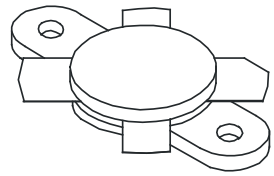
SD2931-12MR

150 W – 50 V moisture resistant HF/VHF DMOS transistor

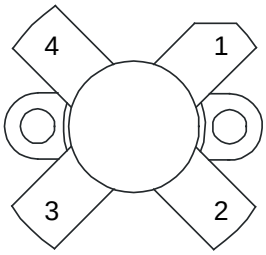
Datasheet - production data



M174MR Epoxy sealed

Figure 1: Pin connection

1. Drain
2. Source
3. Gate
4. Source



Features

- Gold metallization
- Excellent thermal stability
- Common source, push-pull configuration
- P_{OUT} = 150 W min. with 14 dB gain @ 175 MHz
- Thermally enhanced packaging for lower junction temperatures
- G_{FS} and V_{GS} sort marked on unit
- Moisture resistant package specifically designed to operate in extreme environments

Description

The SD2931-12MR is a gold metallized N-channel MOS field-effect RF power transistor. Electrically identical to the standard SD2931 MOSFET, it is intended for use in 50 V DC large signal applications up to 230 MHz.

The SD2931-12MR is mechanically compatible with the SD2931 but offers better thermal capability (25% lower thermal resistance), representing the best-in-class in transistors for ISM applications, where reliability and ruggedness are critical factors.

The SD2931-12MR benefits from the latest generation of environmentally designed packaging, ruggedized against cyclic high moisture operation and severe storage conditions.

Table 1: Device summary

Order code	Marking	Package	Packaging
SD2931-12MR	SD2931-12MR(1)	M174MR	Plastic tray

Notes:

(1) For more details please refer to *"Marking, packing and shipping specifications"*.

Contents

1 Electrical data

1.1 Maximum rating

T_{CASE}= 25 °C

Table 2: Absolute maximum rating

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain source voltage	125	V
V_{DGR}	Drain-gate voltage (R_{GS} = 1MW)	125	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current	20	A
P_{DISS}	Power dissipation	389	W
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	-65 to +150	°C

1.2 Thermal data

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction to case thermal resistance	0.45	°C/W

2 Electrical characteristics

T_{CASE}= 25 °C

Table 4: Static

Symbol	Test conditions			Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V	I_{DS} = 100 mA		125			V
I_{DSS}	V_{GS} = 0 V V_{GS} = 0 V	V_{DS} = 5 V V_{DS} = 50 V				20 50	µA
I_{GSS}	V_{GS} = 20 V	V_{DS} = 0 V				250	nA
$V_{GS(Q)}$ (1)	V_{DS} = 10 V	I_D = 250 mA		see table below			V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 10 A				3.0	V
G_{FS} (1)	V_{DS} = 10 V	I_D = 5 A		see table below			mho
C_{ISS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		480		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		190		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		18		pF

Notes:

(1)$V_{GS(Q)}$ and G_{FS} sorted with alpha/numeric code marked on unit.

Table 5: V_{GS} and G_{FS} sorts

	V_{GS}	G_{FS}
I	2.65 - 3.15	6.0 - 6.5
J	2.65 - 3.15	6.5 - 7.0
K	2.65 - 3.15	7.0 - 7.5

Table 6: Dynamic

Symbol	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	V_{DD} = 50 V I_{DQ} = 250 mA f = 175MHz	150			W
G_{PS}	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 150 W f = 175MHz	14	15		dB
η_D	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 150 W f = 175MHz	55	65		%
Load mismatch	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 150 W f = 175MHz all phase angles	10:1			VSWR

3 Impedance

Figure 2: Impedance data schematic

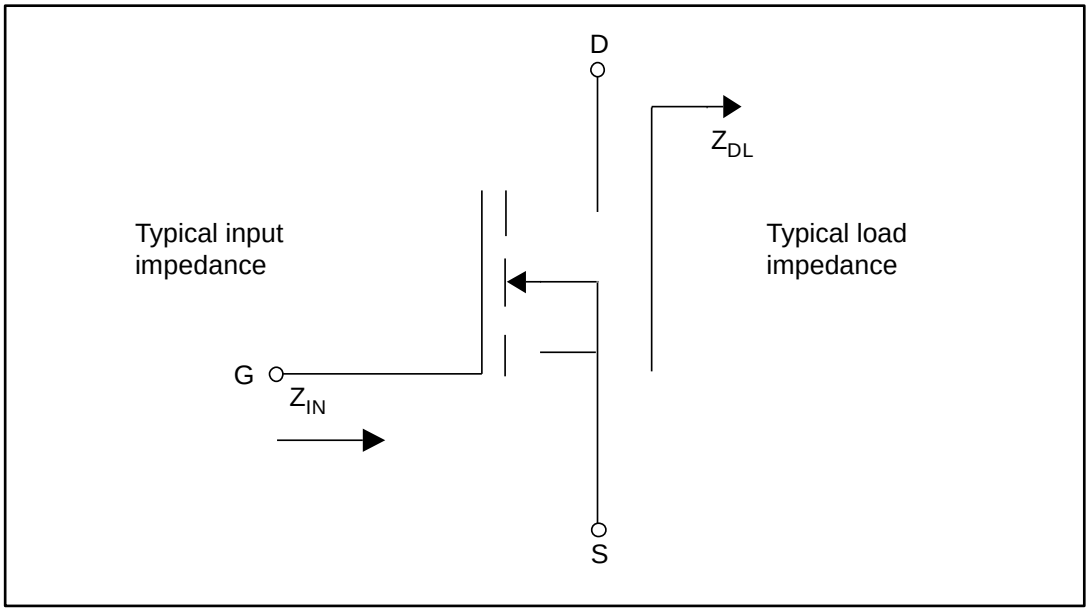


Table 7: Impedance data

f	Z IN(Ω)	Z DL(Ω)
30 MHz	1.7 - j 5.7	6.8 + j 0.9
175 MHz	1.2 - j 2.0	2.0 + j 2.4

4 Transient thermal impedance

Figure 3: Transient thermal impedance

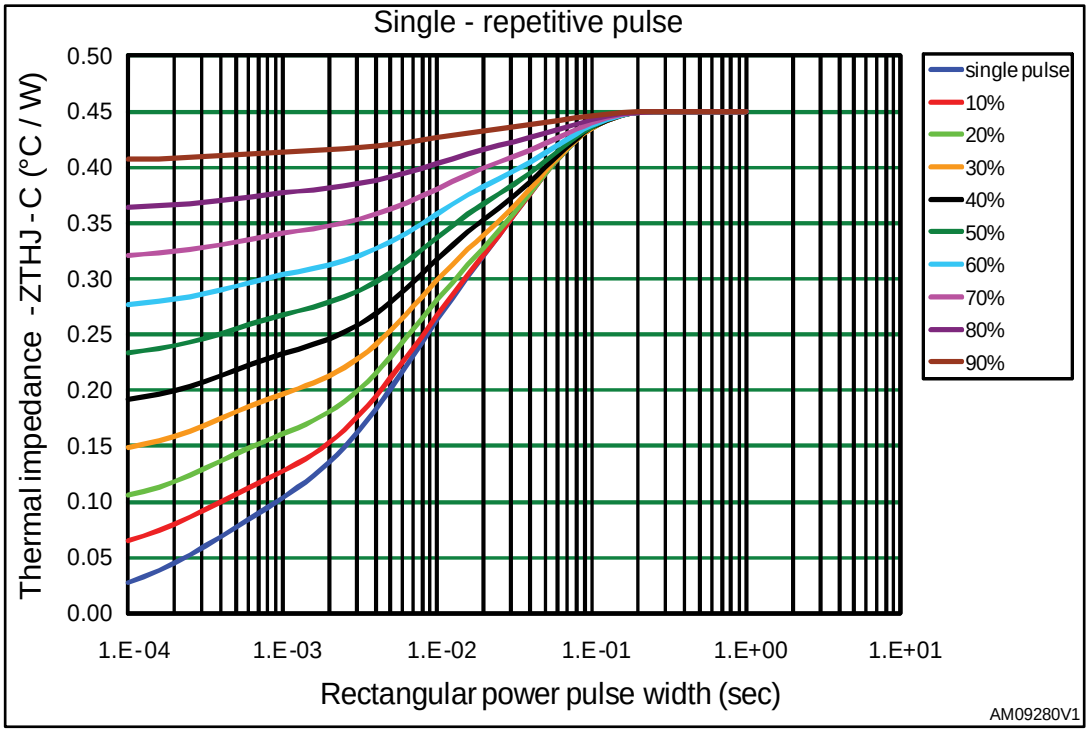
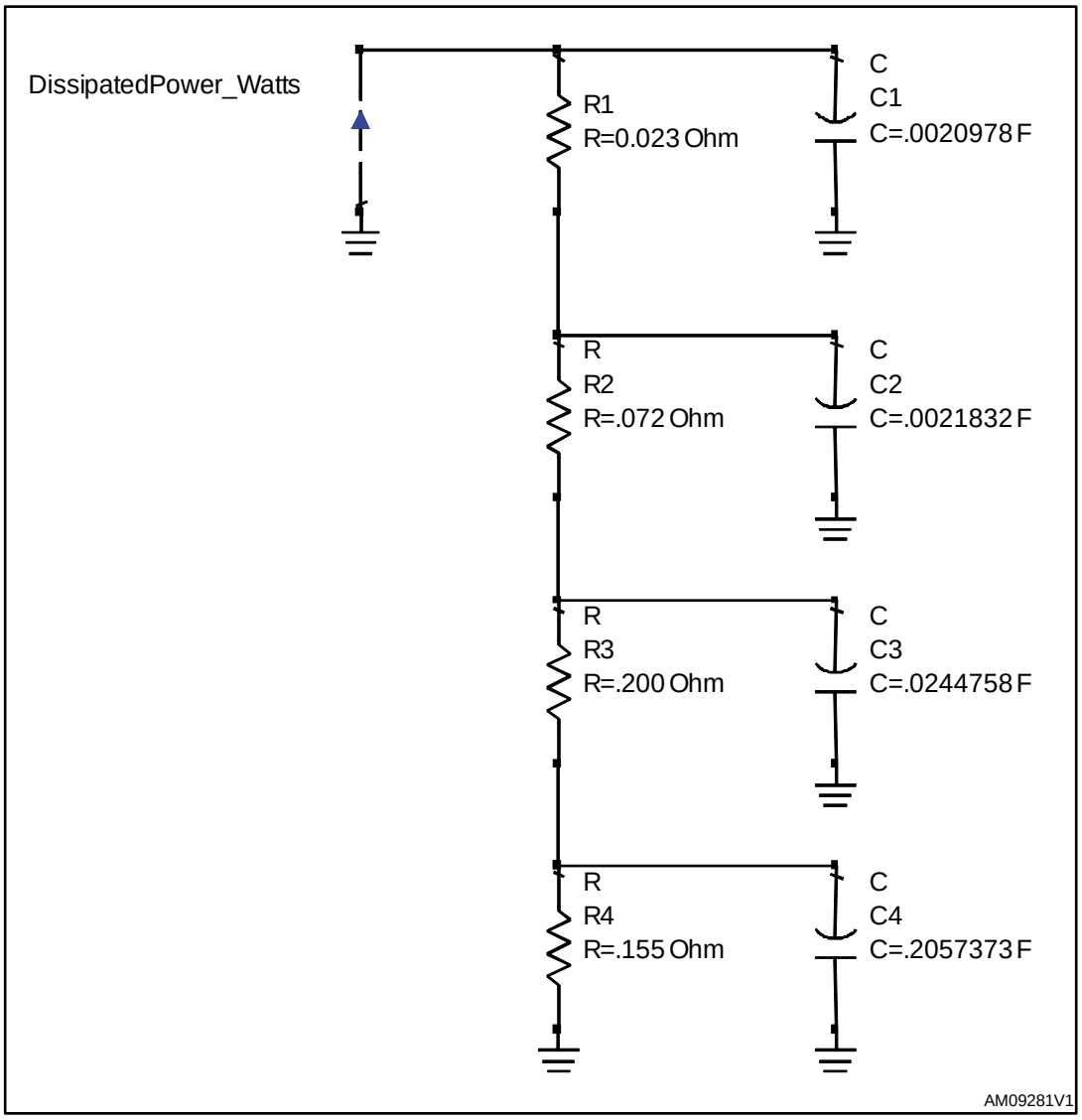


Figure 4: Transient thermal impedance model



5 Typical performance

Figure 5: Capacitance vs. drain voltage

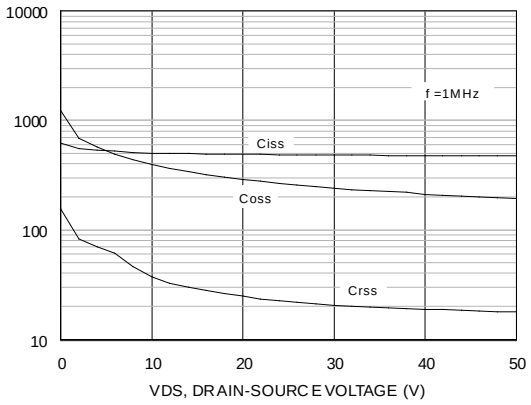


Figure 6: Drain current vs. gate voltage

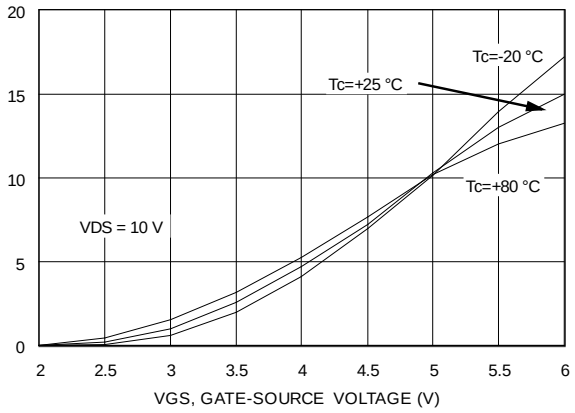


Figure 7: Gate-source voltage vs. case temperature

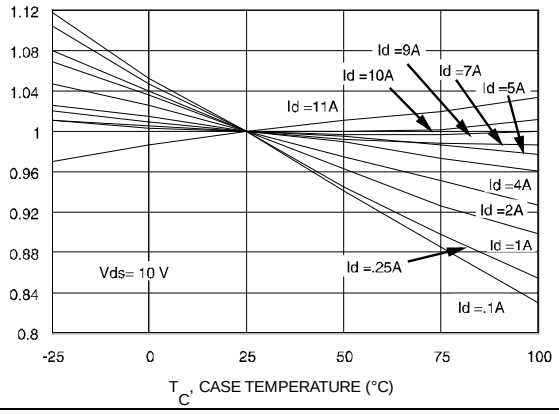


Figure 8: Maximum thermal resistance vs. case temperature

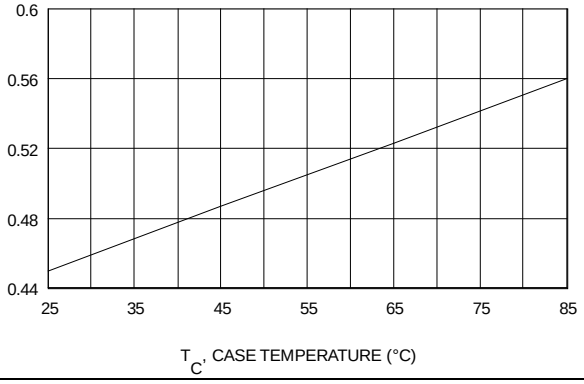
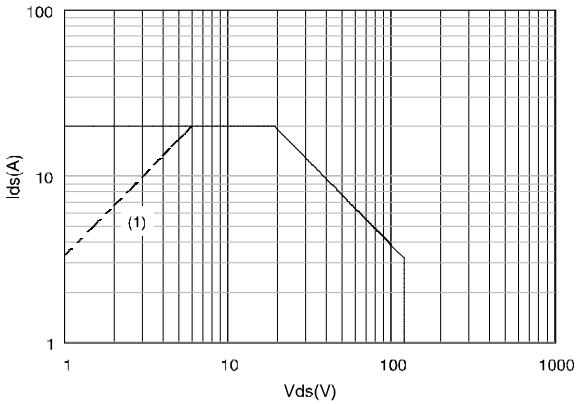


Figure 9: Safe operating area



5.1 Typical performance (175 MHz)

Figure 10: Output power vs. input power

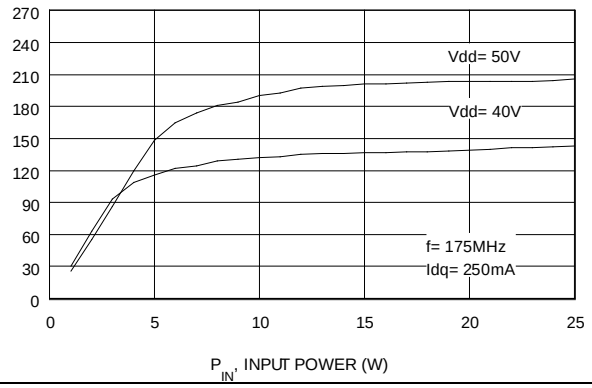


Figure 11: Output power vs. input power at different Tc

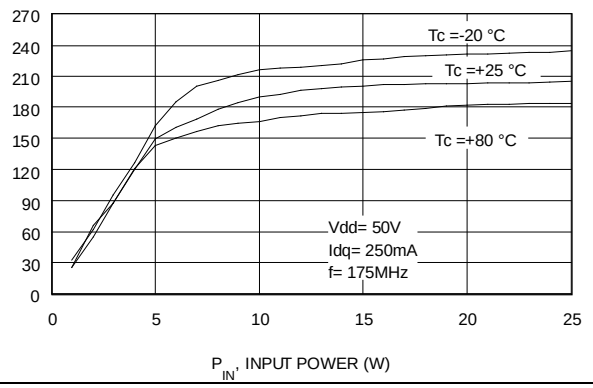


Figure 12: Power gain vs. output power

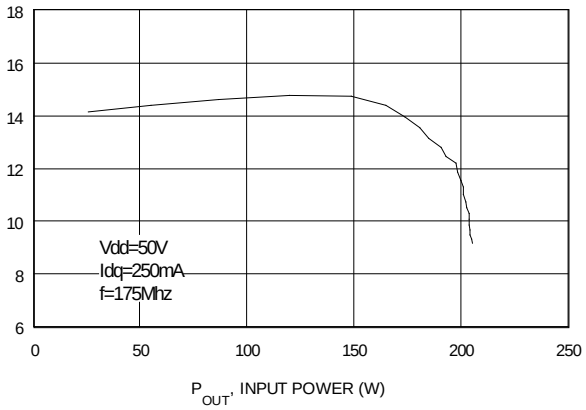


Figure 13: Efficiency vs. output power

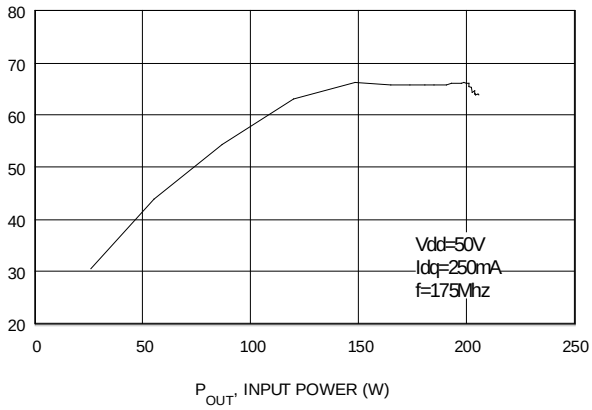


Figure 14: Output power vs. supply voltage

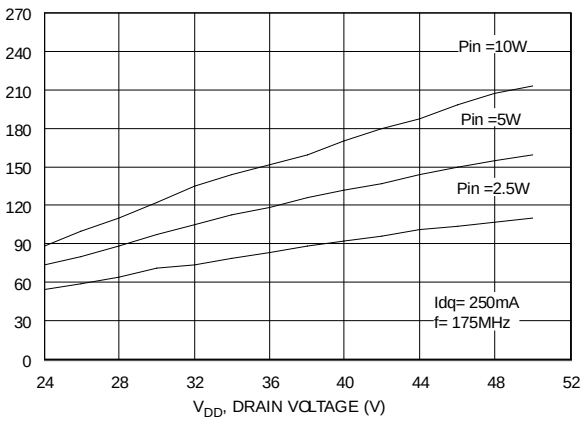
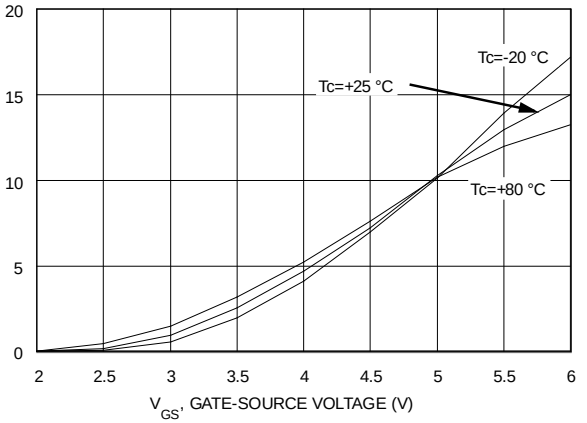


Figure 15: Drain current vs. gate-source voltage



5.1.1 Test circuit (175 MHz)

Figure 16: 175 MHz test circuit schematic (production test circuit)

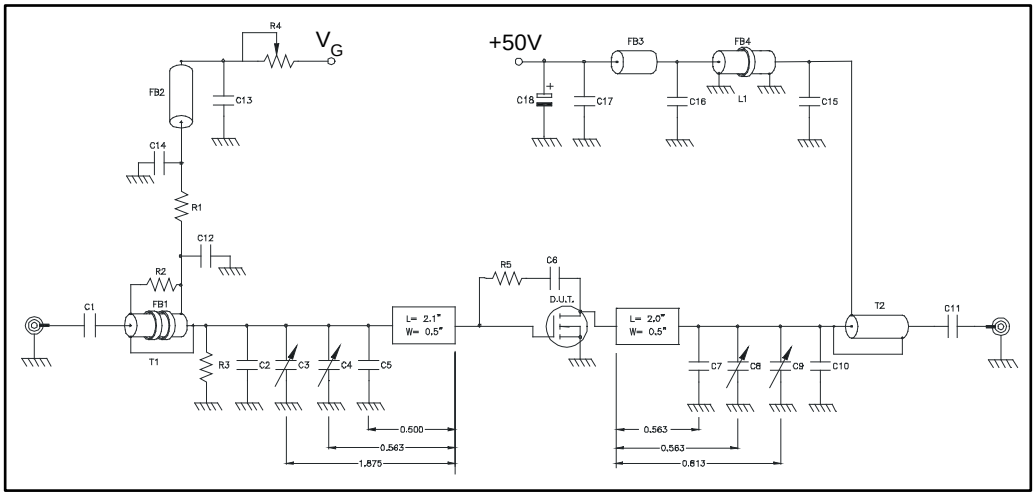


Table 8: 175 MHz test circuit parts list

Component	Description
T1	4:1 transformer, 25 Ω flexible coax .090 OD 6” long
T2	1:4 transformer, 25 Ω semi-rigid coax .141 OD 6” long
FB1	Toroid X 2, 0.5” OD .312” ID 850µ 2 turns
FB2, FB3	VK200
FB4	Shield bead, 1” OD 0.5” ID 850µ 3 turns
L1	1/4 wave choke, 50 Ω semi-rigid coax .141 OD 12” Long
PCB	0.62” woven fiberglass, 1 oz. copper, 2 Sides, εr = 2.55
R1, R3	470 Ω 1 W chip resistor
R2	360 Ω 1/2 W resistor
R4	20 kΩ 10 turn potentiometer
R5	560 Ω 1 W resistor
C1, C11	470 pF ATC chip cap
C2	43 pF ATC chip cap
C3, C8, C9	Arco 404, 12-65 pF
C4	Arco 423, 16-100 pF
C5	120 pF ATC chip cap
C6	0.01 µF ATC chip cap
C7	30 pF ATC chip cap
C10	91 pF ATC chip cap
C12, C15	1200 pF ATC chip cap
C13, C14,C16, C17	0.01 µF / 500 V chip cap
C18	10 µF 63 V electrolytic capacitor

Figure 17: 175 MHz test circuit photomaster

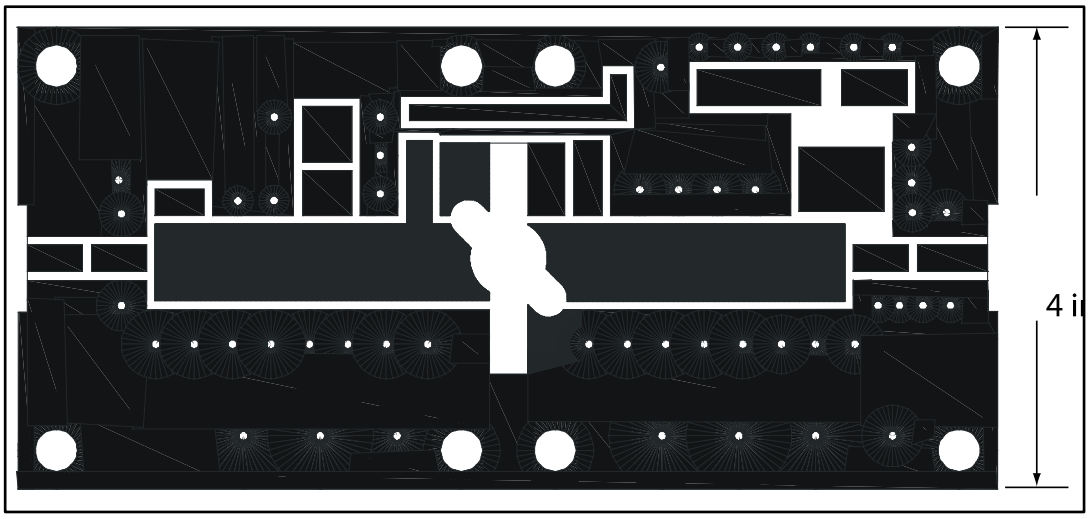
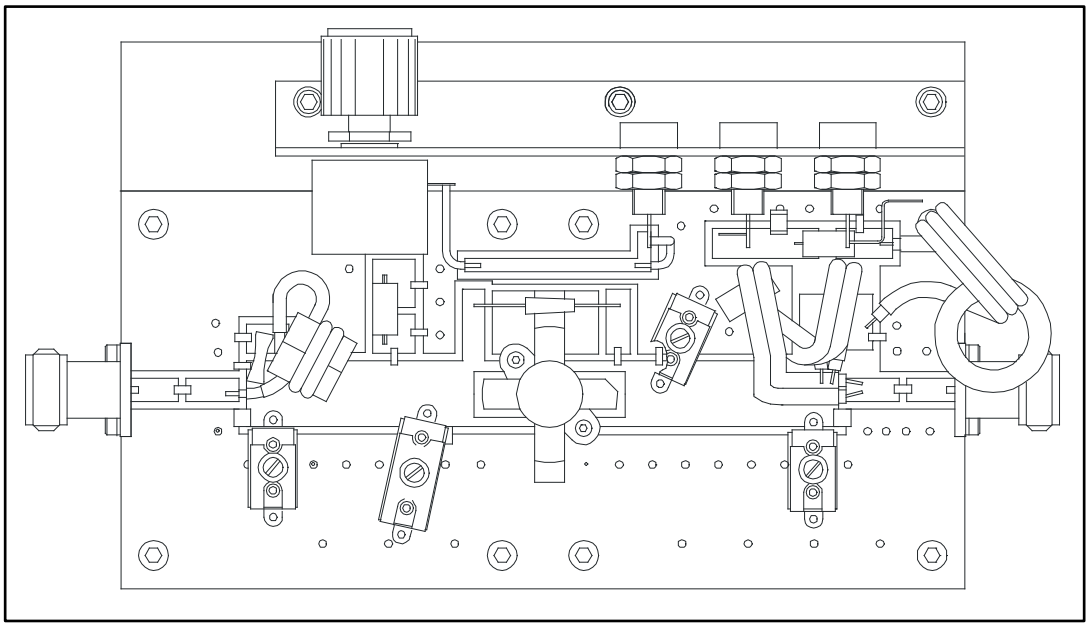


Figure 18: 175 MHz test circuit



5.3 Typical performance (30 MHz)

Figure 19: Output power vs. input power

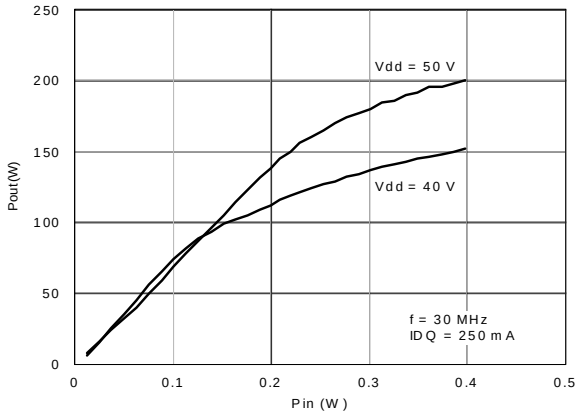


Figure 20: Power gain vs. output power

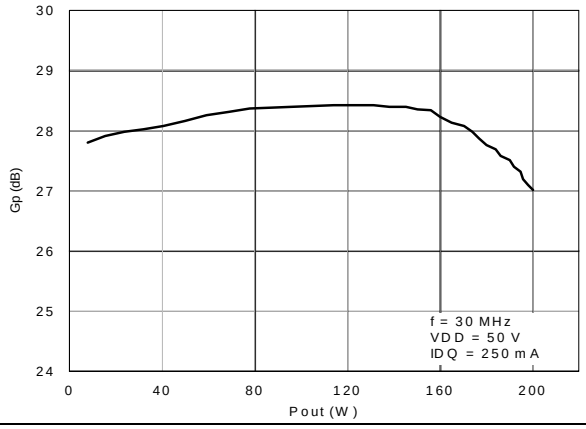


Figure 21: Efficiency vs. output power

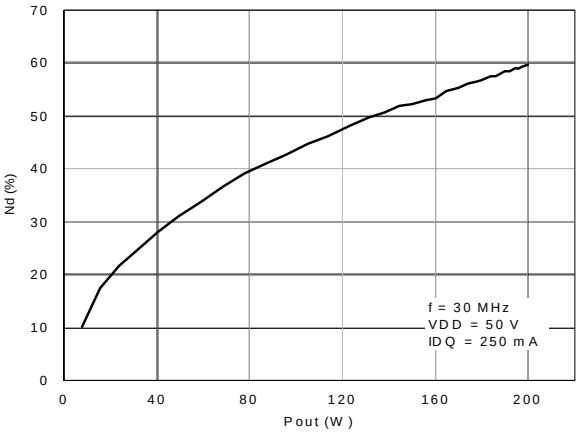


Figure 22: Output power vs. supply voltage

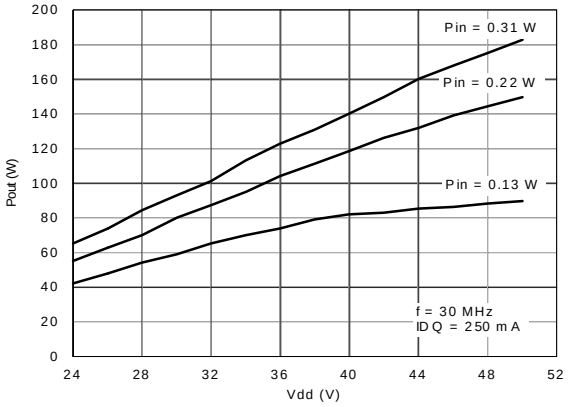
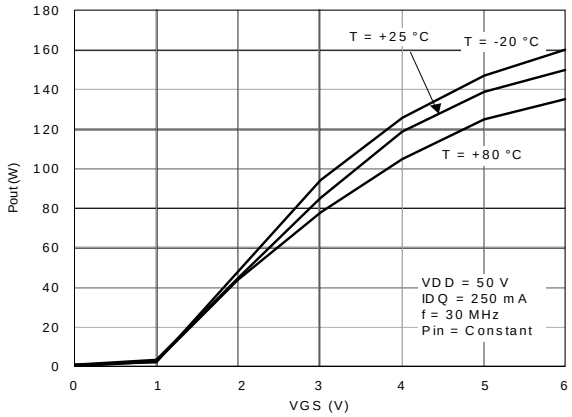


Figure 23: Output power vs. gate-source voltage



5.3.1 Test circuit (30 MHz)

Figure 24: 30 MHz test circuit schematic (production test circuit)

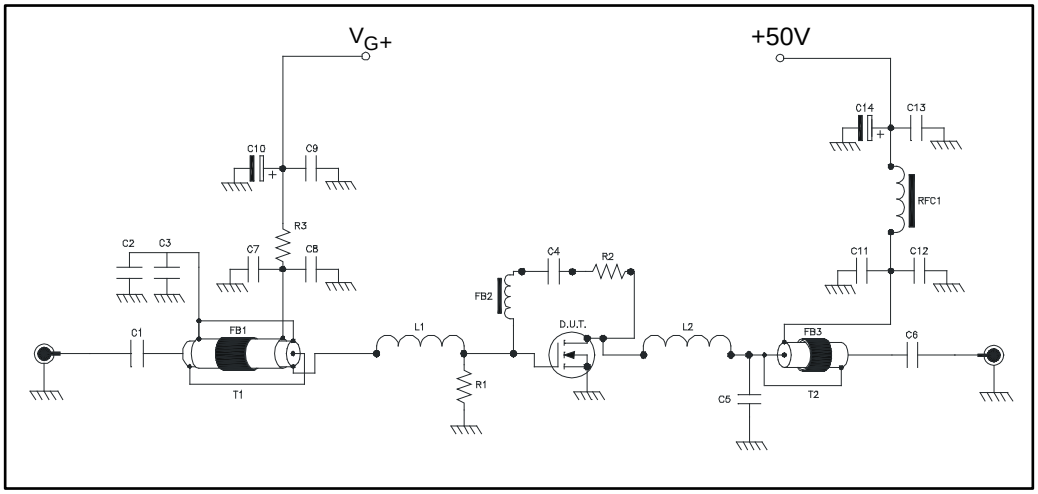


Table 9: 30 MHz test circuit part list

Component	Description
T1	9:1 transformer, 25 Ω flexible coax with extra shield .090 OD 15” long
T2	1:4 transformer, 50 Ω flexible coax .225 OD 15” long
FB1	Toroid 1.7” OD .30” ID 220µ 4 turns
FB2	Surface mount EMI shield bead
FB3	Toroid 1.7” OD .300” ID 220µ 3 turns
RFC1	Toroid 0.5” OD 0.30” ID 125µ 4 turns 12 awg wire
PCB	0.62” woven fiberglass, 1 oz. copper, 2 Sides, εr = 2.55
R1, R3	1 kohm 1 W chip resistor
R2	680 ohm 3 W wirewound resistor
C1,C4,C6,C7,C8,C9, C11,C12,C13	0.1 µF ATC chip cap
C2,C3	750 pF ATC chip cap
C5	470 pF ATC chip cap
C10	10 µF 63 V electrolytic capacitor
C14	100 µF 63 V electrolytic capacitor

6 Marking, packing and shipping specifications

Table 10: Packing and shipping specifications

Order code	Packaging	Pcs per tray	Dry pack humidity	V_{GS} and G_{FS} code	Lot code
SD2931-12MR	Plastic tray	25	< 10%	Not mixed	Not mixed

Figure 25: Marking layout for SD2391-12MR

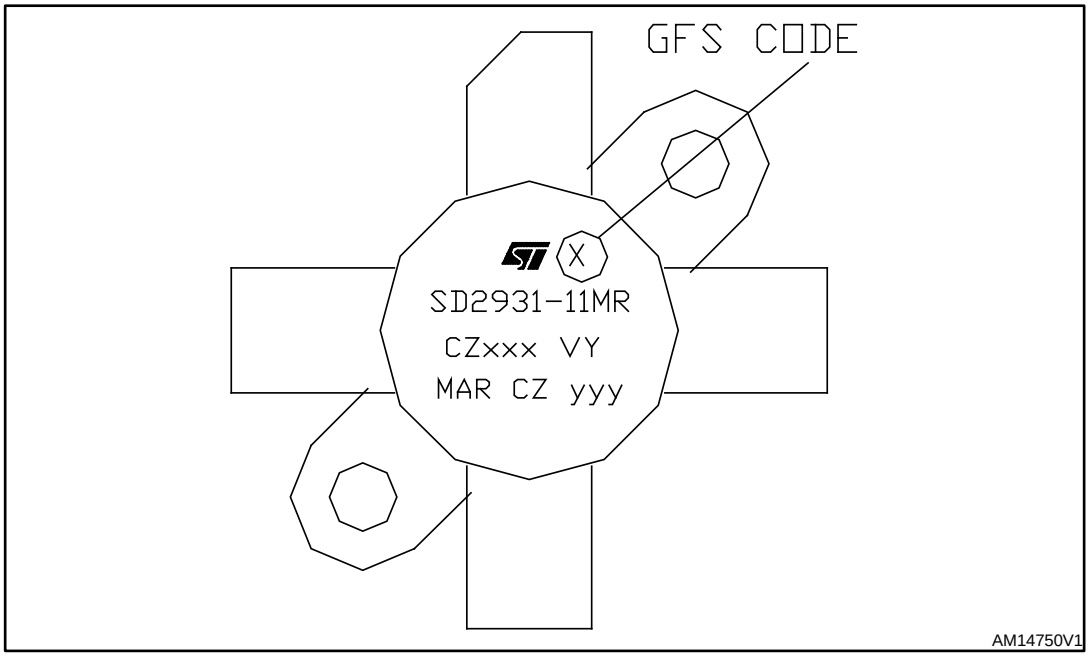


Table 11: Marking specifications

Symbol	Description
X	V_{GS} and G_{FS} sort
CZ	Assembly plant
xxx	Last 3 digits of diffusion lot
VY	Diffusion plant
MAR	Country of origin
CZ	Test and finishing plant
y	Assembly year
yy	Assembly week

7 Package information

7.1 M174MR package information

Figure 26: M174MR drawing

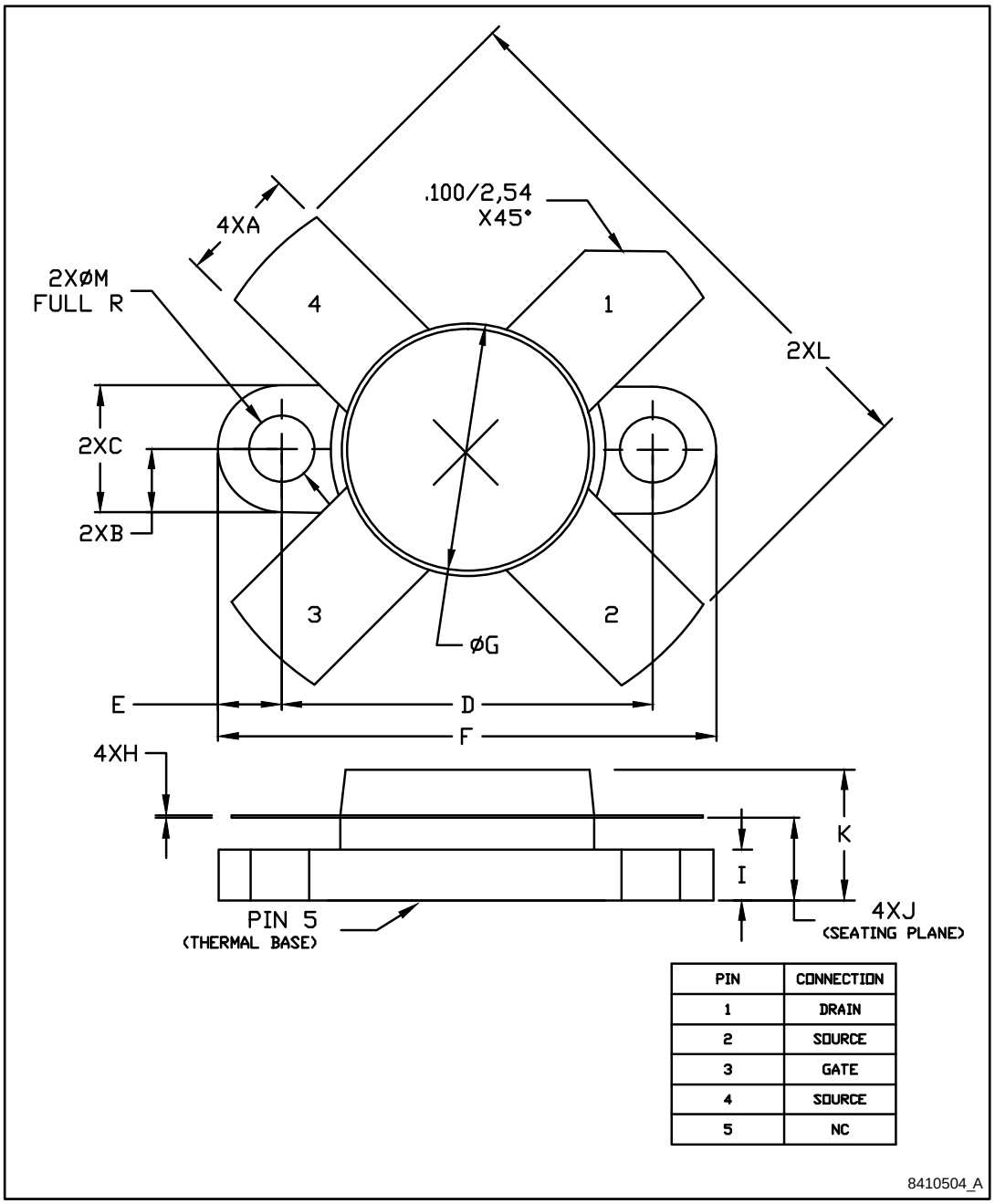


Table 12: M174MR mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	5.56		5.84
B		3.18	
C	6.22		6.48
D	18.29		18.54
E		3.18	
F	24.64		24.89
G	12.07		12.83
H	0.08		0.18
I	2.11		3.00
J	3.81		4.45
K			8.00
L	25.53		26.67
M	3.05		3.30

8 Revision history

Table 13: Document revision history

Date	Revision	Changes
20-Feb-2013	1	First issue.
10-Sep-2013	2	– Document promoted from preliminary data to full datasheet. – Formatting and minor text changes.

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