ATF-55143

Low Noise Enhancement Mode Pseudomorphic HEMT in a Surface Mount Plastic Package

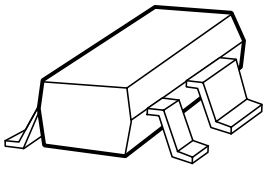
Data Sheet

Description

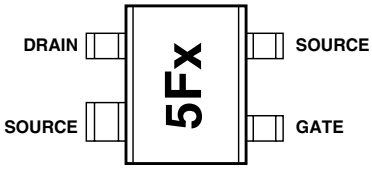
Avago Technologies' ATF-55143 is a high dynamic range, very low noise, single supply E-PHEMT housed in a 4-lead SC-70 (SOT-343) surface mount plastic package.

The combination of high gain, high linearity and low noise makes the ATF-55143 ideal for cellular/PCS handsets, wireless data systems (WLL/RLL, WLAN and MMDS) and other systems in the 450 MHz to 6 GHz frequency range.

Surface Mount Package SOT-343



Pin Connections and Package Marking



Note:
Top View. Package marking provides orientation and identification

"5F" = Device Code
"x" = Date code character identifies month of manufacture.

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 0)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

Features

- High linearity performance
- Single Supply Enhancement Mode Technology[1]
- Very low noise figure
- Excellent uniformity in product specifications
- 400 micron gate width
- Low cost surface mount small plastic package SOT-343 (4 lead SC-70)
- Tape-and-Reel packaging option available
- Lead Free Option Available

Specifications

- 2 GHz; 2.7V, 10 mA (Typ.)
- 24.2 dBm output 3rd order intercept
- 14.4 dBm output power at 1 dB gain compression
- 0.6 dB noise figure
- 17.7 dB associated gain
- Lead-free option available

Applications

- Low noise amplifier for cellular/PCS handsets
- LNA for WLAN, WLL/RLL and MMDS applications
- General purpose discrete E-PHEMT for other ultra low noise applications

Note:
1. Enhancement mode technology requires positive Vgs, thereby eliminating the need for the negative gate voltage associated with conventional depletion mode devices.

ATF-55143 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain-Source Voltage[2]	V	5
V_{GS}	Gate-Source Voltage[2]	V	-5 to 1
V_{GD}	Gate Drain Voltage[2]	V	-5 to 1
I_{DS}	Drain Current[2]	mA	100
I_{GS}	Gate Current[5]	mA	1
P_{diss}	Total Power Dissipation[3]	mW	270
$P_{in\ max.}$	RF Input Power[5]		
	(Vds=2.7V, Ids=10mA)	dBm	10
	(Vds=0V, Ids=0mA)	dBm	10
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{jc}	Thermal Resistance[4]	°C/W	235
	ESD (Human Body Model)	V	200
	ESD (Machine Model)	V	25

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. Source lead temperature is 25°C. Derate 4.3 mW/°C for T_L > 87°C.
4. Thermal resistance measured using 150°C Liquid Crystal Measurement method.
5. Device can safely handle +10 dBm RF Input Power as long as I_{GS} is limited to 1 mA. I_{GS} at P_{1dB} drive level is bias circuit dependent. See applications section for additional information.

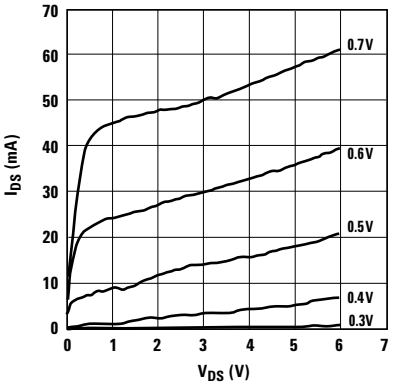


Figure 1. Typical I-V Curves. (V_{GS} = 0.1 V per step)

Product Consistency Distribution Charts[6, 7]

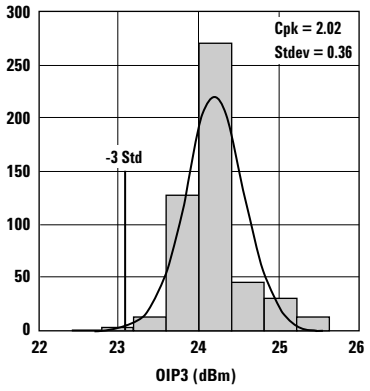


Figure 2. OIP3 @ 2.7 V, 10 mA. LSL = 22.0, Nominal = 24.2

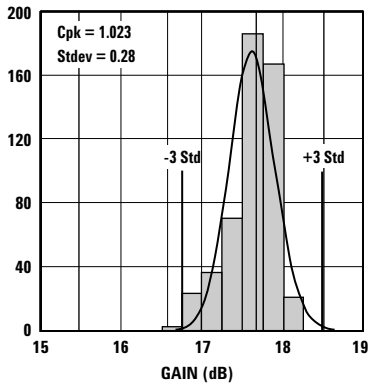


Figure 3. Gain @ 2.7 V, 10 mA. USL = 18.5, LSL = 15.5, Nominal = 17.7

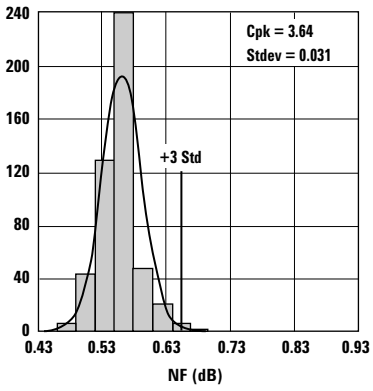


Figure 4. NF @ 2.7 V, 10 mA. USL = 0.9, Nominal = 0.6

Notes:
6. Distribution data sample size is 500 samples taken from 6 different wafers. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
7. Measurements made on production test board. This circuit represents a trade-off between an optimal noise match and a realizeable match based on production test equipment. Circuit losses have been de-embedded from actual measurements.

ATF-55143 Electrical Specifications

T_A = 25°C, RF parameters measured in a test circuit for a typical device

Symbol	Parameter and Test Condition			Units	Min.	Typ.[2]	Max.
Vgs	Operational Gate Voltage		Vds = 2.7V, Ids = 10 mA	V	0.3	0.47	0.65
Vth	Threshold Voltage		Vds = 2.7V, Ids = 2 mA	V	0.18	0.37	0.53
Idss	Saturated Drain Current		Vds = 2.7V, Vgs = 0V	µA	—	0.1	3
Gm	Transconductance		Vds = 2.7V, gm = ΔIdss/ΔVgs; ΔVgs = 0.75 – 0.7 = 0.05V	mmho	110	220	285
Igss	Gate Leakage Current		Vgd = Vgs = -2.7V	µA	—	—	95
NF	Noise Figure [1]	f = 2 GHz	Vds = 2.7V, Ids = 10 mA	dB	—	0.6	0.9
		f = 900 MHz	Vds = 2.7V, Ids = 10 mA	dB	—	0.3	—
Ga	Associated Gain [1]	f = 2 GHz	Vds = 2.7V, Ids = 10 mA	dB	15.5	17.7	18.5
		f = 900 MHz	Vds = 2.7V, Ids = 10 mA	dB	—	21.6	—
OIP3	Output 3rd Order Intercept Point [1]	f = 2 GHz	Vds = 2.7V, Ids = 10 mA	dBm	22.0	24.2	—
		f = 900 MHz	Vds = 2.7V, Ids = 10 mA	dBm	—	22.3	—
P1dB	1dB Compressed Output Power [1]	f = 2 GHz	Vds = 2.7V, Ids = 10 mA	dBm	—	14.4	—
		f = 900 MHz	Vds = 2.7V, Ids = 10 mA	dBm	—	14.2	—

Notes:

1. Measurements obtained using production test board described in Figure 5.
2. Typical values determined from a sample size of 500 parts from 6 wafers.

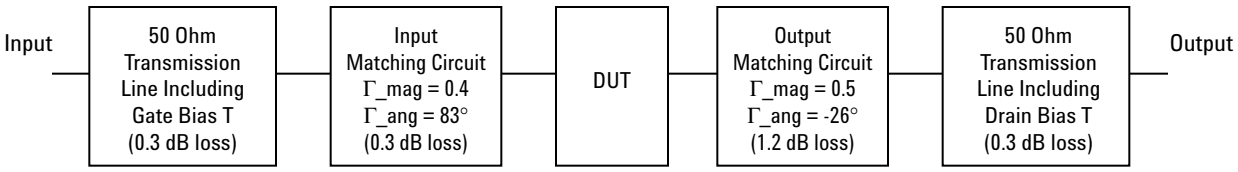


Figure 5. Block diagram of 2 GHz production test board used for Noise Figure, Associated Gain, P1dB, OIP3, and IIP3 measurements. This circuit represents a trade-off between an optimal noise match, maximum OIP3 match and associated impedance matching circuit losses. Circuit losses have been de-embedded from actual measurements.