Quad, 12-Bit, 170 MSPS/210 MSPS/250 MSPS Serial Output 1.8 V ADC

Data Sheet **AD9239**

FEATURES

- 4 ADCs in 1 package
- Coded serial digital outputs with ECC per channel
- On-chip temperature sensor
- −95 dB channel-to-channel crosstalk
- SNR = 65 dBFS with AIN = 85 MHz at 250 MSPS
- SFDR = 77 dBc with AIN = 85 MHz at 250 MSPS
- Excellent linearity
  - DNL = ±0.3 LSB (typical)
  - INL = ±0.7 LSB (typical)
- 780 MHz full power analog bandwidth
- Power dissipation = 380 mW per channel at 250 MSPS
- 1.25 V p-p input voltage range, adjustable up to 1.5 V p-p
- 1.8 V supply operation
- Clock duty cycle stabilizer
- Serial port interface features
  - Power-down modes
  - Digital test pattern enable
  - Programmable header
  - Programmable pin functions (PGMx, PDWN)

APPLICATIONS

- Communication receivers
- Cable head end equipment/M-CMTS
- Broadband radios
- Wireless infrastructure transceivers
- Radar/military-aerospace subsystems
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

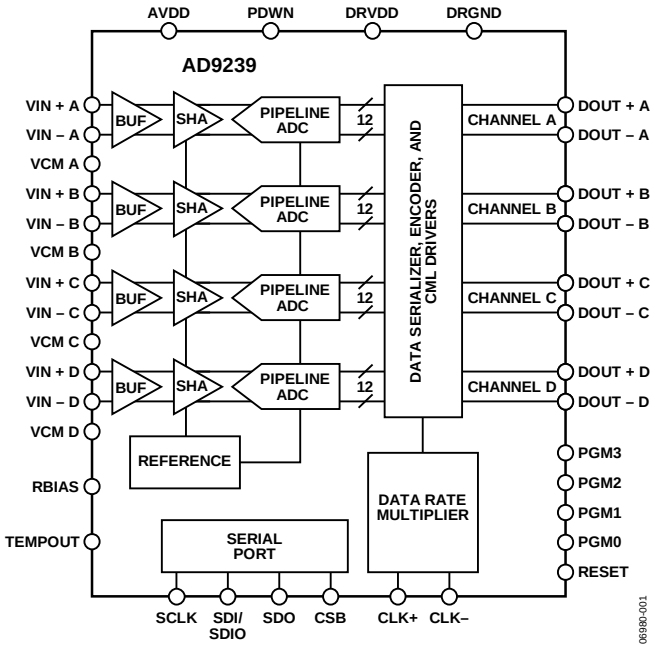

Figure 1.

GENERAL DESCRIPTION

The AD9239 is a quad, 12-bit, 250 MSPS analog-to-digital converter (ADC) with an on-chip temperature sensor and a high speed serial interface. It is designed to support digitizing high frequency, wide dynamic range signals with an input bandwidth up to 780 MHz. The output data are serialized and presented in packet format, consisting of channel-specific information, coded samples, and error correction code.

The ADC requires a single 1.8 V power supply and the input clock may be driven differentially with a sine wave, LVPECL, TTL, or LVDS. A clock duty cycle stabilizer allows high performance at full speed with a wide range of clock duty cycles. The on-chip reference eliminates the need for external decoupling and can be adjusted by means of SPI control.

Various power-down and standby modes are supported. The ADC typically consumes 145 mW per channel with the digital link still in operation when standby operation is enabled.

Fabricated on an advanced CMOS process, the AD9239 is available in a Pb-free/RoHS-compliant, 72-lead LFCSP package. It is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Four ADCs are contained in a small, space-saving package.
2. An on-chip PLL allows users to provide a single ADC sampling clock, and the PLL distributes and multiplies up to produce the corresponding data rate clock.
3. Coded data rate supports up to 4.0 Gbps per channel. Coding includes scrambling to ensure proper dc common mode, embedded clock, and error correction.
4. The AD9239 operates from a single 1.8 V power supply.
5. Flexible synchronization schemes and programmable mode pins.
6. On-chip temperature sensor.

Rev. D
Document Feedback

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REVISION HISTORY

5/14—Rev. C to Rev. D

Changes to Digital Outputs and Timing Section ... 25
Changes to Table 15 ... 35

6/13—Rev. B to Rev. C

Changed Temperature Sensor Output Current Drive from 10 µA to 50 µA; Table 1 ... 3
Changes to Digital Outputs and Timing Section ... 24
Updated Outline Dimensions ... 38

5/10—Rev. A to Rev. B

Changes to Table 15 ... 35, 36

2/10—Rev. 0 to Rev. A

Changes to Analog Inputs, Differential Input Voltage Range Parameter and Endnote 3, Table 1 ... 3
Changes to Table 8 ... 9
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Changes to Digital Outputs and Timing Section ... 23
Changes to Table 15 ... 34

10/08—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, 1.25 V p-p differential input, AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 1.

		AD9239BCPZ-170			AD9239BCPZ-210			AD9239BCPZ-250			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			12						Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	25°C		−2	±12		−2	±12		−2	±12	mV
Offset Matching	25°C		4	12		4	12		4	12	mV
Gain Error	25°C	−2.8	+1	+4.7	−2.8	+1	+4.7	−2.8	+1	+4.7	% FS
Gain Matching	25°C		0.9	2.7		0.9	2.7		0.9	2.7	% FS
Differential Nonlinearity (DNL)	Full		±0.28	±0.6		±0.28	±0.6		±0.3	±0.6	LSB
Integral Nonlinearity (INL)	Full		±0.45	±0.9		±0.7	±1.3		±0.7	±1.3	LSB
ANALOG INPUTS											
Differential Input Voltage Range[2]	Full	1.0	1.25	1.5	1.0	1.25	1.5	1.0	1.25	1.5	V p-p
Common-Mode Voltage	Full		1.4			1.4			1.4		V
Input Capacitance	25°C		2			2			2		pF
Input Resistance	Full		4.3			4.3			4.3		kΩ
Analog Bandwidth, Full Power	Full		780			780			780		MHz
Voltage Common Mode (VCMx)											
Voltage Output	Full	1.4	1.44	1.5	1.4	1.44	1.5	1.4	1.44	1.5	V
Current Drive	Full		1			1			1		mA
Temperature Sensor Output			−1.12			−1.12			−1.12		mV/°C
Voltage Output	Full		739			737			734		mV
Current Drive	Full		50			50			50		µA
POWER SUPPLY											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{AVDD}	Full		535	570		610	650		725	775	mA
I_{DRVDD}	Full		98	105		111	120		123	133	mA
Total Power Dissipation (Including Output Drivers)	Full		1.139	1.215		1.298	1.386		1.526	1.634	W
Power-Down Dissipation	Full		3			3			3		mW
Standby Dissipation[2]	Full		152			173			195		mW
CROSSTALK	Full		−95			−95			−95		dB
Overrange Condition[3]	Full		−90			−90			−90		dB

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and details on how these tests were completed.
[2] AVDD/DRVDD, with link established.
[3] Overrange condition is specified as 6 dB above the full-scale input range.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, 1.25 V p-p differential input, AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 2.

		AD9239BCPZ-170			AD9239BCPZ-210			AD9239BCPZ-250			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)											
f_{IN} = 9.7 MHz	25°C								64.5		dB
f_{IN} = 84.3 MHz	Full	63.5	64.5		63.2	64.2		63.1	64.1		dB
f_{IN} = 170.3 MHz	25°C								63.9		dB
f_{IN} = 240.3 MHz	25°C		64.1			63.2			63.3		dB
SIGNAL-TO-NOISE RATIO (SINAD)											
f_{IN} = 9.7 MHz	25°C								64.2		dB
f_{IN} = 84.3 MHz	Full	63.3	64.4		62.8	63.9		62.8	63.8		dB
f_{IN} = 170.3 MHz	25°C								63.1		dB
f_{IN} = 240.3 MHz	25°C		63.9			63			63.1		dB
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 9.7 MHz	25°C								10.4		Bits
f_{IN} = 84.3 MHz	Full	10.2	10.4		10.1	10.3		10.14	10.3		Bits
f_{IN} = 170.3 MHz	25°C								10.2		Bits
f_{IN} = 240.3 MHz	25°C		10.3			10.2			10.2		Bits
WORST HARMONIC (SECOND)											
f_{IN} = 9.7 MHz	25°C								90		dBc
f_{IN} = 84.3 MHz	Full		87.5	78.6		86	77		86	74.5	dBc
f_{IN} = 170.3 MHz	25°C								76		dBc
f_{IN} = 240.3 MHz	25°C		82			80			82		dBc
WORST HARMONIC (THIRD)											
f_{IN} = 9.7 MHz	25°C								78		dBc
f_{IN} = 84.3 MHz	Full		79	74		76	72.6		76	72.5	dBc
f_{IN} = 170.3 MHz	25°C								74		dBc
f_{IN} = 240.3 MHz	25°C		84			77			80		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD)											
f_{IN} = 9.7 MHz	25°C								85		dBc
f_{IN} = 84.3 MHz	Full		96	86		90	83.7		94	83.6	dBc
f_{IN} = 170.3 MHz	25°C								85		dBc
f_{IN} = 240.3 MHz	25°C		88			88			85		dBc
TWO-TONE INTERMOD DISTORTION (IMD)											
f_{IN1} = 140.2 MHz, f_{IN2} = 141.3 MHz, AIN1 and AIN2 = −7.0 dBFS	25°C		78			77			76		dBc
f_{IN1} = 170.2 MHz, f_{IN2} = 171.3 MHz, AIN1 and AIN2 = −7.0 dBFS[2]	25°C					77			76		dBc

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and details on how these tests were completed.
[2] Tested at 210 MSPS and 250 MSPS only.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, 1.25 V p-p differential input, AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 3.

		AD9239BCPZ-170			AD9239BCPZ-210			AD9239BCPZ-250			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUTS (CLK+, CLK–)											
Logic Compliance	Full		LVPECL/LVDS/CMOS			LVPECL/LVDS/CMOS			LVPECL/LVDS/CMOS		
Differential Input Voltage	Full	0.2		6	0.2		6	0.2		6	V p-p
Input Voltage Range	Full	AVDD – 0.3		AVDD + 1.6	AVDD – 0.3		AVDD + 1.6	AVDD – 0.3		AVDD + 1.6	V
Internal Common-Mode Bias	Full		1.2			1.2			1.2		V
Input Common-Mode Voltage	Full	1.1		AVDD	1.1		AVDD	1.1		AVDD	V
High Level Input Voltage (V_{IH})	Full	1.2		3.6	1.2		3.6	1.2		3.6	V
Low Level Input Voltage (V_{IL})	Full	0		0.8	0		0.8	0		0.8	V
High Level Input Current (I_{IH})	Full	−10		+10	−10		+10	−10		+10	µA
Low Level Input Current (I_{IL})	Full	−10		+10	−10		+10	−10		+10	µA
Differential Input Resistance	25°C	16	20	24	16	20	24	16	20	24	kΩ
Input Capacitance	25°C		4			4			4		pF
LOGIC INPUTS (PDWN, CSB, SDI/SDIO, SCLK, RESET, PGMx)[2]											
Logic 1 Voltage	Full	0.8 × AVDD			0.8 × AVDD			0.8 × AVDD			V
Logic 0 Voltage	Full			0.2 × AVDD			0.2 × AVDD			0.2 × AVDD	V
Logic 1 Input Current (CSB)	Full		0			0			0		µA
Logic 0 Input Current (CSB)	Full		−60			−60			−60		µA
Logic 1 Input Current (SCLK, PDWN, SDI/SDIO, RESET, PGMx)	Full		55			55			55		µA
Logic 0 Input Current (SCLK, PDWN, SDI/SDIO, RESET, PGMx)	Full		0			0			0		µA
Input Resistance	25°C		30			30			30		kΩ
Input Capacitance	25°C		4			4			4		pF
LOGIC OUTPUTS (SDO)											
Logic 1 Voltage	Full	1.2		AVDD + 0.3	1.2		AVDD + 0.3	1.2		AVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	0		0.3	0		0.3	V
DIGITAL OUTPUTS (DOUT + x, DOUT – x)											
Logic Compliance			Current mode logic			Current mode logic			Current mode logic		
Differential Output Voltage	Full		0.8			0.8			0.8		V
Common-Mode Level	Full		DRVDD/2			DRVDD/2			DRVDD/2		V

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and details on how these tests were completed.
[2] Specified for 13 SDI/SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, 1.25 V p-p differential input, AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 4.

		AD9239BCPZ-170			AD9239BCPZ-210			AD9239BCPZ-250			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK											
Clock Rate	Full	170		100	210		100	250		100	MSPS
Clock Pulse Width High (t_{EH})	Full	2.65	2.9		2.15	2.4		1.8	2.0		ns
Clock Pulse Width Low (t_{EL})	Full	2.65	2.9		2.15	2.4		1.8	2.0		ns
DATA OUTPUT PARAMETERS											
Data Output Period or UI (DOUT + x, DOUT − x)	Full		1/(16 × f_{CLK})			1/(16 × f_{CLK})			1/(16 × f_{CLK})		sec
Data Output Duty Cycle	25°C		50			50			50		%
Data Valid Time	25°C		0.8			0.8			0.8		UI
PLL Lock Time (t_{LOCK})	25°C		4			4			4		µs
Wake-Up Time (Standby)	25°C		250			250			250		ns
Wake-Up Time (Power-Down)[2]	25°C		50			50			50		µs
Pipeline Latency	Full			40			40			40	CLK cycles
Data Rate per Channel (NRZ)	25°C		2.72			3.36			4.0		Gbps
Deterministic Jitter	25°C		10			10			10		ps max
Random Jitter	25°C		6			6			6		ps rms
Channel-to-Channel Bit Skew	25°C		0			0			0		sec
Channel-to-Channel Packet Skew[3]	25°C		±1			±1			±1		CLK cycles
Output Rise/Fall Time	25°C		50			50			50		ps
TERMINATION CHARACTERISTICS											
Differential Termination Resistance	25°C		100			100			100		Ω
APERTURE											
Aperture Delay (t_A)	25°C		1.2			1.2			1.2		ns
Aperture Uncertainty (Jitter)	25°C		0.2			0.2			0.2		ps rms
OUT-OF-RANGE RECOVERY TIME	25°C		1			1			1		CLK cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and details on how these tests were completed.
[2] Receiver dependent.
[3] See the Digital Start-Up Sequence section.

TIMING DIAGRAM

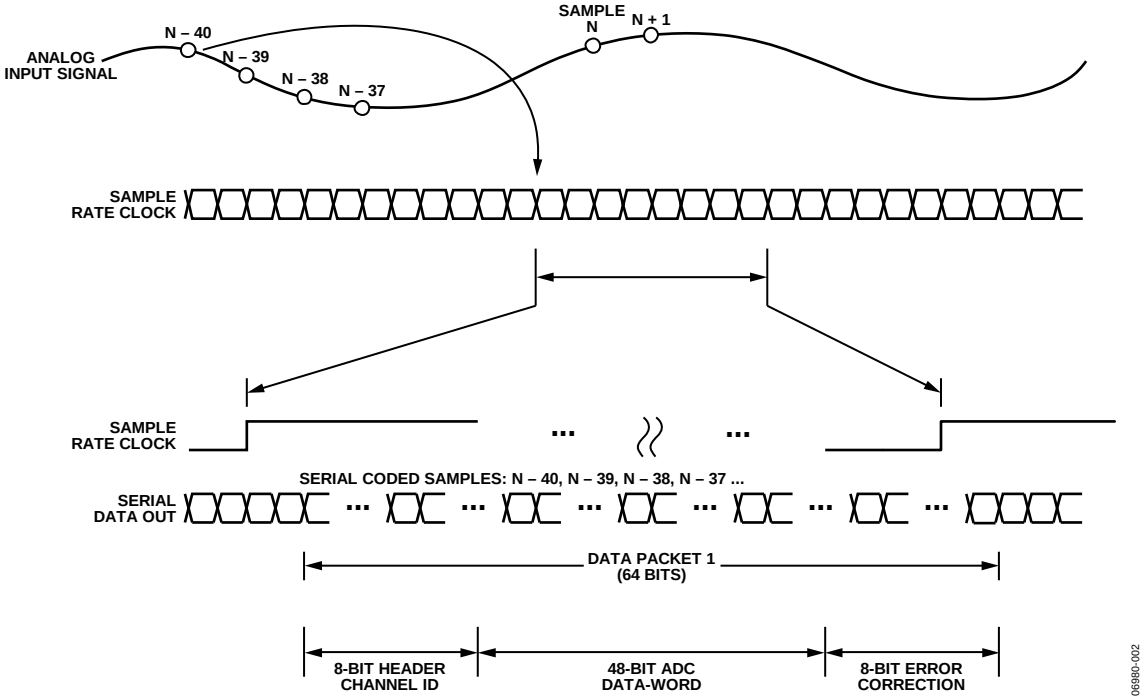

Figure 2. Timing Diagram

Table 5. Packet Protocol

Bits[64:57]	Bits[56:45]	Bits[44:33]	Bits[32:21]	Bits[20:9]	Bits[8:1]
Header (8 bits MSB first)	Data 1 (12 bits MSB first)	Data 2 (12 bits MSB first)	Data 3 (12 bits MSB first)	Data 4 (12 bits MSB first)	ECC (8 bits MSB first)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +2.0 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−2.0 V to +2.0 V
DOUT ± x to DRGND	−0.3 V to DRVDD + 0.3 V
SDO, SDI/SDIO, CLK± , VIN ± x, VCMx, TEMPOUT, RBIAS to AGND	−0.3 V to AVDD + 0.3 V
SCLK, CSB, PGMx, RESET, PDWN to AGND	−0.3 V to AVDD + 0.3 V
Environmental	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
72-Lead LFCSP (CP-72-3)	16.2	7.9	0.6	°C/W

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces and through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

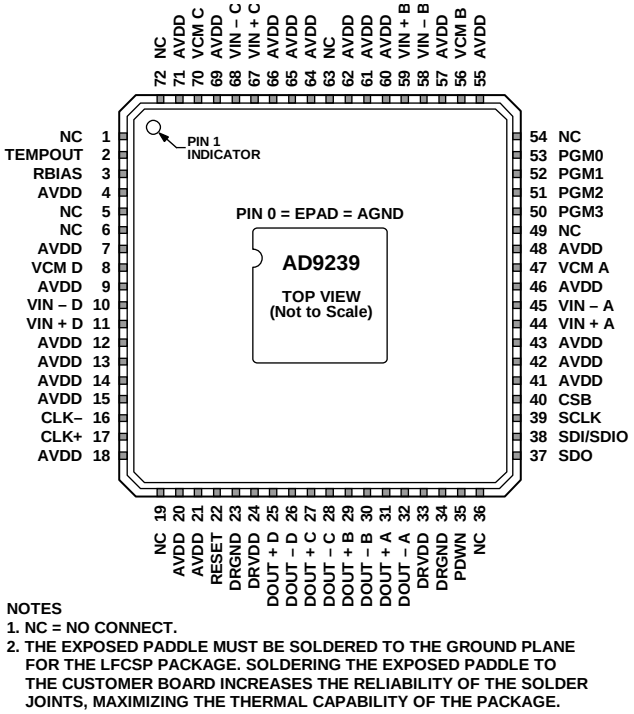

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND	Analog Ground (Exposed Paddle).
23, 34	DRGND	Digital Output Driver Ground.
4, 7, 9, 12, 13, 14, 15, 18, 20, 21, 41, 42, 43, 46, 48, 55, 57, 60, 61, 62, 64, 65, 66, 69, 71	AVDD	1.8 V Analog Supply.
24, 33	DRVDD	1.8 V Digital Output Driver Supply.
2	TEMPOUT	Output Voltage to Monitor Temperature.
3	RBIAS	External Resistor to Set the Internal ADC Core Bias Current.
8	VCM D	Common-Mode Output Voltage Reference.
10	VIN – D	ADC D Analog Complement.
11	VIN + D	ADC D Analog True.
16	CLK–	Input Clock Complement.
17	CLK+	Input Clock True.
22	RESET	Digital Output Timing Reset.
25	DOUT + D	ADC D True Digital Output.
26	DOUT – D	ADC D Complement Digital Output.
27	DOUT + C	ADC C True Digital Output.
28	DOUT – C	ADC C Complement Digital Output.
29	DOUT + B	ADC B True Digital Output.
30	DOUT – B	ADC B Complement Digital Output.
31	DOUT + A	ADC A True Digital Output.
32	DOUT – A	ADC A Complement Digital Output.
35	PDWN	Power-Down.

Pin No.	Mnemonic	Description
37	SDO	Serial Data Output. Used for 4-wire SPI interface.
38	SDI/SDIO	Serial Data Input/Serial Data IO for 3-Wire SPI Interface.
39	SCLK	Serial Clock.
40	CSB	Chip Select Bar.
44	VIN + A	ADC A Analog Input True.
45	VIN − A	ADC A Analog Input Complement.
47	VCM A	Common-Mode Output Voltage Reference.
50	PGM3	Optional Pin to be Programmed by Customer.
51	PGM2	Optional Pin to be Programmed by Customer.
52	PGM1	Optional Pin to be Programmed by Customer.
53	PGM0	Optional Pin to be Programmed by Customer.
56	VCM B	Common-Mode Output Voltage Reference.
58	VIN − B	ADC B Analog Input Complement.
59	VIN + B	ADC B Analog Input True.
67	VIN + C	ADC C Analog Input True.
68	VIN − C	ADC C Analog Input Complement.
70	VCM C	Common-Mode Output Voltage Reference.
1, 5, 6, 19, 36, 49, 54, 63, 72	NC	No Connection.

TYPICAL PERFORMANCE CHARACTERISTICS

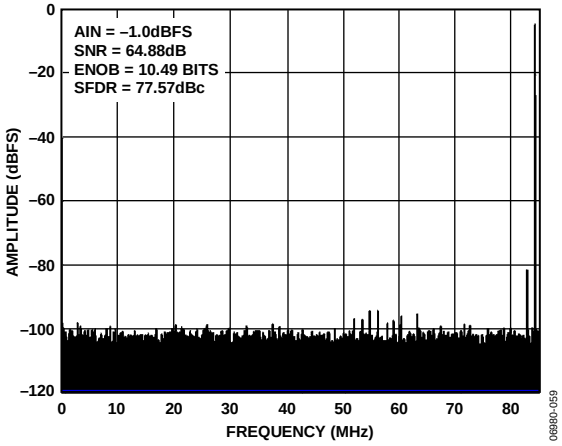

Figure 4. Single-Tone 32k FFT with f_{IN} = 84.3 MHz, f_{SAMPLE} = 170 MSPS

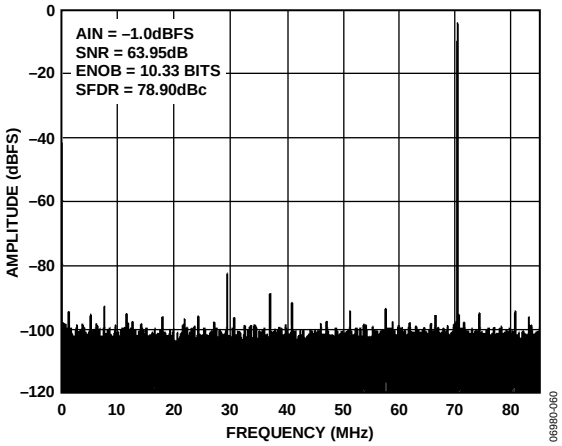

Figure 5. Single-Tone 32k FFT with f_{IN} = 240.3 MHz, f_{SAMPLE} = 170 MSPS

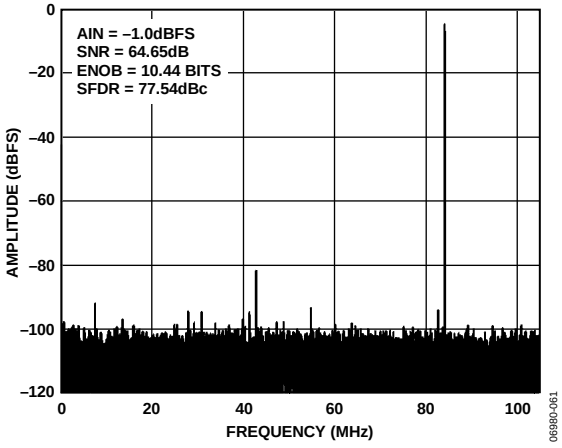

Figure 6. Single-Tone 32k FFT with f_{IN} = 84.3 MHz, f_{SAMPLE} = 210 MSPS

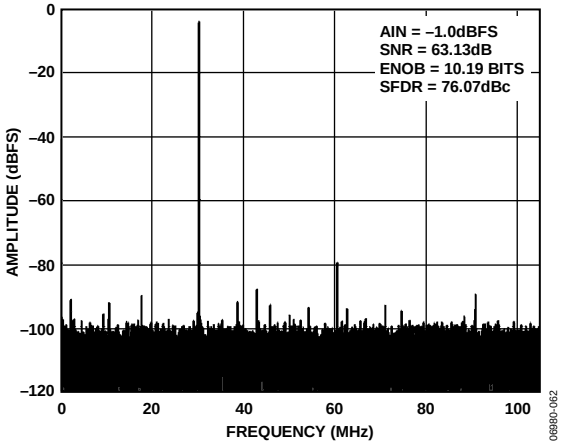

Figure 7. Single-Tone 32k FFT with f_{IN} = 240.3 MHz, f_{SAMPLE} = 210 MSPS

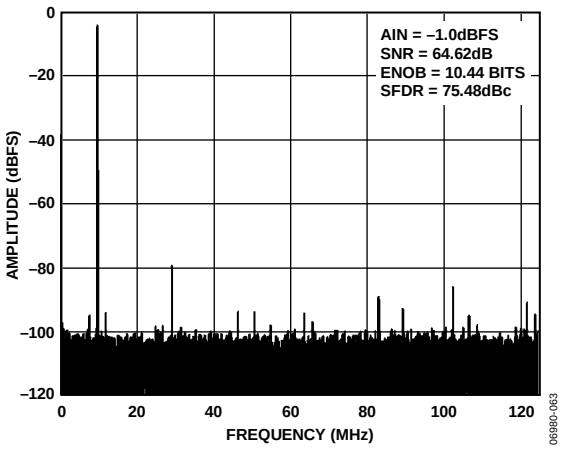

Figure 8. Single-Tone 32k FFT with f_{IN} = 10.3 MHz, f_{SAMPLE} = 250 MSPS

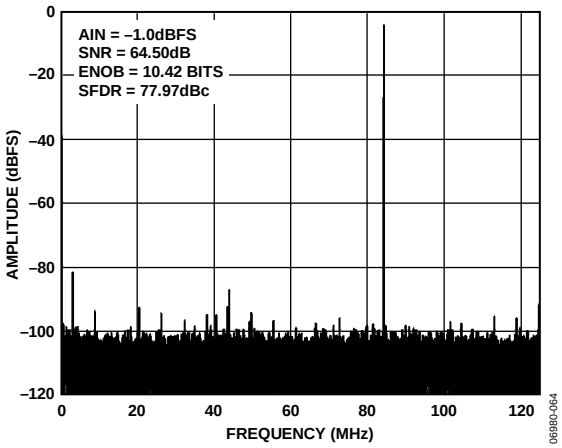

Figure 9. Single-Tone 32k FFT with f_{IN} = 84.3 MHz, f_{SAMPLE} = 250 MSPS

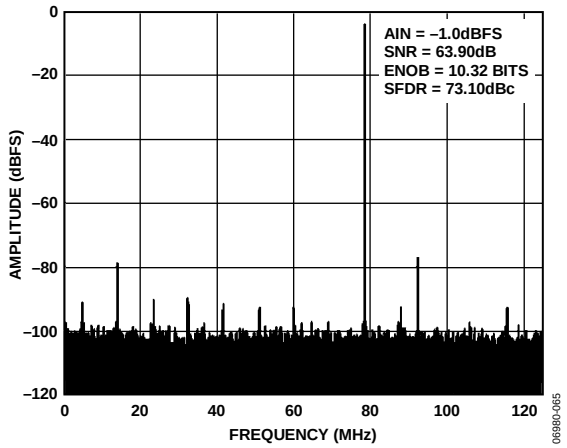

Figure 10. Single-Tone 32k FFT with f_{IN} = 171.3 MHz, f_{SAMPLE} = 250 MSPS

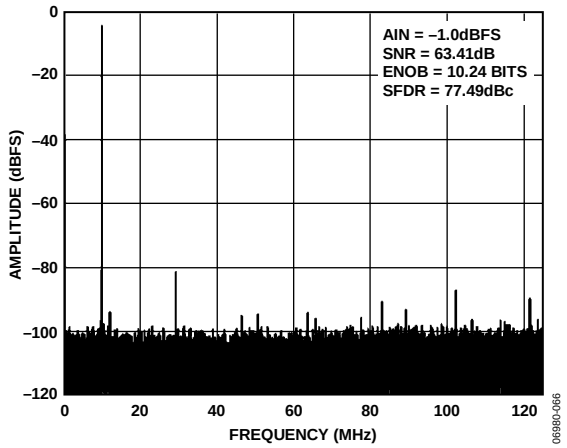

Figure 11. Single-Tone 32k FFT with f_{IN} = 240.3 MHz, f_{SAMPLE} = 250 MSPS

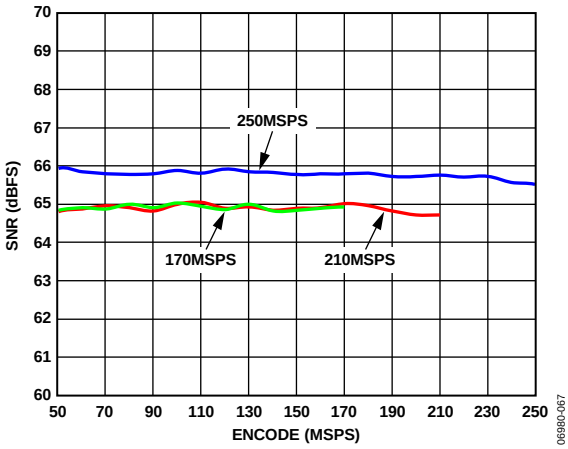

Figure 12. SNR vs. Encode, f_{IN} = 84.3 MHz

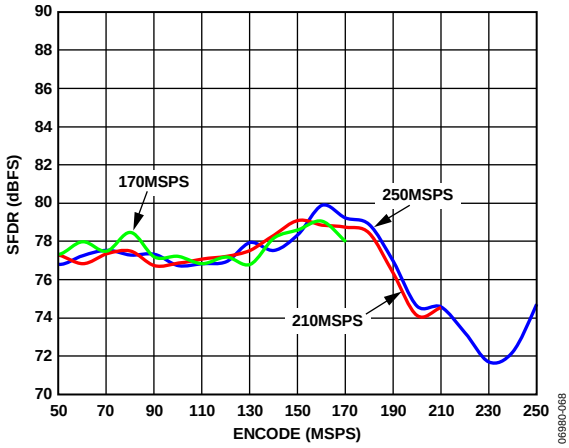

Figure 13. SFDR vs. Encode, f_{IN} = 84.3 MHz

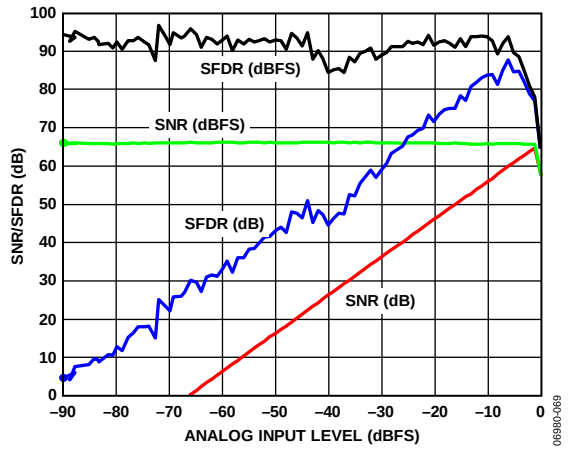

Figure 14. SNR/SFDR vs. Analog Input Level, f_{IN} = 84.3 MHz, f_{SAMPLE} = 170 MSPS

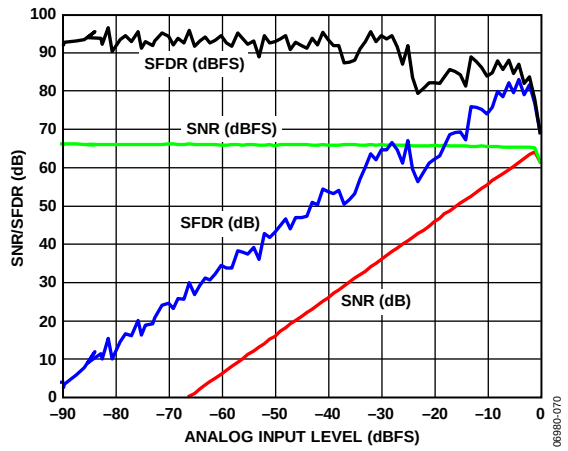

Figure 15. SNR/SFDR vs. Analog Input Level, f_{IN} = 84.3 MHz, f_{SAMPLE} = 210 MSPS

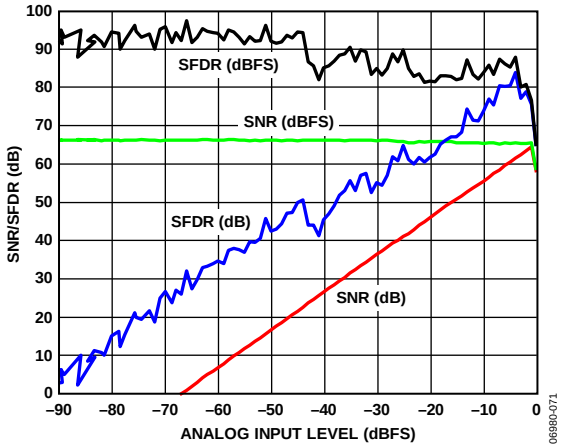

Figure 16. SNR/SFDR vs. Analog Input Level, f_{IN} = 84.3 MHz, f_{SAMPLE} = 250 MSPS

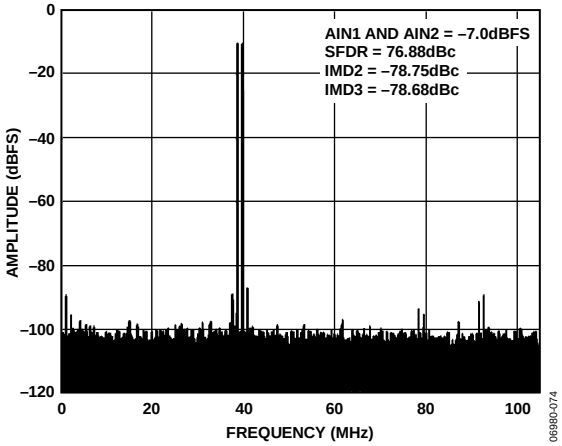

Figure 19. Two-Tone 32k FFT with f_{IN1} = 170.2 MHz and f_{IN2} = 171.3 MHz, f_{SAMPLE} = 2 10 MSPS

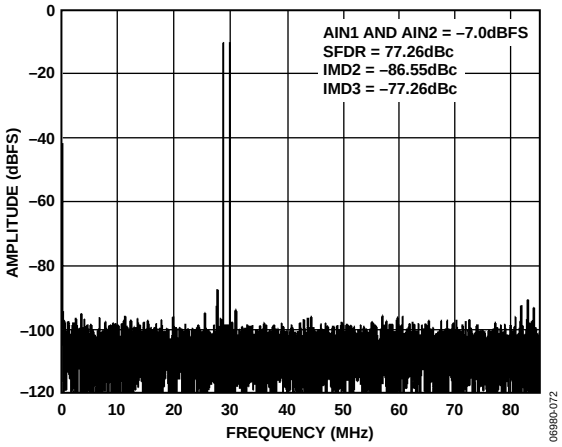

Figure 17. Two-Tone 32k FFT with f_{IN1} = 140.2 MHz and f_{IN2} = 141.3 MHz, f_{SAMPLE} = 170 MSPS

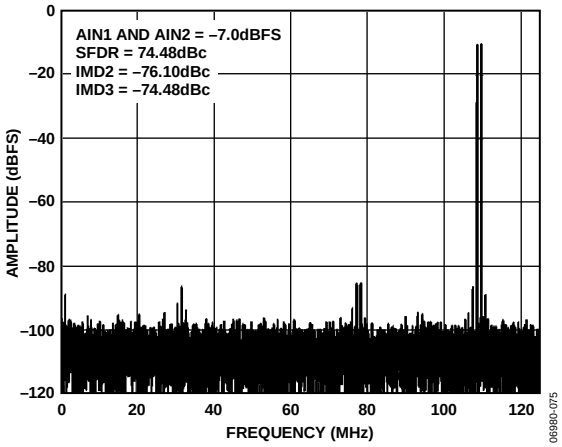

Figure 20. Two-Tone 32k FFT with f_{IN1} = 140.2 MHz and f_{IN2} = 141.3 MHz, f_{SAMPLE} = 250 MSPS

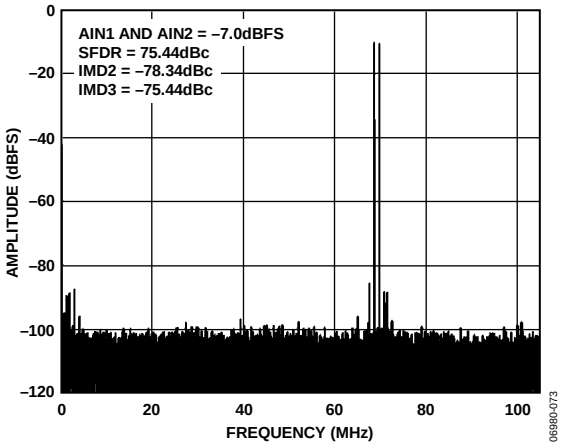

Figure 18. Two-Tone 32k FFT with f_{IN1} = 140.2 MHz and f_{IN2} = 141.3 MHz, f_{SAMPLE} = 210 MSPS

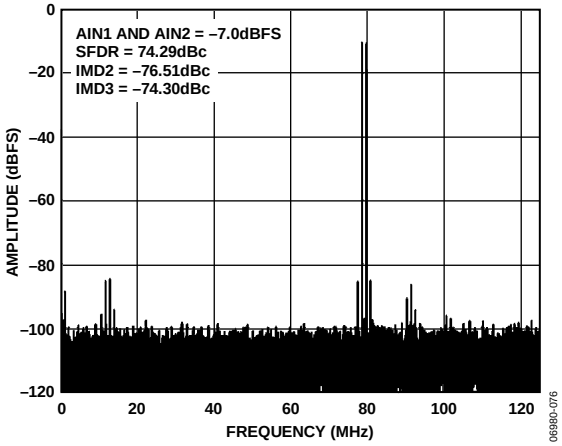

Figure 21. Two-Tone 32k FFT with f_{IN1} = 170.2 MHz and f_{IN2} = 171.3 MHz, f_{SAMPLE} = 250 MSPS

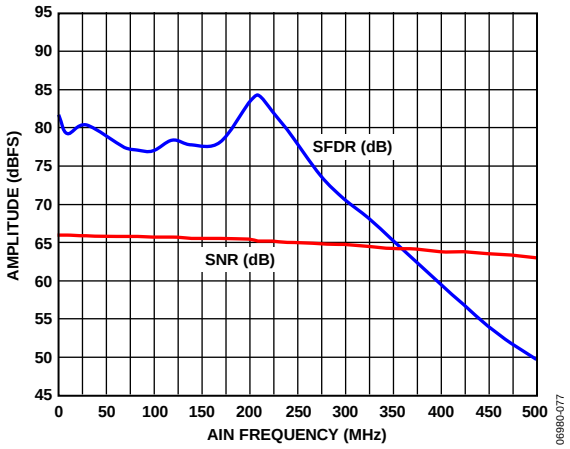

Figure 22. SNR/SFDR Amplitude vs. AIN Frequency, f_{SAMPLE} = 170 MSPS

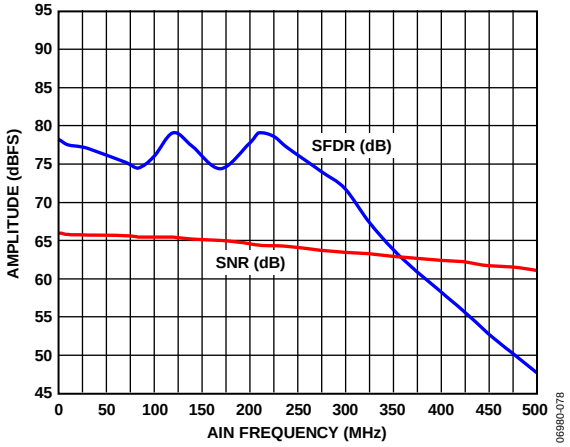

Figure 23. SNR/SFDR Amplitude vs. AIN Frequency, f_{SAMPLE} = 210 MSPS

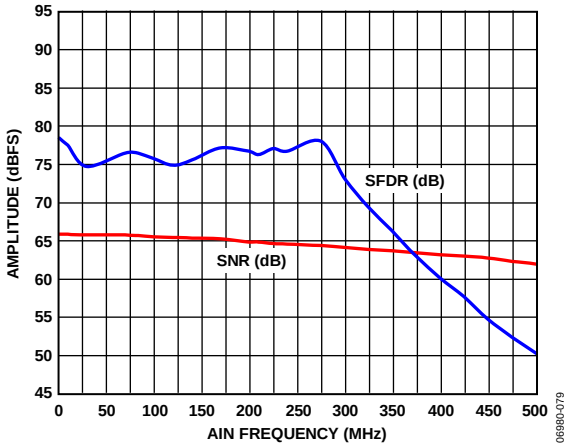

Figure 24. SNR/SFDR Amplitude vs. AIN Frequency, f_{SAMPLE} = 250 MSPS

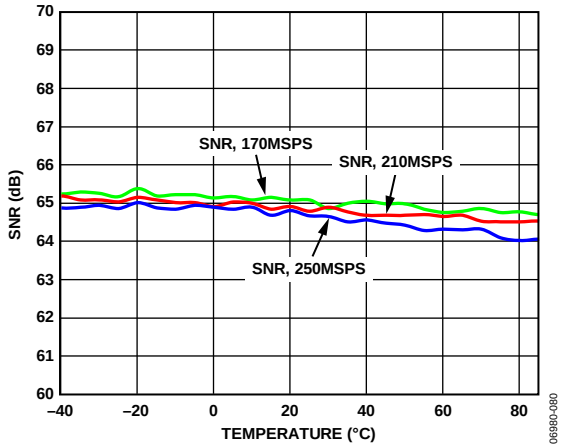

Figure 25. SNR vs. Temperature, f_{IN} = 84.3 MHz

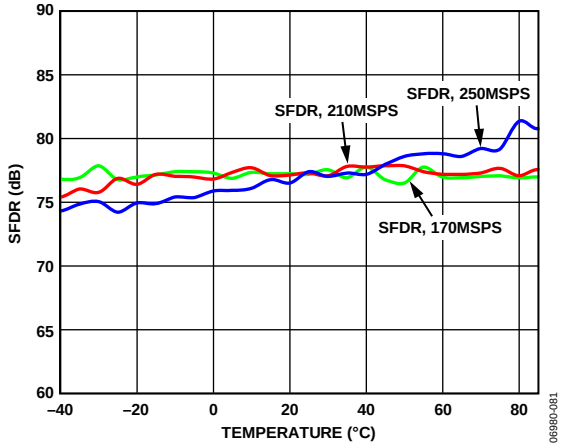

Figure 26. SFDR vs. Temperature, f_{IN} = 84.3 MHz

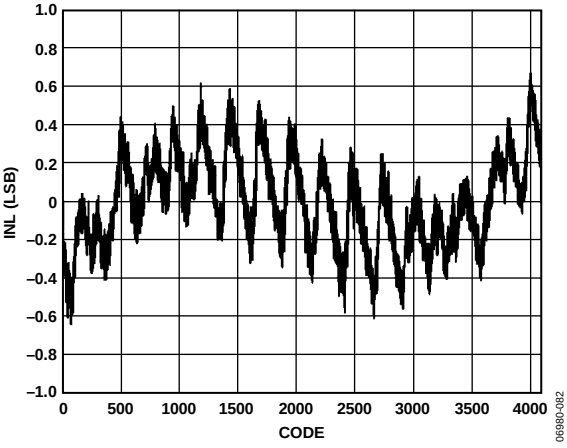

Figure 27. INL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 250 MSPS

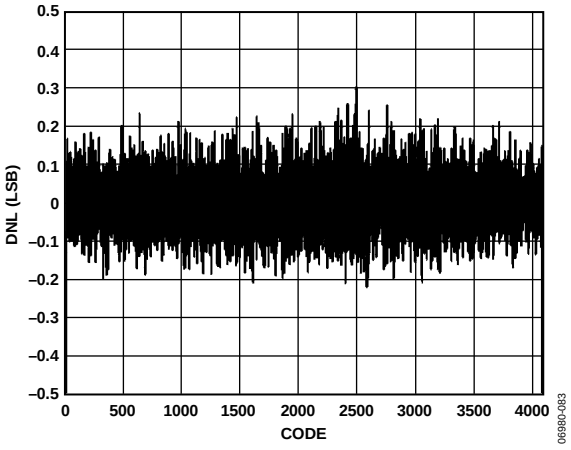

Figure 28. DNL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 250 MSPS

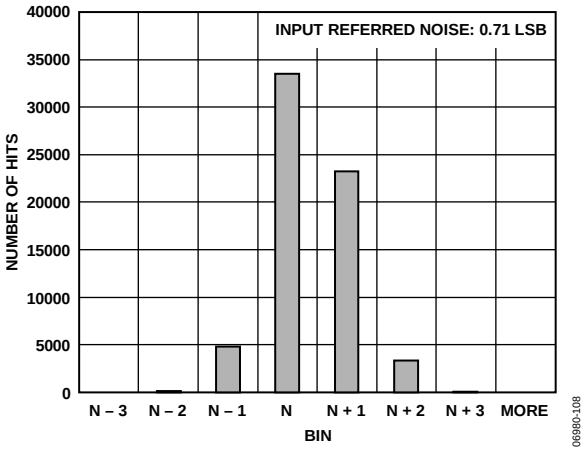

Figure 31. Input-Referred Noise Histogram, f_{SAMPLE} = 250 MSPS

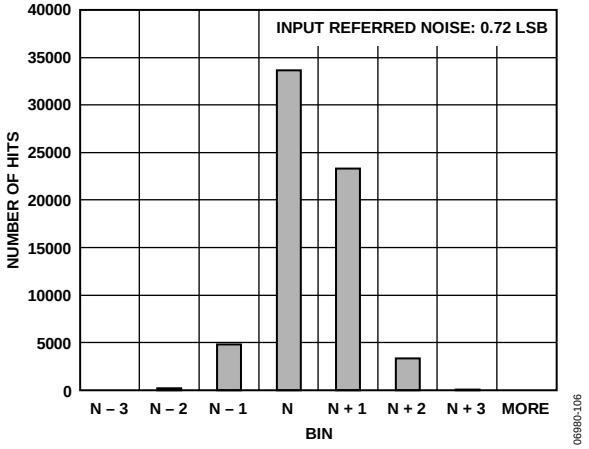

Figure 29. Input-Referred Noise Histogram, f_{SAMPLE} = 170 MSPS

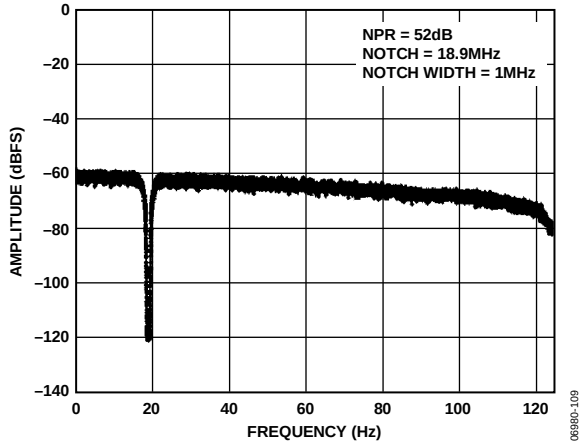

Figure 32. Noise Power Ratio (NPR), f_{SAMPLE} = 250 MSPS

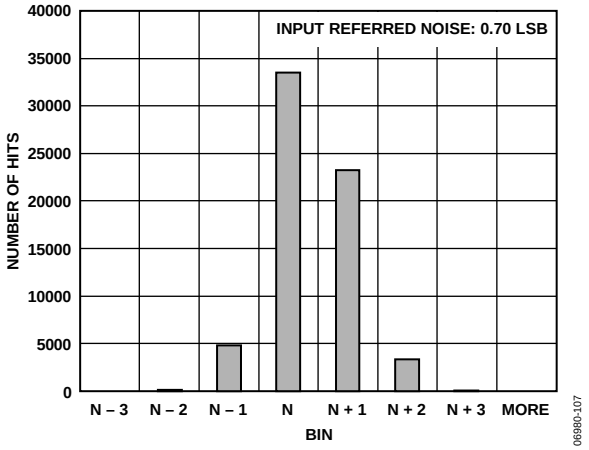

Figure 30. Input-Referred Noise Histogram, f_{SAMPLE} = 210 MSPS

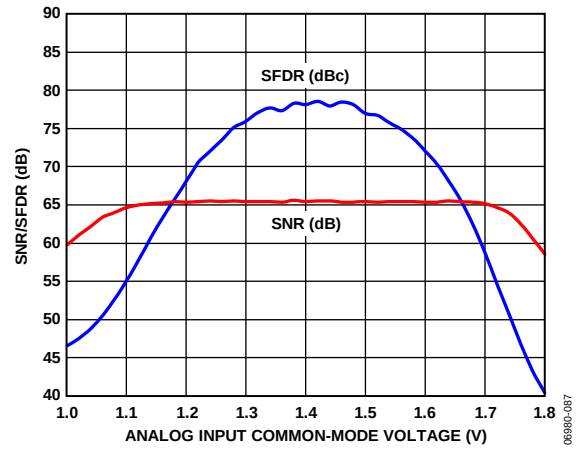

Figure 33. SNR/SFDR vs. Analog Input Common-Mode Voltage, f_{IN} = 84.3 MHz, f_{SAMPLE} = 250 MSPS

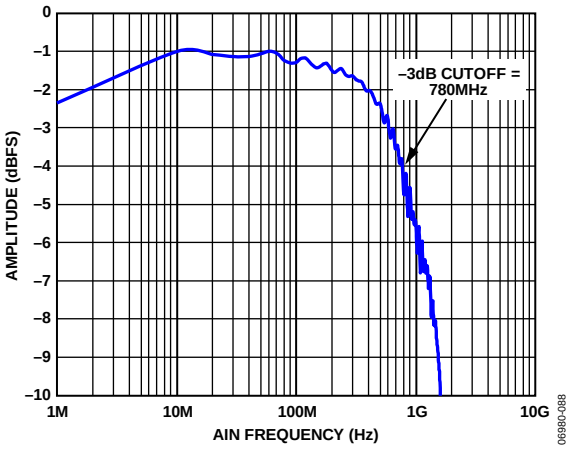

Figure 34. Full-Power Bandwidth Amplitude vs. AIN Frequency, f_{SAMPLE} = 250 MSPS

EQUIVALENT CIRCUITS

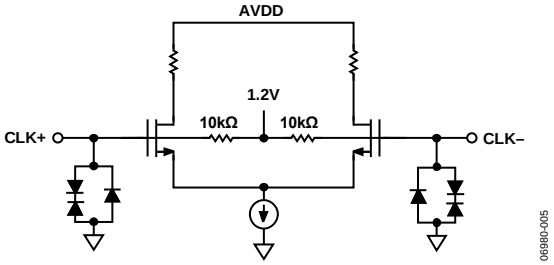

Figure 35. CLK± Inputs

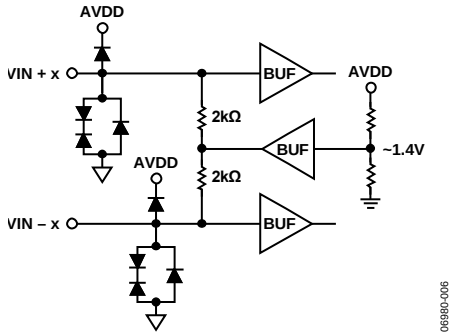

Figure 36. Analog Inputs

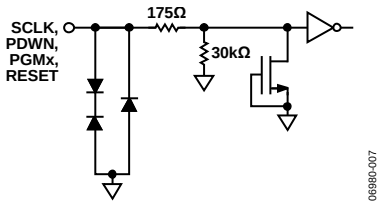

Figure 37. Equivalent SCLK, PDWN, PGMx, RESET Input Circuit

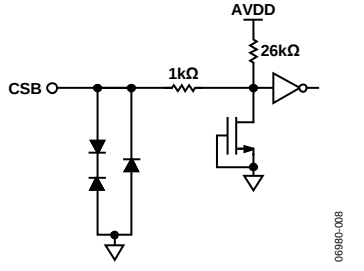

Figure 38. Equivalent CSB Input Circuit

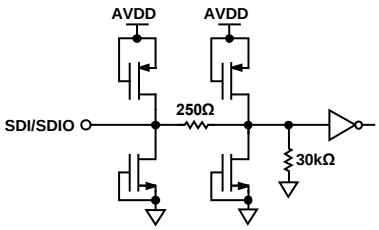

Figure 39. Equivalent SDI/SDIO Input Circuit

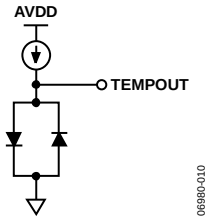

Figure 40. Equivalent TEMPOUT Output Circuit

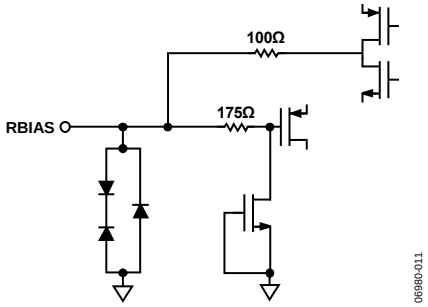

Figure 41. Equivalent RBIAS Input/Output Circuit

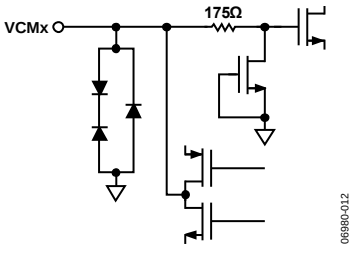

Figure 42. Equivalent VCMx Output Circuit

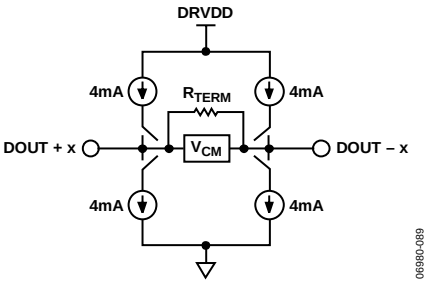

Figure 43. Equivalent Digital Output Circuit

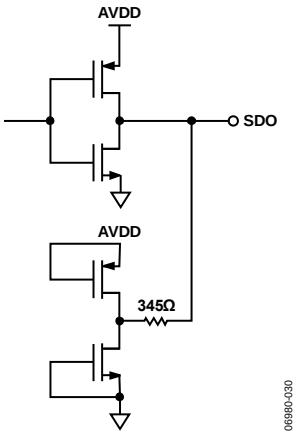

Figure 44. Equivalent SDO Output Circuit

THEORY OF OPERATION

The AD9239 architecture consists of a differential input buffer, front-end sample-and-hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended mode. The output of the pipeline ADC is put into its final serial format by the data serializer, encoder, and CML drivers block. The data rate multiplier creates the clock used to output the high speed serial data at the CML outputs.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9239 is a differential buffer. This input is optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance degrades if the analog input is driven with a single-ended signal.

For best dynamic performance, the source impedances driving VIN + x and VIN − x should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source.

In addition, low-Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of low-Q inductors or ferrite beads is required when driving the converter front end at high intermediate frequency (IF). Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-827 Application Note and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information on this subject. In general, the precise values depend on the application.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9239, the default input span is 1.25 V p-p. To configure the ADC for a different input span, see Register 18. For the best performance, an input span of 1.25 V p-p or greater should be used (see Table 15 for details).

Differential Input Configurations

There are several ways to drive the AD9239 either actively or passively; in either case, optimum performance is achieved by driving the analog input differentially. For example, using the ADA4937 differential amplifier to drive the AD9239 provides excellent performance and a flexible interface to the ADC (see Figure 45 and Figure 46) for baseband and second Nyquist (~100 MHz IF) applications. In either application, 1% resistors should be used for good gain matching. It should also be noted that the dc-coupled configuration will show some degradation in spurious performance. For further reference, consult the ADA4937 data sheet.

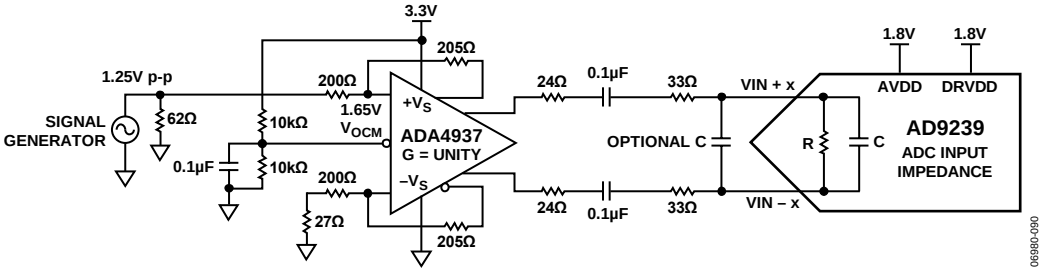

Figure 45. Differential Amplifier Configuration for AC-Coupled Baseband Applications

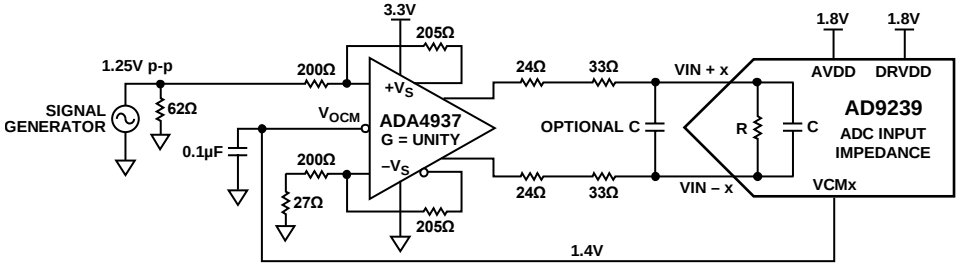

Figure 46. Differential Amplifier Configuration for DC-Coupled Baseband Applications

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 47 to Figure 49), to achieve the true performance of the AD9239.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

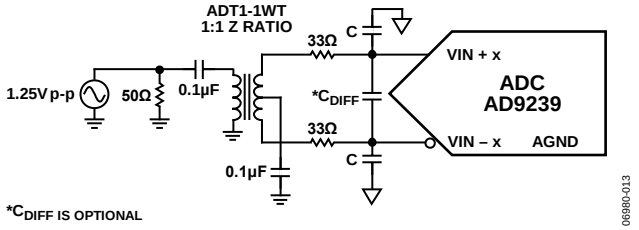

Figure 47. Differential Transformer-Coupled Configuration for Baseband Applications

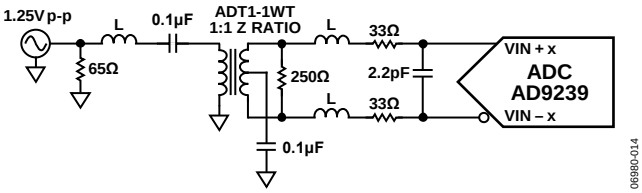

Figure 48. Differential Transformer-Coupled Configuration for Wideband IF Applications

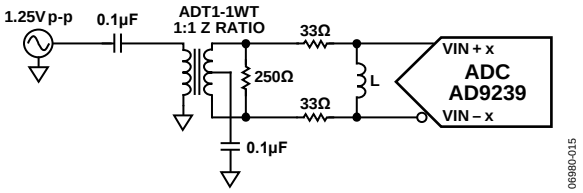

Figure 49. Differential Transformer-Coupled Configuration for Narrow-Band IF Applications

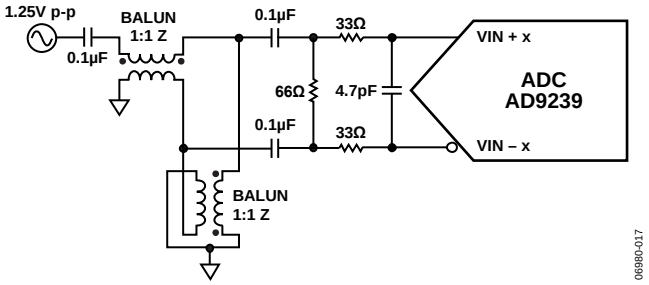

Figure 50. Differential Balun-Coupled Configuration for Wideband IF Applications

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance can degrade due to input common-mode swing mismatch. If the application requires a single-ended input configuration, ensure that the source impedances on each input are well matched in order to achieve the best possible performance. A full-scale input of 1.25 V p-p can be applied to the ADC's VIN + x pin while the VIN – x pin is terminated. Figure 51 details a typical single-ended input configuration.

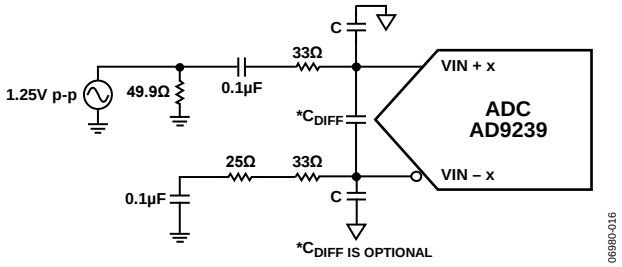

Figure 51. Single-Ended Input Configuration

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9239 sample clock inputs (CLK+ and CLK–) should be clocked with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally to 1.2 V and require no additional biasing.

Figure 52 shows a preferred method for clocking the AD9239. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9239 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9239, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

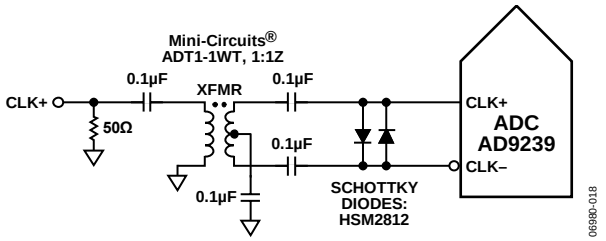

Figure 52. Transformer-Coupled Differential Clock

Another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 53. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9518 family of clock drivers offers excellent jitter performance.

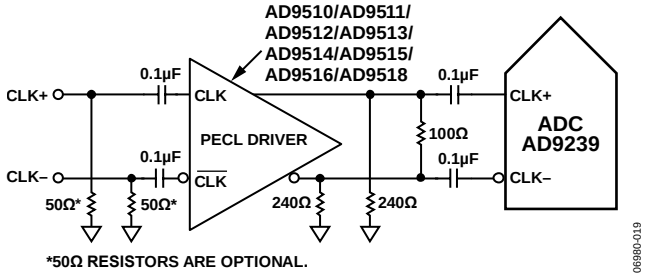

Figure 53. Differential PECL Sample Clock

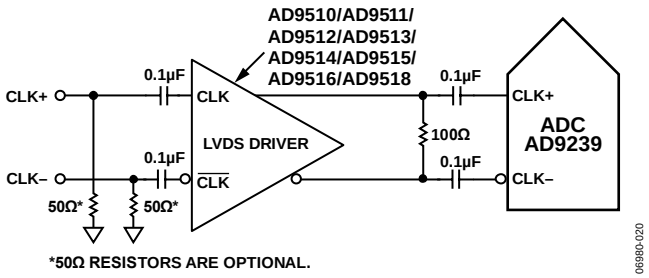

Figure 54. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be driven directly from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 55). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages of up to 3.3 V and therefore offers several selections for the drive logic voltage.

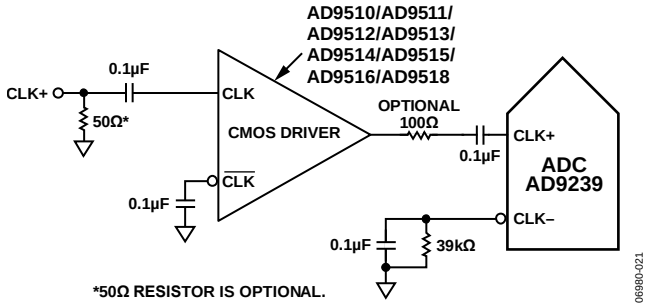

Figure 55. Single-Ended 1.8 V CMOS Sample Clock

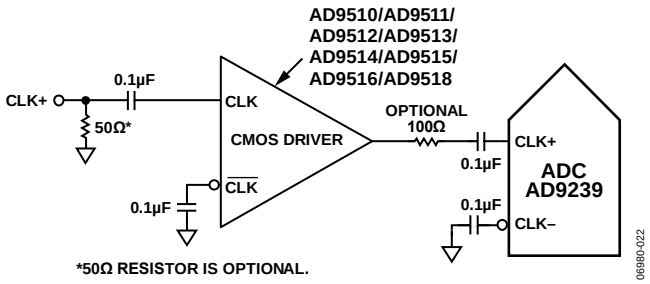

Figure 56. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9239 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9239. When the DCS is on (default), noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance may be affected when operated in this mode. See the Memory Map section for more details on using this feature.

Jitter in the rising edge of the input is an important concern, and it is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 50 MHz nominal. It is not recommended that this ADC clock be dynamic in nature. Moving the clock around dynamically requires long wait times for the back end serial capture to retime and resynchronize to the receiving logic. This long time constant far exceeds the time it takes for the DCS and PLL to lock and stabilize. Only in rare applications would it be necessary to disable the DCS circuitry of Register 9 (see Table 15). Keeping the DCS circuit enabled is recommended to maximize ac performance.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \times \log 10(1/2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (see Figure 57).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9239. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators are the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock during the last step.

Refer to the AN-501 Application Note, the AN-756 Application Note, and the *Analog Dialogue* article "Analog-to-Digital Converter Clock Optimization: A Test Engineering Perspective" (Volume 42, Number 2, February 2008) for more in-depth information about jitter performance as it relates to ADCs (visit www.analog.com).

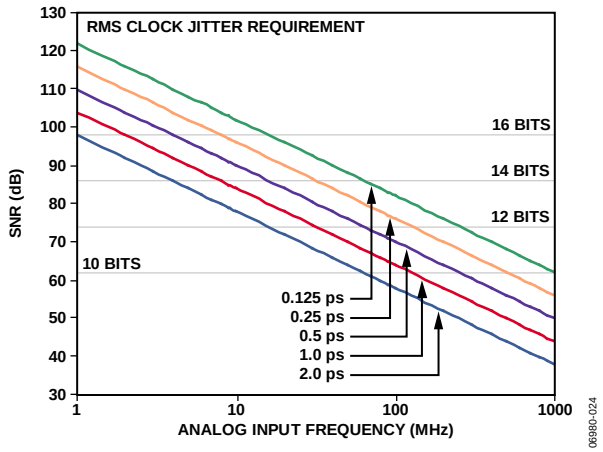

Figure 57. Ideal SNR vs. Input Frequency and Jitter

Power Dissipation

As shown in Figure 58 to Figure 60, the power dissipated by the AD9239 is proportional to its clock rate. The digital power dissipation does not vary significantly because it is determined primarily by the DRVDD supply and bias current of the digital output drivers.

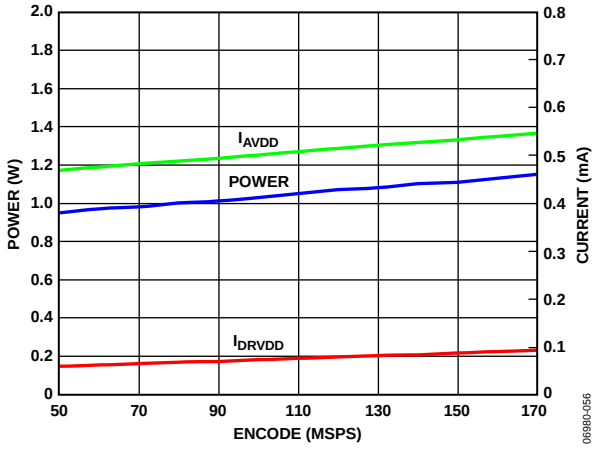

Figure 58. Supply Current vs. Encode for f_{IN} = 84.3 MHz, f_{SAMPLE} = 170 MSPS

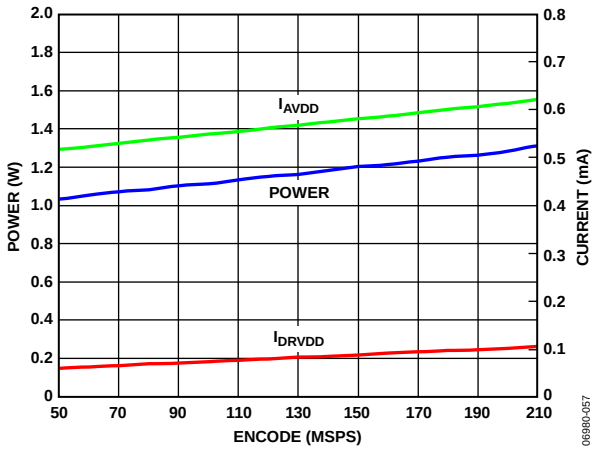

Figure 59. Supply Current vs. Encode for f_{IN} = 84.3 MHz, f_{SAMPLE} = 210 MSPS

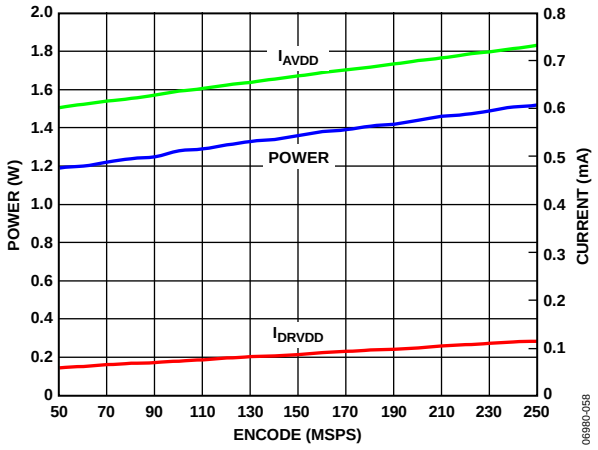

Figure 60. Supply Current vs. Encode for f_{IN} = 84.3 MHz, f_{SAMPLE} = 250 MSPS

Digital Start-Up Sequence

The output digital data from the AD9239 is coded and packetized, which requires the device to have a certain start-up sequence. The following steps should be initialized by the user to capture coherent data at the receiving logic.

1. Initialize a soft reset via Bit 5 of Register 0 (see Table 15).
2. All PGMx pins are automatically initialized as sync pins by default. These pins can be used to lock the FPGA timing and data capture during initial startup. These pins are respective to each channel (PGM3 = Channel A).
3. Each sync pin is held low until its respective PGMx pin receives a high signal input from the receiver, during which time the ADC outputs a training pattern.
4. The training pattern defaults to the values implemented by the user in Register 19 through Register 20.
5. When the receiver finds the frame boundary, the sync identification is deasserted high via the sync pin or via a SPI write. The ADC outputs the valid data on the next packet boundary. The time necessary for sync establishment is highly dependent on the receiver logic processing. Refer to the Switching Specifications section; the switching timing is directly related to the ADC channel.
6. Once steady state operation for the device has occurred, these pins can each be assigned to be a standby option by using Register 53 (see Table 15). All other pins act as universal sync pins.

To minimize skew and time misalignment between each channel of the digital outputs, the following actions should be taken to ensure that each channel data packet is within ±1 clock cycle of its specified switching time. For some receiver logic, this is not required.

1. Full power-down through external PDWN pin.
2. Chip reset via external RESET pin.
3. Power back up by releasing external PDWN pin.

Digital Outputs and Timing

The AD9239 has differential digital outputs that power up on default. The driver current is derived on chip and sets the output current at each output equal to a nominal 4 mA. Each output presents a 100 Ω dynamic internal termination to reduce unwanted reflections.

A 100 Ω differential termination resistor should be placed at each receiver input to result in a nominal 400 mV p-p swing at the receiver. Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage should be DRVDD/2; otherwise, ac coupling capacitors can be used to terminate to any single-ended voltage.

The AD9239 digital outputs can interface with custom application-specific integrated circuits (ASICs) and field-programmable gate array (FPGA) receivers, providing superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver logic as possible. The common mode of the digital output automatically biases itself to half the supply of DRVDD if dc-coupled connecting is used. For receiver logic that is not within the bounds of the DRVDD supply, an ac-coupled connection should be used. Simply place a 0.1 µF capacitor on each output pin and derive a 100 Ω differential termination close to the receiver side.

If there is no far-end receiver termination or there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than 6 inches and that the differential output traces be close together and at equal lengths.

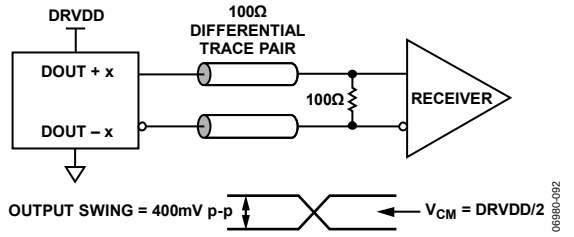

Figure 61. DC-Coupled Digital Output Termination Example

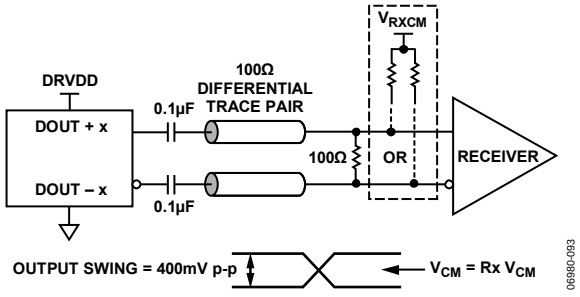

Figure 62. AC-Coupled Digital Output Termination Example

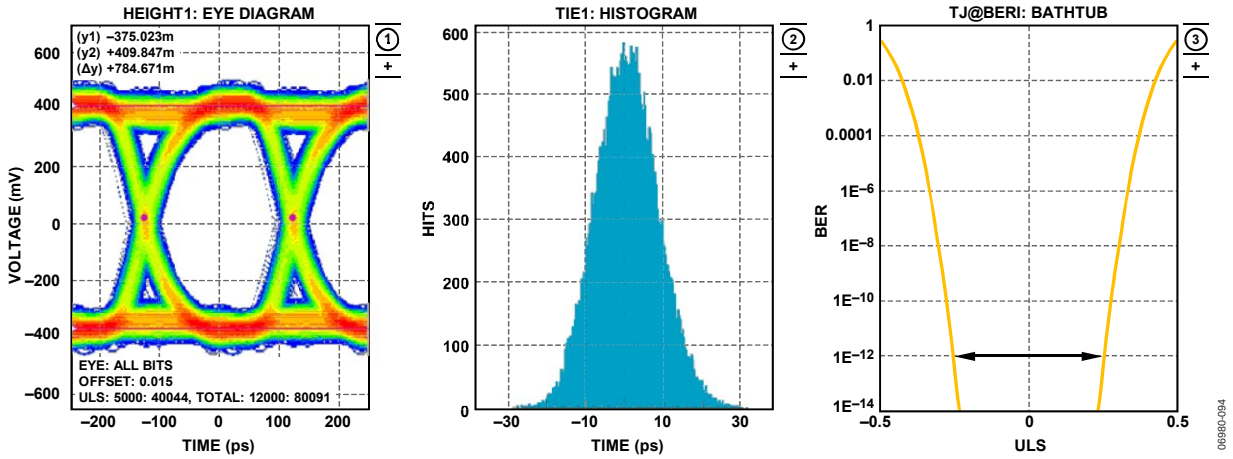

Figure 63. Digital Outputs Data Eye with Trace Lengths Less than 6 Inches on Standard FR-4, External 100 Ω Terminations at Receiver

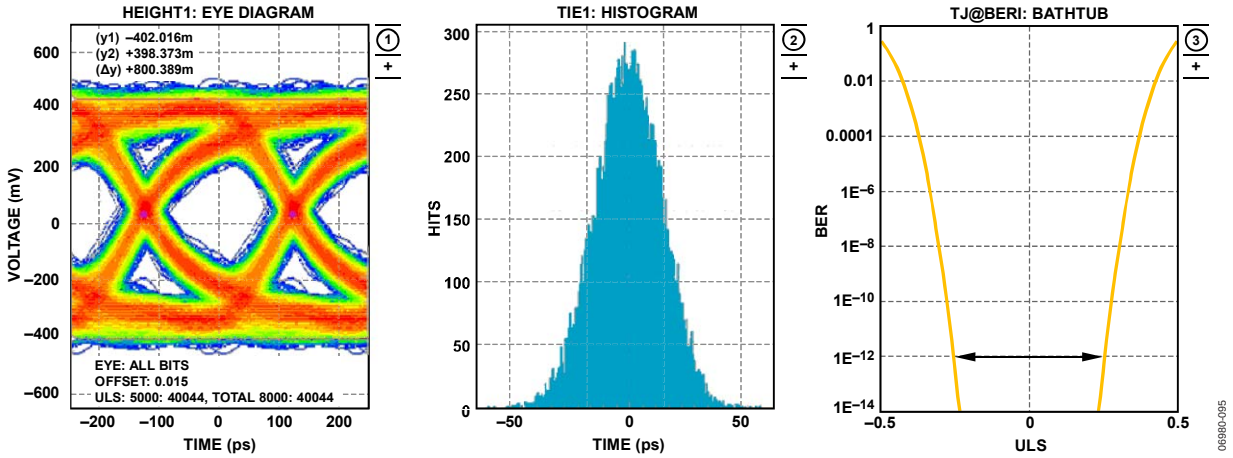

Figure 64. Digital Outputs Data Eye with Trace Lengths Greater than 12 Inches on Standard FR-4, External 100 Ω Terminations at Receiver

An example of the digital output (default) data eye and a time interval error (TIE) jitter histogram with trace lengths less than 6 inches on standard FR-4 material is shown in Figure 63. Figure 64 shows an example of trace lengths exceeding 12 inches on standard FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position. It is the user's responsibility to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 6 inches.

Additional SPI options allow the user to further increase the output driver voltage swing of all four outputs in order to drive longer trace lengths (see Register 15 in Table 15). Even though this produces sharper rise and fall times on the data edges and is less prone to bit errors, the power dissipation of the DRVDD supply increases when this option is used. See the Memory Map section for more details.

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 9.

To change the output data format to twos complement or gray code, see the Memory Map section.

Table 9. Digital Output Coding

Code	(VIN + x) − (VIN − x), Input Span = 1.25 V p-p (V)	Digital Output Offset Binary (D11 ... D0)
4095	+0.625	1111 1111 1111
2048	0.00	1000 0000 0000
2047	−0.000305	0111 1111 1111
0	−0.625	0000 0000 0000

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to N bits times the sample clock rate, in addition to some amount of overhead to account for the 8-bit header and error correction, for a maximum of 3.36 Gbps (that is, 12 bits × 210 MSPS × 64/48 = 3.36 Gbps). The lowest typical clock rate is 100 MSPS. For clock rates slower than 100 MSPS, refer to Register 21 in the SPI Memory Map. This option allows the user to adjust the PLL loop bandwidth in order to use clock rates as low as 50 MSPS.

Table 10. Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select
0000	Off (default)	N/A	N/A	Yes
0001	Midscale short	1000 0000 0000	Same	Yes
0010	+Full-scale short	1111 1111 1111	Same	Yes
0011	−Full-scale short	0000 0000 0000	Same	Yes
0100	Checkerboard	1010 1010 1010	0101 0101 0101	No
0101	PN sequence long[1]	N/A	N/A	Yes
0110	PN sequence short[1]	N/A	N/A	Yes
0111	One-/zero-word toggle	1111 1111 1111	0000 0000 0000	No

[1] All test mode options except PN sequence short and PN sequence long can support 8- to 14-bit word lengths in order to verify data capture to the receiver.

Register 14 allows the user to invert the digital outputs from their nominal state. This is not to be confused with inverting the serial stream to an LSB-first mode. In default mode, as shown in Figure 2, the MSB is first in the data output serial stream. However, this can be inverted so that the LSB is first in the data output serial stream.

There are eight digital output test pattern options available that can be initiated through the SPI. This feature is useful when validating receiver capture and timing. Refer to Table 10 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen. It should be noted that some patterns do not adhere to the data format select option.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. A description of the PN sequence and how it is generated can be found in Section 5.1 of the ITU-T 0.150 (05/96) standard. The only difference is that the starting value must be a specific value instead of all 1s (see Table 11 for the initial values).

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8,388,607 bits. A description of the PN sequence and how it is generated can be found in Section 5.6 of the ITU-T 0.150 (05/96) standard. The only differences are that the starting value must be a specific value instead of all 1s (see Table 11 for the initial values) and the AD9239 inverts the bit stream with relation to the ITU standard.

Table 11. PN Sequence

Sequence	Initial Value	First Three Output Samples (MSB First)
PN Sequence Short	0x0df	0xdf9, 0x353, 0x301
PN Sequence Long	0x29b80a	0x591, 0xfd7, 0x0a3

Consult the Memory Map section for information on how to change these additional digital output timing features through the SPI.

Digital Output Scrambler and Error Code Correction

The data from the AD9239 is sent serially in packets of 64 bits. These numbers are derived from the necessity to have the output data streaming at 16× the encode clock. The data packets consist of a header, data, and error correction code (that is, 8 Bits of Header + 48 Bits of Data (4 Conv.) + 8 Bits of ECC = 64 Bits). The 12-bit protocol is shown in Figure 2 and Table 5.

Error Correction Code

The error correction code (ECC) is a Hamming code due to the ease of implementation. Seven bits are used for the ECC to correct one error or detect one or two errors during transmission.

The MSB of the ECC is always 0 and is not used to detect an error. The six LSBs of the ECC are the result of the XORs of the given bits (see Figure 68 to Figure 75). These bits allow for a parity check for any bit in the header and data field.

The seventh parity bit is applied to the entire packet after the Hamming parity bits are calculated. This parity check allows correction of an error in the data or in the ECC bits.

In the general implementation, the parity bits are located in the power of 2 positions, but are pulled from these locations and placed together at the end of the packet. Figure 68 to Figure 75 show which header and data bits are associated with the parity bits.

In the receiver, these parity checks are performed and the receiver parity bits are calculated. The difference between the received parity bits and the calculated parity bits indicate which bit was in error.

Scramblers

There are three scramblers on the AD9239. The scramblers are an Ethernet scrambler ($x^{58} + x^{39} + 1$), a SONET scrambler ($x^7 + x^6 + 1$), and a static inverter scrambler (inverts bits at set locations in the packet). The scramblers are used to help balance the number of 1s and 0s in the packet.

The Ethernet and SONET scramblers work on scrambling the whole packet (64 bits), the header and the data (56 bits), or just the data (48 bits). The scrambler is self-synchronizing on the descramble end or receive end and does not require an additional sync bit. For a copy of either the Ethernet or SONET scrambler code, send an email to highspeed.converters@analog.com. Figure 65 and Figure 66 show the serial implementation of the Ethernet and SONET scramblers. The parallel implementation allows the scrambler and descrambler to run at a slower clock rate and can be implemented in the fabric of a receiver.

The serial implementations of the Ethernet and SONET scramblers more easily show what is being done. The parallel implementation must be derived from the serial implementation. The end product depends on how many bits need to be processed in parallel. For the scrambler, 64 bits are processed even in the 56- and 48-bit cases. To achieve this for 56 bits and 48 bits, a portion of two samples is used to fill the rest of the input word.

Inverter Balance Example

The inverter implementation uses predetermined bit positions to balance the packet in an overrange condition (all 1s or all 0s) in the converter. The inversions are present in all conditions, not just the overrange condition.

The descrambler can be based off any number of bits the user chooses to process. In the inverter-based scrambler, the packet is balanced based on an overranged condition. If each packet is balanced, the bit stream should be balanced. Instead of a random sequence that changes from packet to packet, certain inverts are set at predetermined bit positions within the packet. This allows the decoding to be done in the receiver end. Figure 67 shows the inverters in the packet for the 12-bit data case and the inverter order in the header.

Table 12 shows the average value of the packet for various conditions.

Table 12. Average of 1s and 0s in Overrange Conditions

Assuming Header Bits are All 0	12-Bit	ECC
No Scramble (Data = 0)	0	00000000
No Scramble (Data = 1)	0.844	00111111
Average of Negative and Positive Overrange	0.422	
Scramble Only Data (Data = 0)	0.375	00000000
Scramble Only Data (Data = 1)	0.469	00111111
Average of Negative and Positive Overrange	0.422	
Scramble Data and Header (Data = 0)	0.437	00000000
Scramble Data and Header (Data = 1)	0.531	00111111
Average of Negative and Positive Overrange	0.484	

If the analog signal is out of range, there should be about the same number of out-of-range positive and out-of-range negative values. The average for no scrambling and for scrambling just the data is about the same. If the header is used to indicate out of range, the balance improves for the 12-bit case.

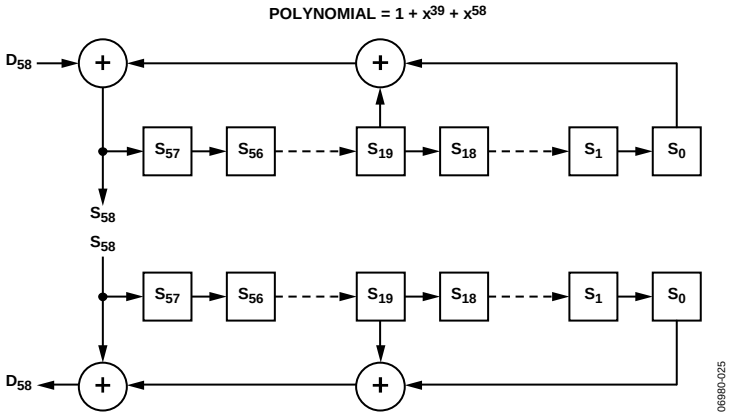

Figure 65. Serial Implementation of Ethernet Scrambler

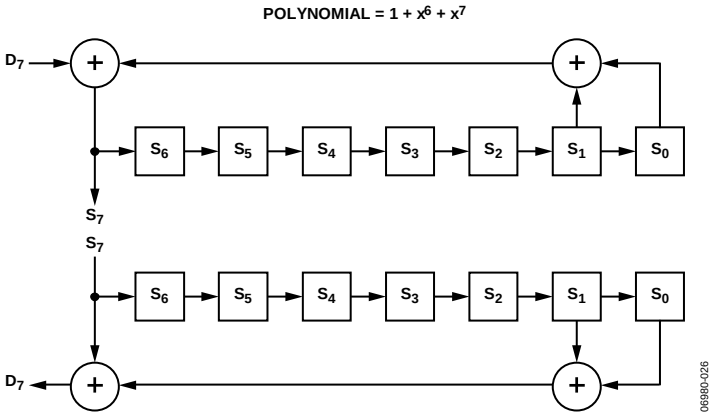

Figure 66. Serial Implementation of SONET Scrambler

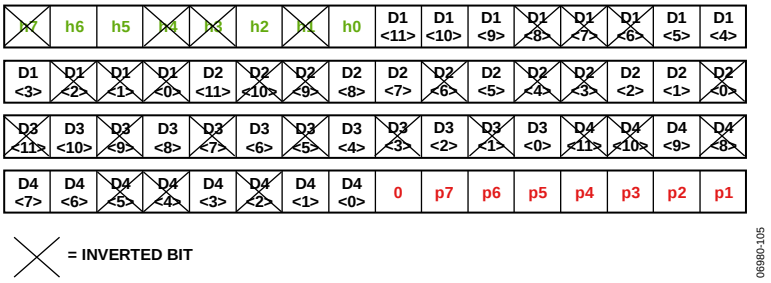

Figure 67. Scrambler Inverters for 64-Bit Packet: 12-Bit Case

Calculating the Parity Bits for the Hamming Code

The Hamming bits are defined as follows. The definition is shown in the charts for a 12-bit example. The Hamming parity bits are shown interleaved in the data. This makes it easier to see the numeric relationship. The decoding on the receive side is just the inversion. A separate document will show the proper way to correct an error in the transmission.

The p8 bit (MSB of the parity bits) will always be 0. The p7 bit is a parity bit for the entire packet after the other parity bits are calculated.

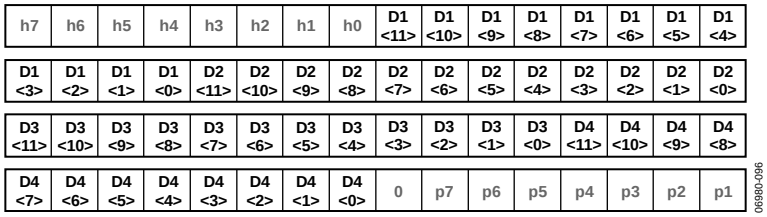

Figure 68. 64-Bit Packet: 12-Bit Case

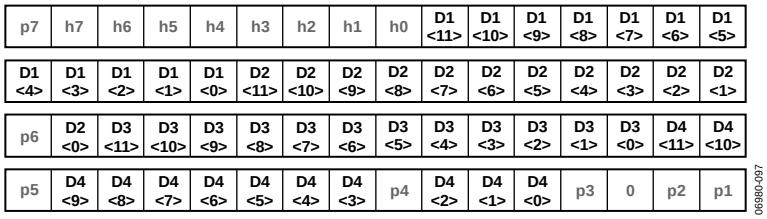

Figure 69. 64-Bit Packet Hamming Template for 12-Bit Case

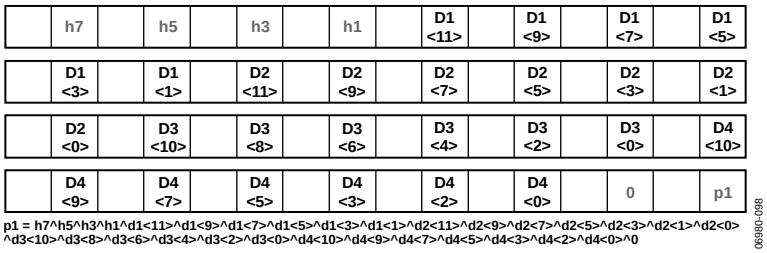

Figure 70. p1 Bit for 64-Bit Packet: 12-Bit Case

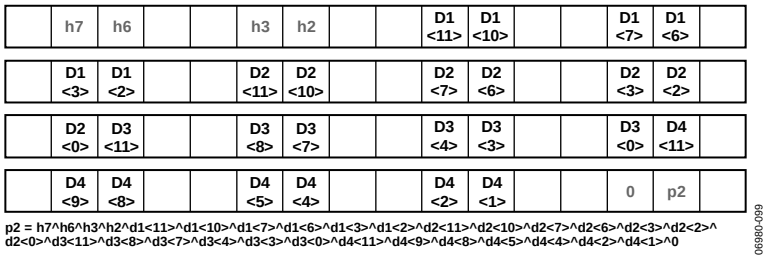

Figure 71. p2 Bit for 64-Bit Packet: 12-Bit Case

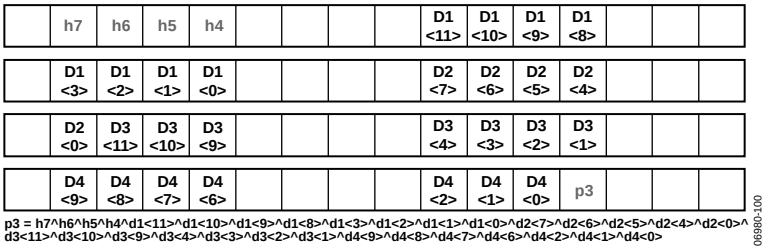

Figure 72. p3 Bit for 64-Bit Packet: 12-Bit Case

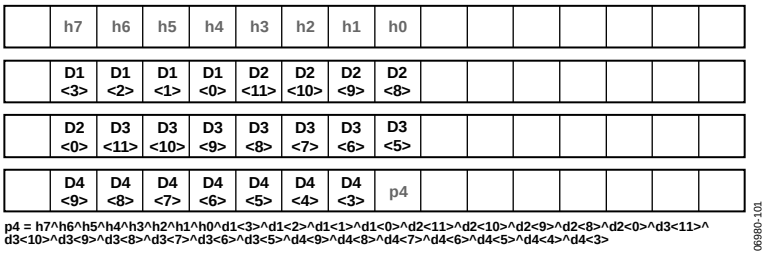

Figure 73. p4 Bit for 64-Bit Packet: 12-Bit Case

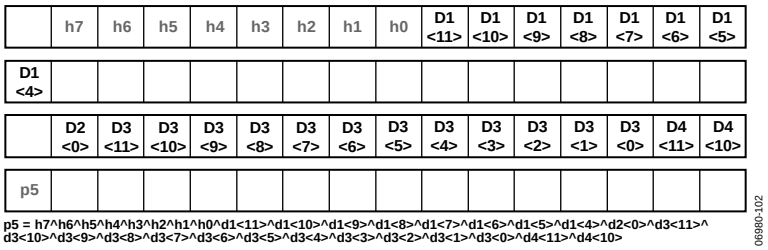

Figure 74. p5 Bit for 64-Bit Packet: 12-Bit Case

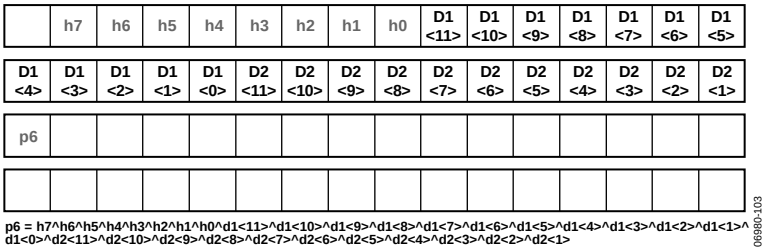

Figure 75. p6 Bit for 64-Bit Packet: 12-Bit Case

TEMPOUT Pin

The TEMPOUT pin can be used as a course temperature sensor to monitor the internal die temperature of the device. This pin typical has a 734 mV output with a clock rate of 250 MSPS and a negative temperature going coefficient of −1.12 mV/C. The voltage response of this pin is characterized in Figure 76.

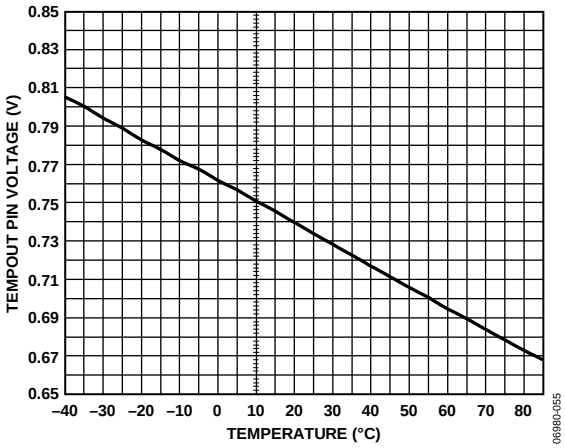

Figure 76. TEMPOUT Pin Voltage vs. Temperature

RBIAS Pin

To set the internal core bias current of the ADC, place a resistor (nominally equal to 10.0 kΩ) between ground and the RBIAS pin. The resistor current is derived on chip and sets the AVDD current of the ADC to a nominal 725 mA at 250 MSPS. Therefore, it is imperative that a 1% or less tolerance on this resistor be used to achieve consistent performance.

VCMx Pins

The common-mode output pins can be enabled through the SPI to provide an external reference bias voltage of 1.4 V for driving the VIN + x/VIN − x analog inputs. These pins may be required when connecting external devices, such as an amplifier or transformer, to interface to the analog inputs.

RESET Pin

The RESET pin sets all SPI registers to their default values and the datapath. Using this pin requires the user to resync the digital outputs. This pin is only 1.8 V tolerant.

PDWN Pin

When asserted high, the PDWN pin turns off all the ADC channels, including the output drivers. This function can be changed to a standby function. See Register 8 in Table 15. Using this feature allows the user to put all channels into standby mode. The output drivers transmit pseudorandom data until the outputs are disabled using Register 14.

By asserting the PDWN pin high, the AD9239 is placed into power-down mode, shutting down the reference, reference buffer, PLL, and biasing networks. In this state, the ADC typically dissipates 3 mW. If any of the SPI features are changed before the power-down feature is enabled, the chip continues to function after PDWN is pulled low without requiring a reset. The AD9239 returns to normal operating mode when the PDWN pin is pulled low. This pin is only 1.8 V tolerant.

SDO Pin

The SDO pin is for use in applications that require a 4-wire SPI mode operation. For normal operation, it should be tied low to AGND through a 10 kΩ resistor. Alternatively, the device pin can be left open, and the 345 Ω internal pull-down resistor pulls this pin low. This pin adheres to only 1.8 V logic.

SDI/SDIO Pin

The SDI/SDIO pin is for use in applications that require either a 4- or 3-wire SPI mode operation. For normal operation, it should be tied low to AGND through a 10 kΩ resistor. Alternatively, the device pin can be left open, and the 30 kΩ internal pull-down resistor pulls this pin low. This pin is only 1.8 V tolerant.

SCLK Pin

For normal operation, the SCLK pin should be tied to AGND through a 10 kΩ resistor. Alternatively, the device pin can be left open, and the 30 kΩ internal pull-down resistor pulls this pin low. This pin is only 1.8 V tolerant.

CSB Pin

For normal operation, the CSB pin should be tied high to AVDD through a 10 kΩ resistor. Alternatively, the device pin can be left open, and the 26 kΩ internal pull-up resistor pulls this pin high. By tying the CSB pin to AVDD, all SCLK and SDI/SDIO information is ignored. In comparison, by tying the CSB pin low, all information on the SDO and SDI/SDIO pins are written to the device. This feature allows the user to reduce the number of traces to the device if necessary. This pin is only 1.8 V tolerant.

PGMx Pins

All PGMx pins are automatically initialized as a sync pin by default. These pins are used to lock the FPGA timing and data capture during initial startup. These pins are respective to each channel (PGM3 = Channel A). The sync pin should be pulled low until this pin receives a high signal input from the receiver, during which time the ADC outputs a training word. The training word defaults to the values implemented by the user in Register 19 through Register 20. When the receiver finds the frame boundary, the sync identification is deasserted high and the ADC outputs the valid data on the next packet boundary.

Once steady state operation for the device has occurred, these pins can be assigned as a standby option using Register 53 in Table 15. All other pins change to a global sync pin.

This pin is only 1.8 V tolerant.

SERIAL PORT INTERFACE (SPI)

The AD9239 serial port interface allows the user to configure the converter for specific functions or operations through a structured register space provided in the ADC. This may provide the user with additional flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, as documented in the Memory Map section. Detailed operational information can be found in the Analog Devices, Inc., AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Four pins define the SPI: SCLK, SDI/SDIO, SDO, and CSB (see Table 13). The SCLK pin is used to synchronize the read and write data presented to the ADC. The SDI/SDIO pin is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB pin is an active low control that enables or disables the read and write cycles.

Table 13. Serial Port Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock input. SCLK is used to synchronize serial interface reads and writes.
SDI/SDIO	Serial Data Input/Output. A dual-purpose pin that typically serves as an input or output, depending on the SPI wire mode and instruction sent and the relative position in the timing frame.
SDO	Serial Data Output is used only in 4-wire SPI mode. When set, the SDO pin becomes active. When cleared, the SDO pin remains in tristate, and all read data is routed to the SDI/SDIO pin.
CSB	Chip Select Bar (Active Low). This control gates the read and write cycles.

The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing sequence. During an instruction phase, a 16-bit instruction is transmitted, followed by one or more data bytes, which is determined by Bit Field W0 and Bit Field W1. An example of the serial timing and its definitions can be found in Figure 78 and Table 14.

During normal operation, CSB is used to signal to the device that SPI commands are to be received and processed. When CSB is brought low, the device processes SCLK and SDI/SDIO to execute instructions. Normally, CSB remains low until the communication cycle is complete. However, if connected to a slow device, CSB can be brought high between bytes, allowing older microcontrollers enough time to transfer data into shift registers. CSB can be stalled when transferring one, two, or three bytes of data. When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until CSB is taken high to end the communication cycle. This allows complete memory transfers without requiring additional instructions. Regardless of the mode, if CSB is taken high in the middle of a byte transfer, the SPI state machine is reset and the device waits for a new instruction.

In addition to the operation modes, the SPI port configuration influences how the AD9239 operates. For applications that do not require a control port, the CSB line can be tied and held high. This places the SDI/SDIO pin into its secondary mode, as defined in the SDI/SDIO Pin section. CSB can also be tied low to enable 2-wire mode. When CSB is tied low, SCLK and SDI/SDIO are the only pins required for communication. Although the device is synchronized during power-up, the user should ensure that the serial port remains synchronized with the CSB line when using this mode. When operating in 2-wire mode, it is recommended to use a 1-, 2-, or 3-byte transfer exclusively. Without an active CSB line, streaming mode can be entered but not exited.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip and read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDI/SDIO pin to change from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB- or LSB-first mode. MSB-first mode is the default at power-up and can be changed by adjusting the configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 13 constitute the physical interface between the user's programming device and the serial port of the AD9239. The SDO, SCLK and CSB pins function as inputs when using the SPI. The SDI/SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

If multiple SDI/SDIO pins share a common connection, care should be taken to ensure that proper V_{OH} levels are met. Assuming the same load for each AD9239, Figure 77 shows the number of SDI/SDIO pins that can be connected together and the resulting V_{OH} level. This interface is flexible enough to be controlled by either serial PROMS or PIC mirocontrollers, providing the user with an alternative method, other than a full SPI controller, to program the ADC (see the AN-812 Application Note).

For users who wish to operate the ADC without using the SPI, remove any connections from the CSB, SCLK, SDO, and SDI/SDIO pins. By disconnecting these pins from the control bus, the ADC can function in its most basic operation. Each of these pins has an internal termination that floats to its respective level.

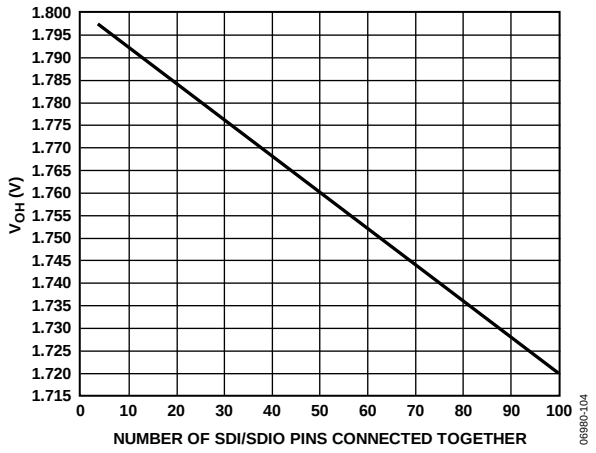

Figure 77. SDI/SDIO Pin Loading

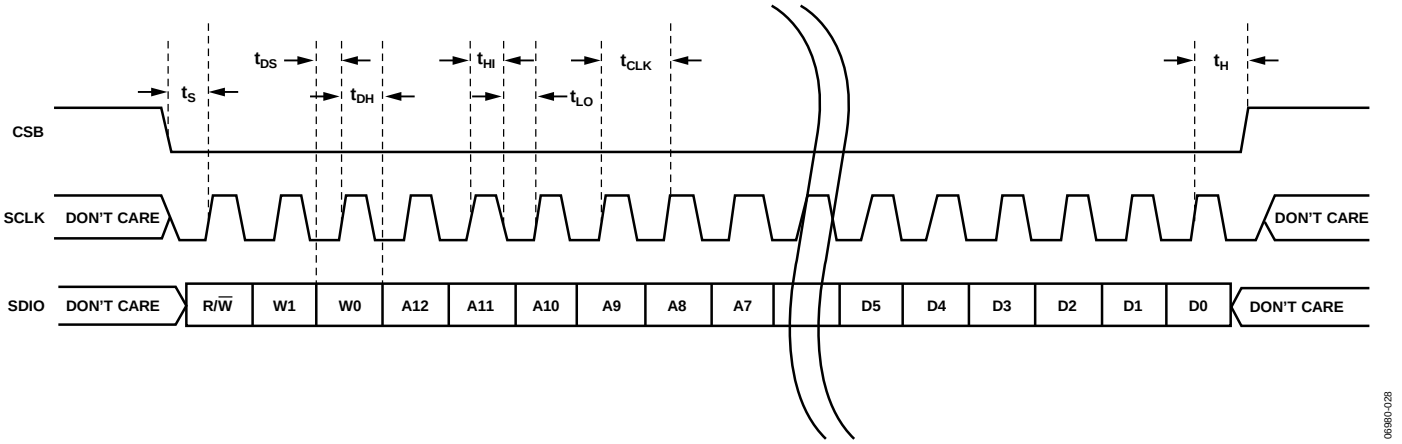

Figure 78. Serial Timing Details

Table 14. Serial Timing Definitions

Parameter	Timing (Minimum, ns)	Description
t_{DS}	5	Setup time between the data and the rising edge of SCLK
t_{DH}	2	Hold time between the data and the rising edge of SCLK
t_{CLK}	40	Period of the clock
t_S	5	Setup time between CSB and SCLK
t_H	2	Hold time between CSB and SCLK
t_{HI}	16	Minimum period that SCLK should be in a logic high state
t_{LO}	16	Minimum period that SCLK should be in a logic low state
$t_{EN\_SDI/SDIO}$	10	Minimum time for the SDI/SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 78)
$t_{DIS\_SDI/SDIO}$	10	Minimum time for the SDI/SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 78)

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map register table (Table 15) has eight bit locations. The memory map is divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02), the device index and transfer registers (Address 0x05 and Address 0xFF), and the ADC functions registers (Address 0x08 to Address 0x53).

The leftmost column of the memory map indicates the register address number, and the default value is shown in the second rightmost column. The Bit 7 column is the start of the default hexadecimal value given. For example, Address 0x09, the clock register, has a default value of 0x01, meaning that Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition. By writing a 0 to Bit 0 of this address, followed by a 0x01 in Register 0xFF (transfer bit), the duty cycle stabilizer turns off. It is important to follow each writing sequence with a transfer bit to update the SPI registers. For more information on this and other functions, consult the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

RESERVED LOCATIONS

Undefined memory locations should not be written to except when writing the default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

DEFAULT VALUES

When the AD9239 comes out of a reset, critical registers are preloaded with default values. These values are indicated in Table 15, where an X refers to an undefined feature.

LOGIC LEVELS

An explanation of various registers follows: "bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit." Similarly, "clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Table 15. Memory Map Register

Addr. (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
00	chip_port_ config (local, master)	SDO active (not required, ignored if not used)	LSB first	Soft reset	16 bit address (default mode for ADCs)					0x18	
01	chip_id (global)	8-bit Chip ID Bits[2:0] 0x0B – AD9239 – 12-bit quad								Read only	
02	chip_grade (global)		Speed grade 010 = 170 100 = 210 101 = 250							Read only	
Device Index and Transfer Registers											
05	device_ index_A (global)					ADC A	ADC B	ADC C	ADC D	0x0F	Bits are set to determine which device on chip receives the next write command. The default is all devices on chip.
FF	device_ update (local, master)								SW transfer 1 = on 0 = off (default)	0x00	Synchro-nously transfers data from the master shift register to the slave.
ADC Functions Registers											
08	modes (local)			External PDWN pin function 00 = full PDWN (default) 01 = standby				00 = chip run (default) 01 = full power-down 10 = standby 11 = reset		0x00	Determines various ge-neric modes of chip operation.
09	Clock (global)								Duty cycle stabilize 1 = on (default) 0 = off	0x01	Turns the internal duty cycle stabilizer on and off.
0D	test_io (local)			Reset PN long gen 1 = on 0 = off (default)	Reset PN short gen 1 = on 0 = off (default)	Flex output test mode 0000 = off (normal operation) 0001 = midscale short 0010 = +FS short 0011 = –FS short 0100 = checkerboard output 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = one/zero word toggle				0x00	When set, the test data is placed on the output pins in place of normal data.
0E	test_bist (local)						BIST init 1 = on 0 = off (default)		BIST enable 1 = on 0 = off (default)	0x00	When Bit 0 is set, the built-in self-test function is initiated.

Addr. (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)	Default Notes/ Comments
0F	adc_input (local)						Analog disconnect enable 1 = on 0 = off (default)	VCM enable 1 = on 0 = off (default)		0x00	
10	offset (local)	6-bit Device Offset Adjustment[5:0] 011111 = +31 LSB 011110 = +30 LSB 011101 = +29 LSB … 000010 = +2 LSB 000001 = +1 LSB 000000 = 0 LSB 111111 = −1 LSB 111110 = −2 LSB 111101 = −3 LSB … 100001 = −31 LSB 100000 = −32 LSB								0x00	Device offset trim.
14	output_mode (local/global)				Output enable bar (local) 1 = off 0 = on (default)		Output invert (global) enable 1 = on 0 = off (default)	Data format select (global) 00 = offset binary (default) 01 = twos complement 10 = gray code		0x00	Configures the outputs and the format of the data.
15	output_adjust (global)							Output Drive Current[1:0] 00 = 400 mV (default) 01 = 500 mV 10 = 440 mV 11 = 320 mV		0x00	VCM output adjustments.
18	vref (global)	Ref_Vfs[4:0] Reference full-scale adjust 10000 = 0.98 V p-p 10001 = 1.00 V p-p 10010 = 1.02 V p-p 10011 = 1.04 V p-p … 11111 = 1.23 V p-p 00000 = 1.25 V p-p (default) 00001 = 1.27 V p-p … 01110 = 1.48 V p-p 01111 = 1.5 V p-p								0x00	Select adjustments for V_{REF}.
21	serial_control (global)					PLL high encode rate mode (global) 0 = low rate 1 = high rate (default)				0x08	Serial stream control.
24	misr_lsb (local)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	Least significant byte of MISR. Read only.
25	misr_msb (local)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	Most significant byte of MISR. Read only.

Addr. (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)	Default Notes/ Comments
32	adi_link_ options (global)		Hamming enable 1 = on (default) 0 = off	Scramble data only 0 = scramble header and data (default) 1 = scramble data only	Data flow order 0 = ECC last (default) 1 = Scrambler last (Override 0x032[5])	Over-range in header 1 = on (default) 0 = off	Scramble options 00 = inverted 01 = SONET (default) 10 = Ethernet		Scramble enable 1 = on (default) 0 = off	0x4B	Default is 56-bit SONET scrambler with over range in the header bits.
34	Channel ID (local)	Channel ID (Only Bits[3:0] used if overrange is included in header)								0x00	
53	Dynamic pgm pins (global)	pgm_3 00 = sync 01 = standby A 10 = standby A and D 11 = standby A and B		pgm_2 00 = sync 01 = standby B 10 = standby B and C 11 = standby B and A		pgm_1 00 = sync 01 = standby C 10 = standby C and B 11 = standby C and D		pgm_0 00 = sync 01 = standby D 10 = standby D and A 11 = standby D and C		0x00	Standby = ADC core off, PN23 enabled, serial channel enabled.

Power and Ground Recommendations

When connecting power to the AD9239, it is recommended that two separate 1.8 V supplies be used: one for analog (AVDD) and one for digital (DRVDD). If only one supply is available, it should be routed to the AVDD first and then tapped off and isolated with a ferrite bead or a filter choke preceded by decoupling capacitors for the DRVDD. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the printed circuit board (PCB) level and close to the parts, with minimal trace lengths.

A single PCB ground plane should be sufficient when using the AD9239. With proper decoupling and smart partitioning of the analog, digital, and clock sections of the PCB, optimum performance can easily be achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is required that the exposed paddle on the underside of the ADC is connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9239. An exposed continuous copper plane on the PCB should mate to the AD9239 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions guarantees only one tie point. See Figure 79 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, at www.analog.com.

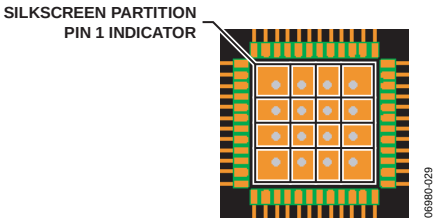

Figure 79. Typical PCB Layout

OUTLINE DIMENSIONS

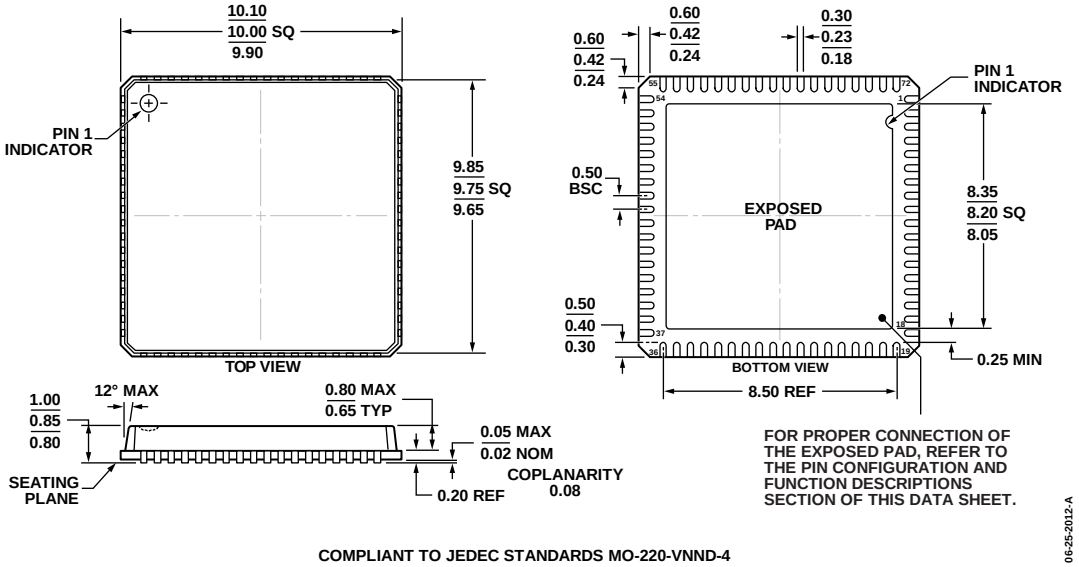

Figure 80. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9239BCPZ-170	–40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-3
AD9239BCPZ-210	–40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-3
AD9239BCPZ-250	–40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-3
AD9239-250KITZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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D06980-0-5/14(D)