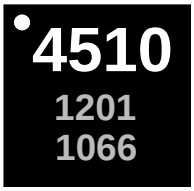
TGC4510-SM

K Band Upconverter

Applications

- VSAT Ground Terminal
- Point-to-Point Radio
- Millimeter wave Communications

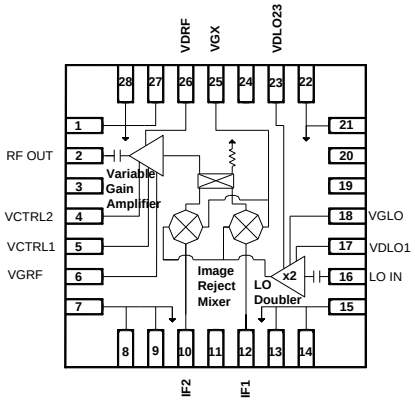


28-pin 5x5mm QFN package

Product Features

- RF Frequency Range: 17.7 – 26.5 GHz
- IF Frequency: DC – 4.0 GHz
- LO Frequency: 6.85 – 15.25 GHz
- LO Input Power: 2 to 10 dBm
- Conversion Gain: 13 dB
- OTOI: 32 dBm at max gain
- Attenuation Range: 30 dB typical
- Bias 5.0 V, 345 mA, 3.3 V, 120 mA
- Package Dimensions: 5.0 x 5.0 x 1.3 mm

Functional Block Diagram



General Description

The TriQuint TGC4510-SM is a K-Band image reject upconverter mixer with integrated x2 LO buffer amplifier and output variable gain amplifier. The TGC4510-SM outputs an RF frequency from 17.7 to 26.5 GHz using IF inputs from DC to 4.0 GHz and a corresponding LO frequency. It is designed using TriQuint's pHEMT production process.

The TGC4510-SM typically provides 32 dBm of output TOI at –10 dBm input power per tone and has a conversion gain of 13 dB. Optional nulling of the LO can improve LO Isolation by 30 dB.

The TGC4510-SM is available in a low-cost, surface mount 28 lead 5x5mm QFN package and is ideally suited for Point-to-Point Radio, and K-Band VSAT Ground Terminal.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Pin Configuration

Pin #	Function Label
1,7,8,9,13,14,15,21,22, 27,28	GND
2	RF OUT
3,11,19,20,24	NC
4	VCTRL2
5	VCTRL1
6	VGRF
10	IF2
12	IF1
16	LO IN
17	VDLO1
18	VGLO
23	VDLO23
25	VGX
26	VDRF

Ordering Information

Part No.	ECCN	Description
TGC4510-SM	EAR99	K Band Upconverter

Standard T/R size = 500 pieces on a 7" reel

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Specifications

Absolute Maximum Ratings

Parameter	Rating
VDRF, VDLO1, VDLO23	6 V
IDRF	390 mA
IDLO1	190 mA
IDLO23	300 mA
VGRF, VGLO, VGX	-3 to +1.5 V
VCTRL1, VCTRL2	-3 to +0 V
DC Voltage at IF1, IF2 for LO nulling	-2 to +2V
RF Input Power,LO IN, 50Ω, T = 25°C	15 dBm
RF Input Power,IF IN, 50Ω, T = 25°C	18 dBm
Channel Temperature, Tch	200 °C
Storage Temperature	-65 to 125 °C
Power Dissipation, Pdiss	2 W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Temp. Range	-40		+85	°C
VDRF		5.0		V
VDLO1, VDLO23		3.3		V
IDRF		360		mA
IDLO1+IDLO23		180		mA
VCTRL1, VCTRL2	-2		0	V
LO IN input power	3	6	9	dBm
IF1, IF2 input power		-10		dBm

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

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Specifications

Electrical Specifications

Test conditions unless otherwise noted: VDLO1, VDLO23 = 3.3 V, VGLO = –1.2 V, IDLO1+IDLO23 = 140 to 200 mA, VDRF = 5.0 V, VGRF = –0.75 V, IDRF = 340 to 380 mA, VGX = –1.2 V, T = 25 °C
Characteristic Impedance: 50 Ω

Parameter	Conditions	Min	Typ	Max	Units
RF Frequency Range		17.7		26.5	GHz
LO Frequency Range		6.85		15.25	GHz
IF Frequency Range		0		4	GHz
Conversion Gain Full Frequency Range 17.7 – 23.6 GHz	1/	 9.5	 13 13	 17.5	dB
Attenuation Range	2/		34		dB
SSB Noise Figure			15		dB
OIP3 Full Frequency Range 17.7 – 23.6 GHz		 27.5	 32 32		dBm
IIP3 at Minimum Gain			13		dBm
Image Rejection			15		dB
LO Isolation at RF Port	3/ 5/		-5		dB
LO Isolation at RF Port	4/ 5/		25		dB
LO Return Loss			12		dB
RF Return Loss			11		dB

1/ maximum gain, VCTL1 = -2 V, VCTL2 = 0 V

2/ maximum gain at VCTL1 = -2 V, VCTL2 = 0 V; minimum gain at VCTL1 = 0 V, VCTL2 = -2 V

3/ without external LO nulling voltage

4/ with external LO nulling voltage

5/ LO Isolation = (Input Power at LO Port at LO Frequency) – (Output Power at RF port at 2xLO frequency)

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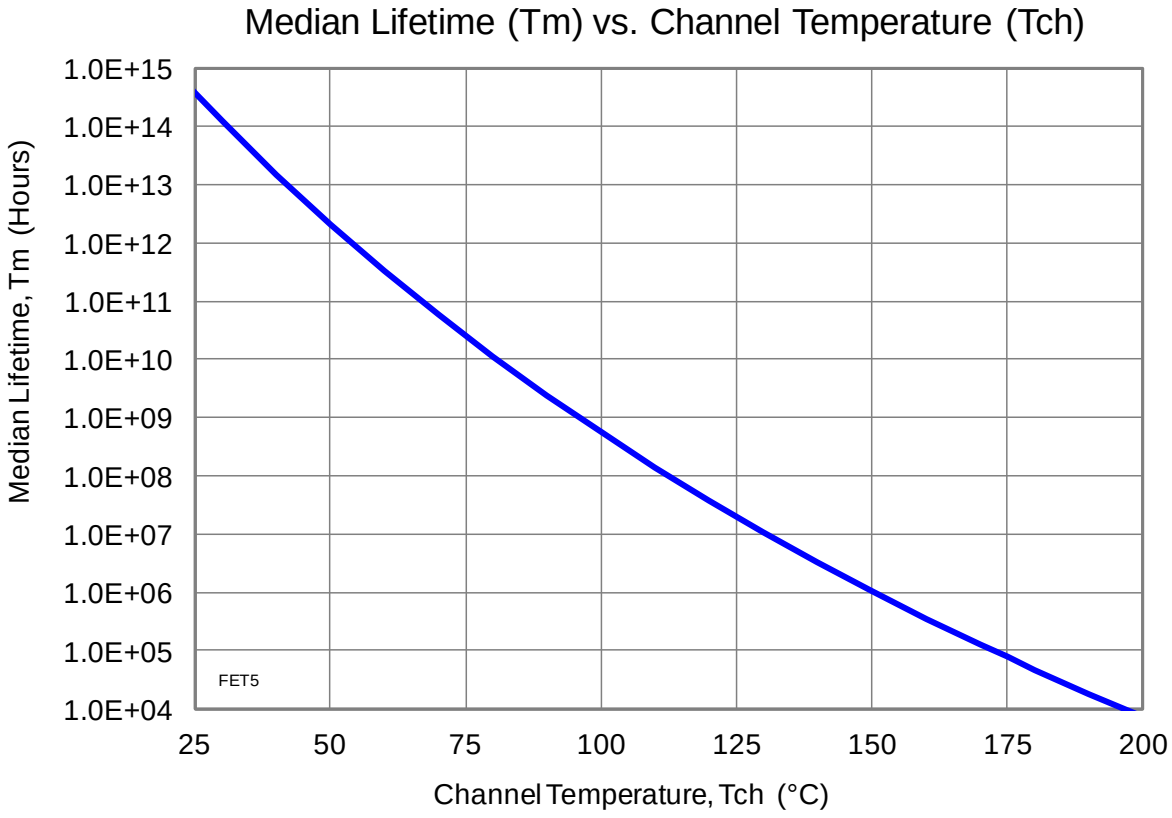
Specifications

Thermal and Reliability Information

Parameter	Conditions	Rating
Thermal Resistance, θ_{JC}, measured to back of package	Tbase = 85 °C	θ_{JC} = 19.6 °C/W
Channel Temperature (Tch), and Median Lifetime (Tm)	Tbase = 85 °C, VDLO = 3.0 V, IDLO=260 mA, VDRF = 5.0 V, IDRF=360 mA Pdiss = 2.6 W	Tch = 136 °C Tm = 5.2 E+06 Hours



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Typical Performance

Unless noted, bias conditions for all measurements:
VDLO1, VDLO23 = 3.3 V, VGLO = -1.2 V, IDLO1+IDLO23 = 140 to 200 mA,
VDRF = 5.0 V, VGRF = -0.75 V, IDRF = 340 to 380 mA; VGX = -1.2 V
Unless noted, all measurements with IF Input Power = -10 dBm, external IF hybrid and no LO nulling at 25 °C

Lower Side Band Frequency Ranges		
IF Freq GHz	LO Freq GHz	RF Freq GHz
0.5	9-14	17.5-27.5
1.0	9-14	17-27
2.0	9-14	16-26
3.0	10-15	17-27
3.3	10-15.5	16.7-27.7
4.0	10-16	16-28

Upper Side Band Frequency Ranges		
IF Freq GHz	LO Freq GHz	RF Freq GHz
0.5	8-14	16.5-28.5
1.0	8-13	17-28
2.0	7-13	16-28
3.0	6.5-12	16-27
3.3	6.5-12	16.3-27.3
4.0	6.5-11	17-26

State	VCTRL1 V	VCTRL2 V
Max Gain	-2	0
Reduced Gain	-1.0	-1.0
Min Gain	0	-2

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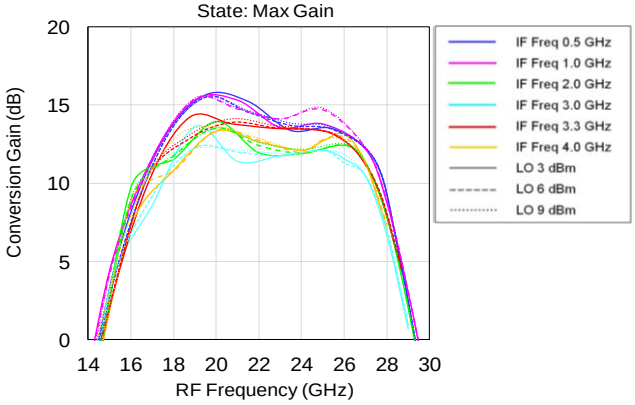
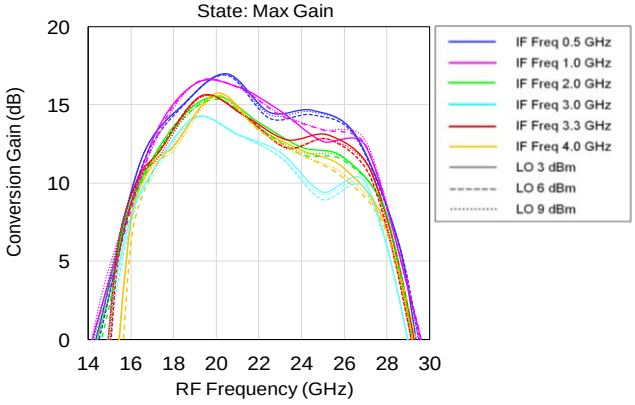
Typical Performance – Conversion Gain and Reduced Gain

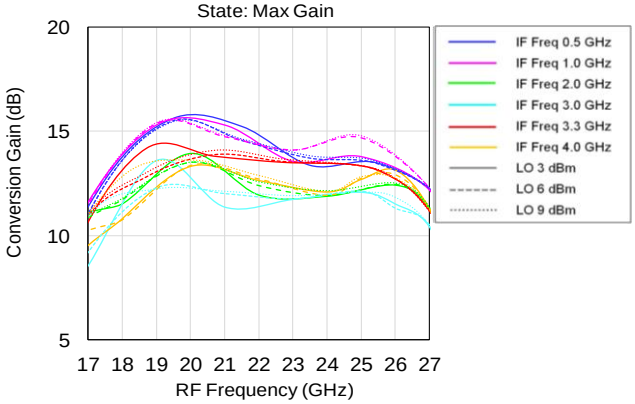
LSB Conversion Gain vs. RF vs. IF and LO Power
State: Max Gain



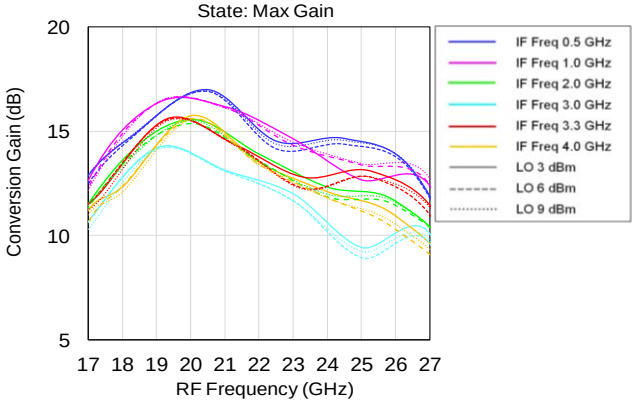
USB Conversion Gain vs. RF vs. IF and LO Power
State: Max Gain



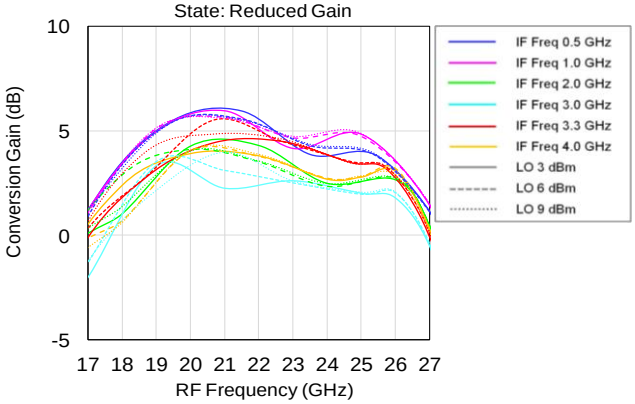
LSB Conversion Gain vs. RF vs. IF and LO Power
State: Max Gain



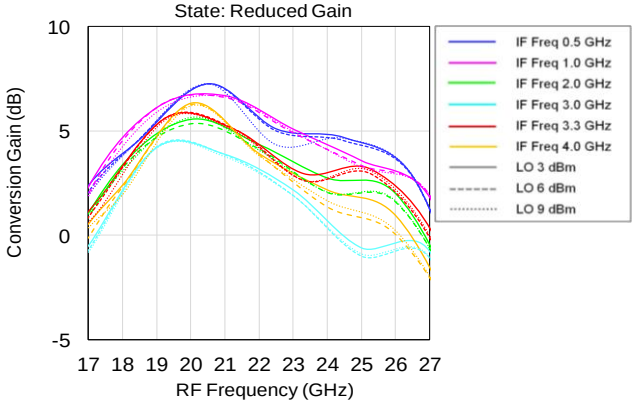
USB Conversion Gain vs. RF vs. IF and LO Power
State: Max Gain



LSB Conversion Gain vs. RF vs. IF and LO Power
State: Reduced Gain



USB Conversion Gain vs. RF vs. IF and LO Power
State: Reduced Gain



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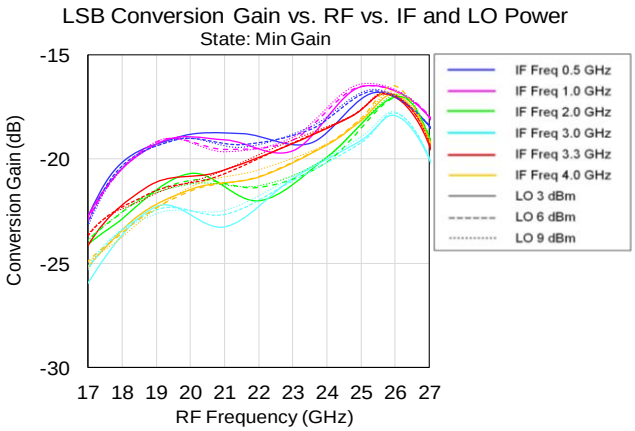
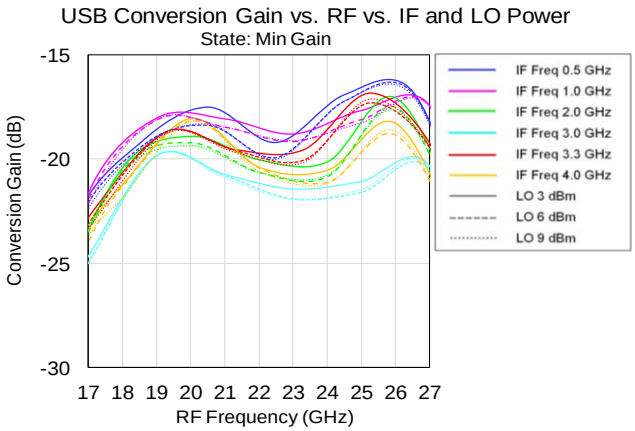
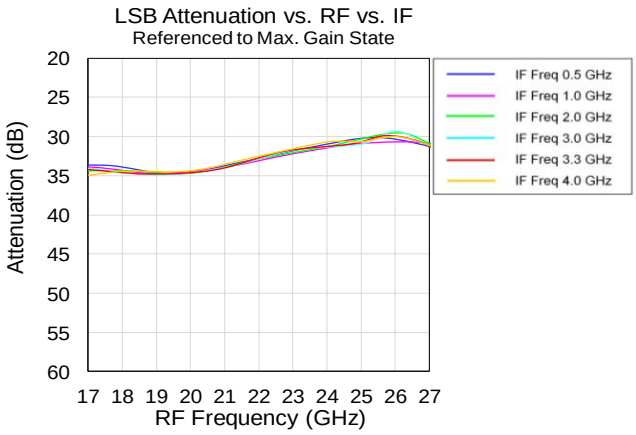
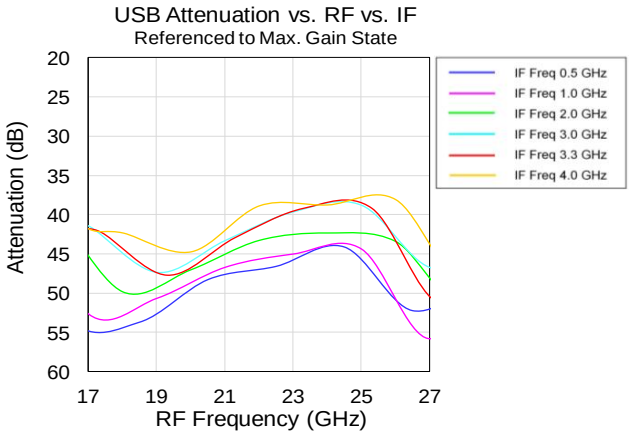
Typical Performance - Conversion Gain and Reduced Gain









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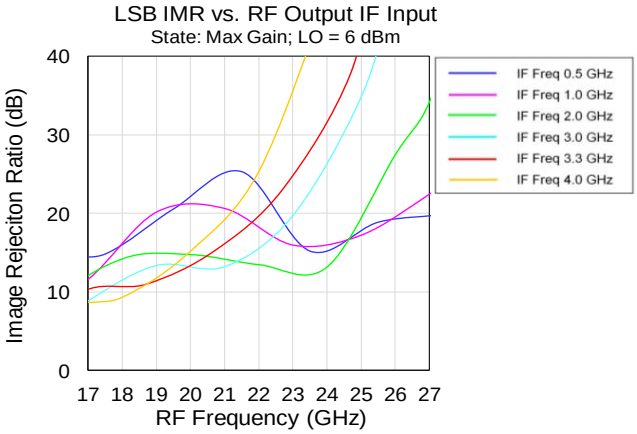
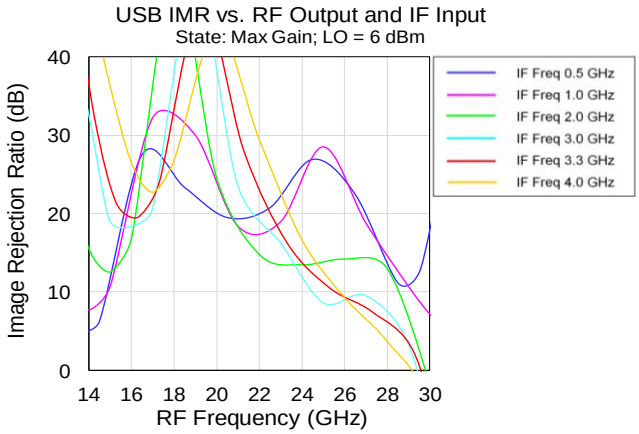
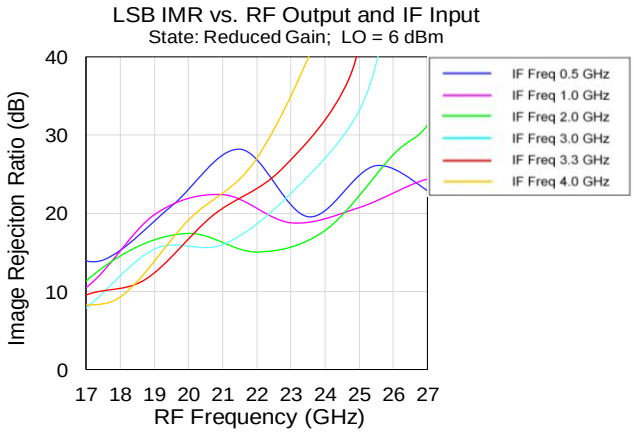
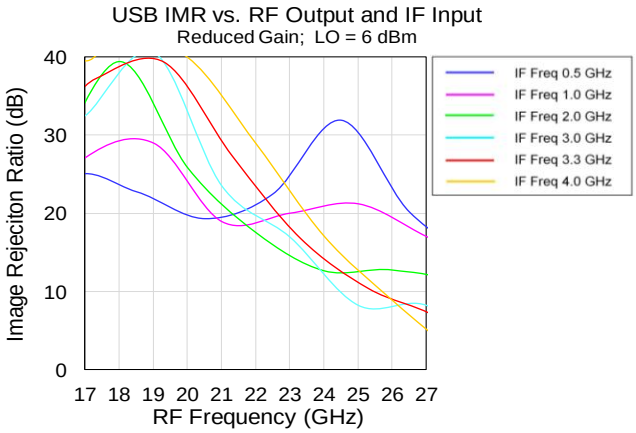
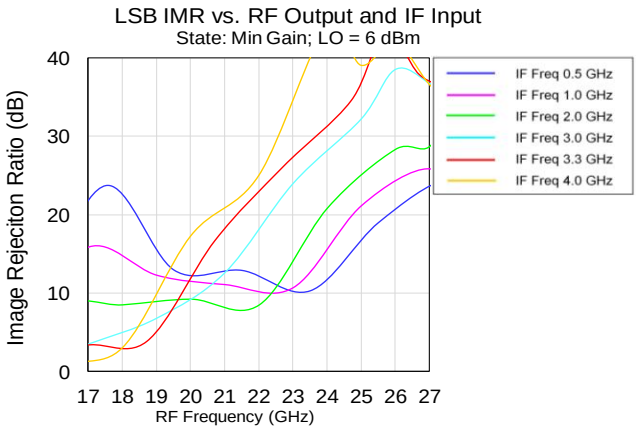
Typical Performance – Image Rejection

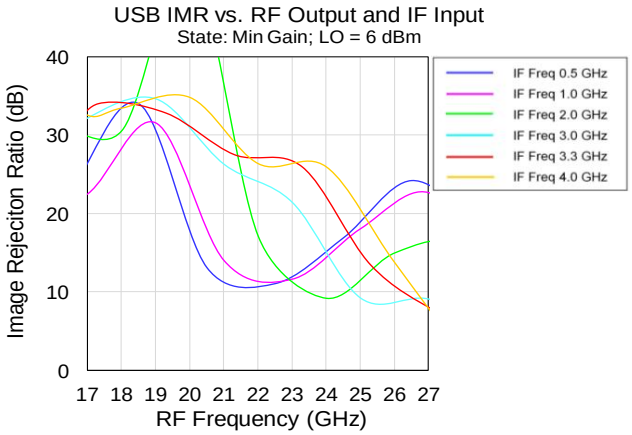












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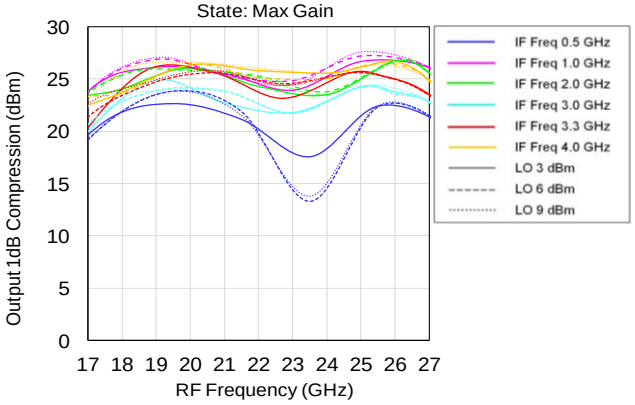
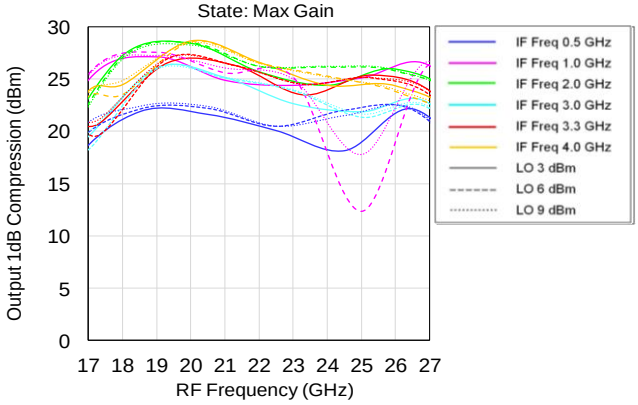
Typical Performance - 1dB Compression, Output IP3

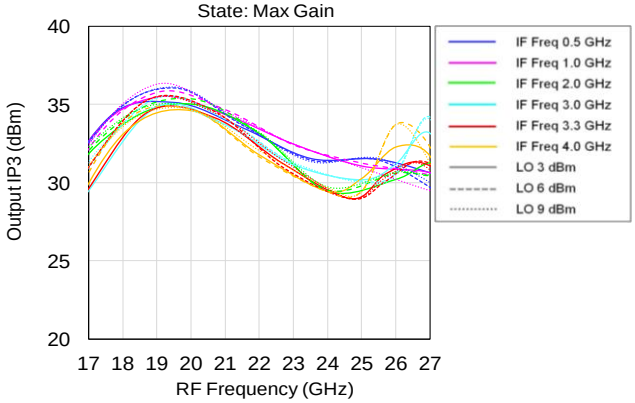
LSB Output 1dB Compression vs. RF vs. IF and LO Power
State: Max Gain



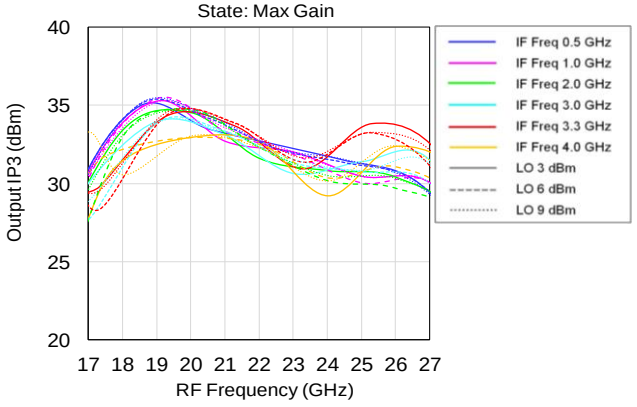
USB Output 1dB Compression vs. RF vs. IF and LO Power
State: Max Gain



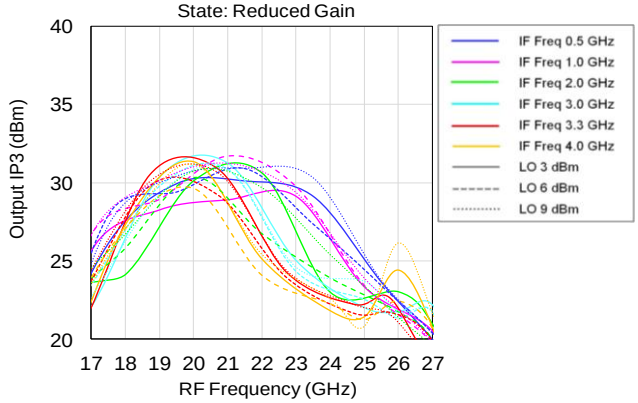
LSB Output IP3 vs. RF vs. IF and LO Power
State: Max Gain



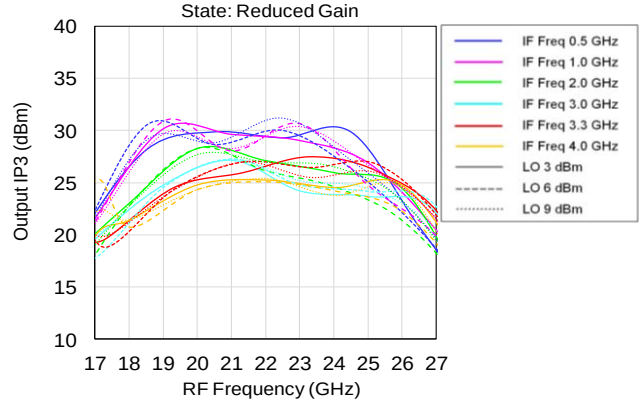
USB Output IP3 vs. RF vs. IF and LO Power
State: Max Gain



LSB Output IP3 vs. RF vs. IF and LO Power
State: Reduced Gain



USB Output IP3 vs. RF vs. IF and LO Power
State: Reduced Gain



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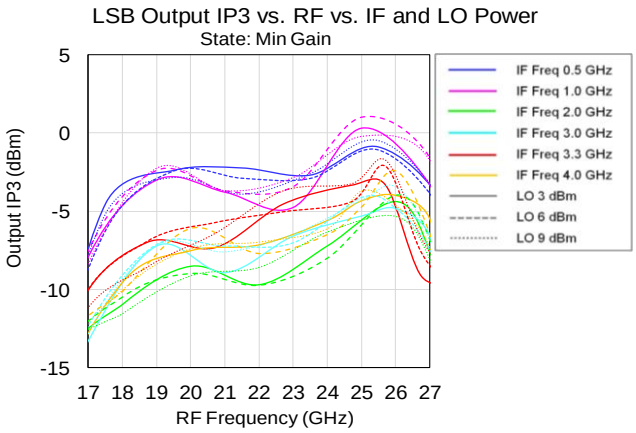
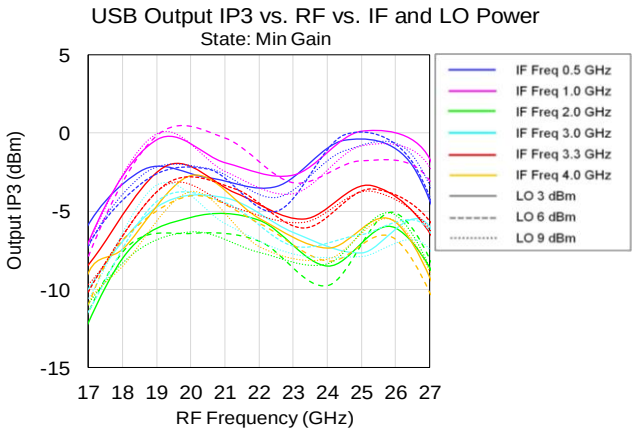
Typical Performance - Output IP3





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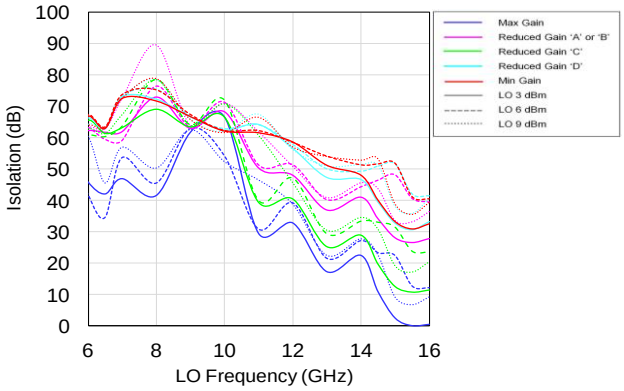
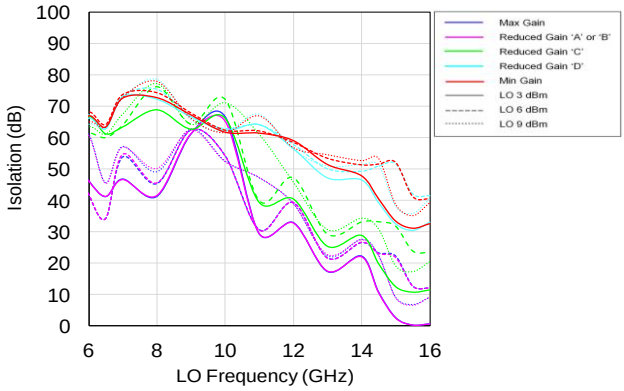
Typical Performance - Isolation

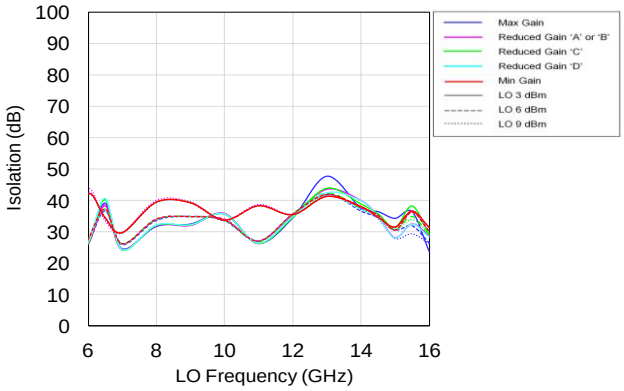
LSB L to R Isolation vs. LO Freq vs. LO Power and State



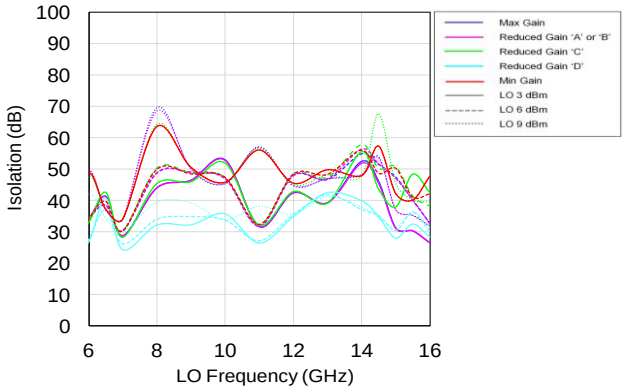
USB L to R Isolation vs. LO Freq vs. LO Power and State



LSB L to I Isolation vs. LO Freq vs. LO Power and State

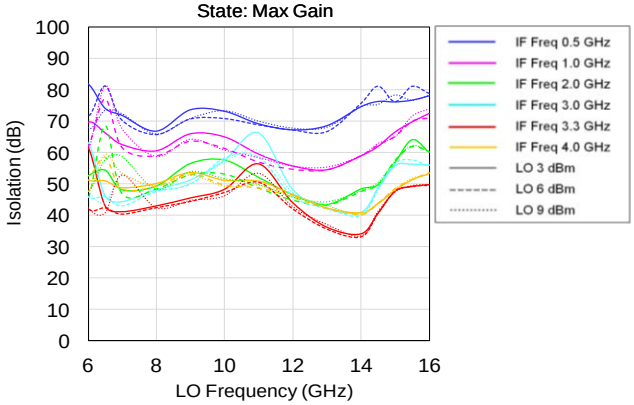


USB L to I Isolation vs. LO Freq vs. LO Power and State



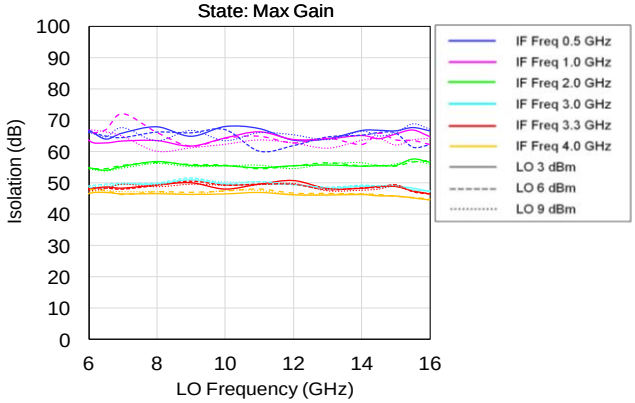
I to R Isolation vs. LO vs. IF and LO Power

State: Max Gain



I to L Isolation vs. LO vs. IF and LO Power

State: Max Gain



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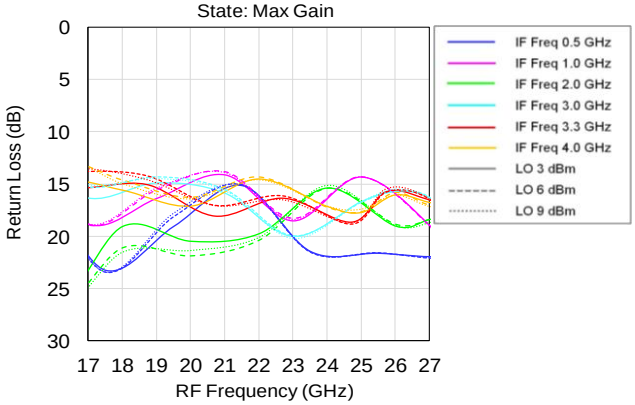
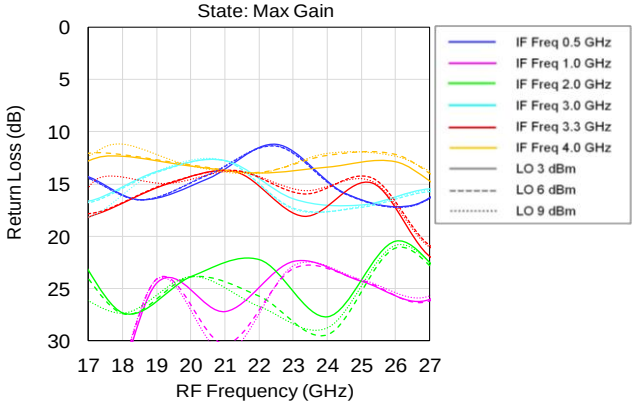
Typical Performance Return Loss

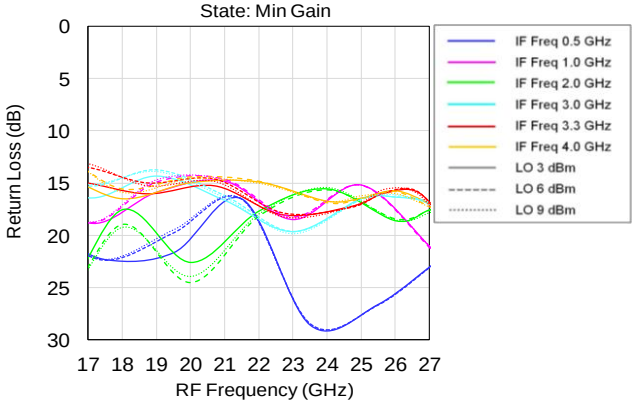
LSB RF Return Loss vs. IF and LO Power
State: Max Gain



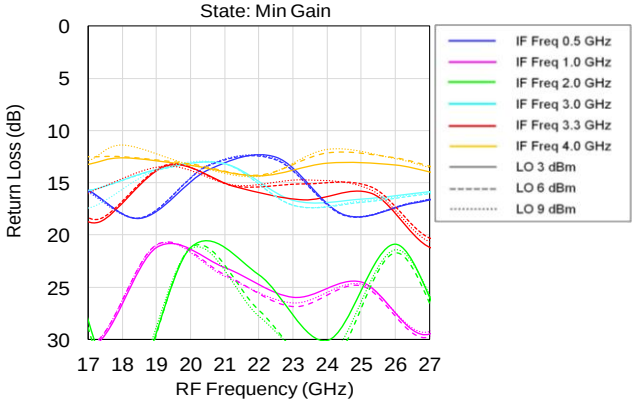
USB RF Return Loss vs. RF vs. IF and LO Power
State: Max Gain



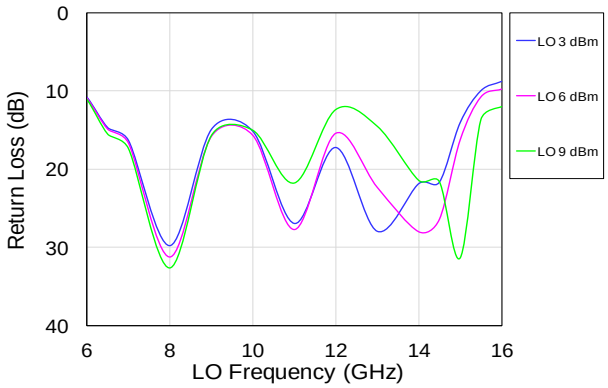
LSB RF Return Loss vs. RF vs. IF and LO Power
State: Min Gain



USB RF Return Loss vs. RF vs. IF and LO Power
State: Min Gain



LO Return Loss vs. Frequency and LO Power



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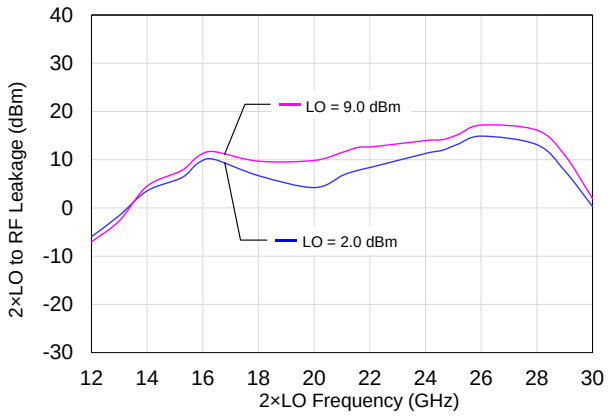
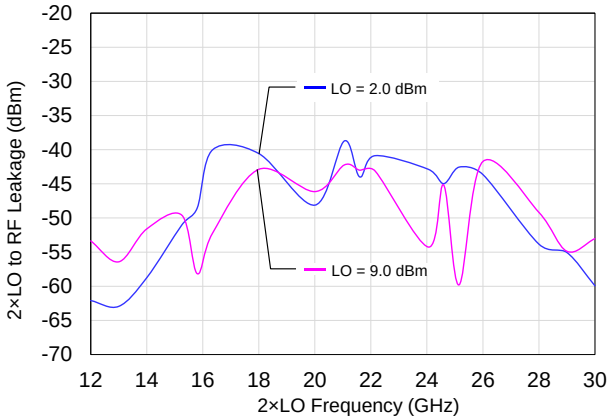
Typical Performance – External LO Nulling

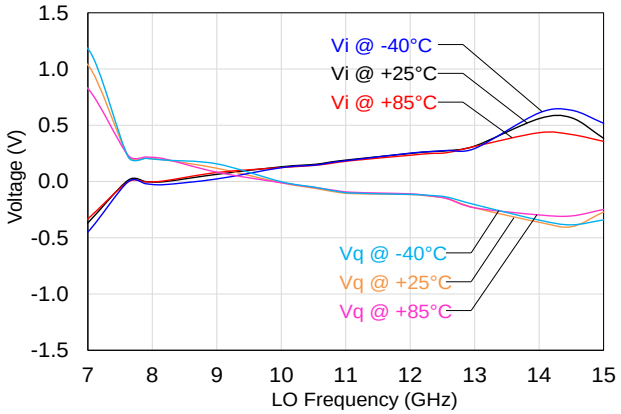
2×LO to RF Leakage **WITHOUT** External LO Nulling Voltages
State: Max Gain



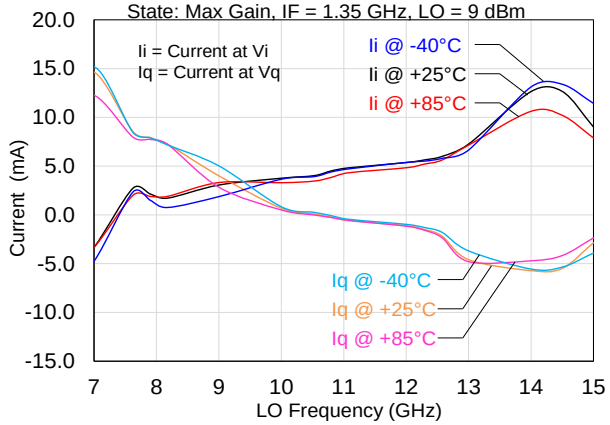
2×LO to RF Leakage **WITH** External LO Nulling Voltages
State: Max Gain



LO Nulling Voltages vs. LO Frequency vs. Temperature
State: Max Gain, IF = 1.35 GHz, LO = 9 dBm



Current for LO Nulling Voltage vs. LO Frequency vs. Temperature
State: Max Gain, IF = 1.35 GHz, LO = 9 dBm



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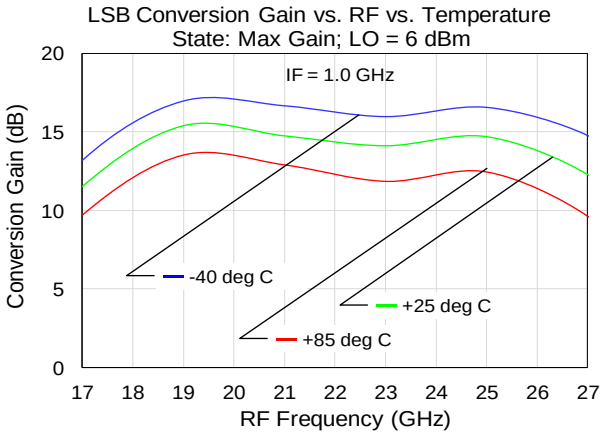
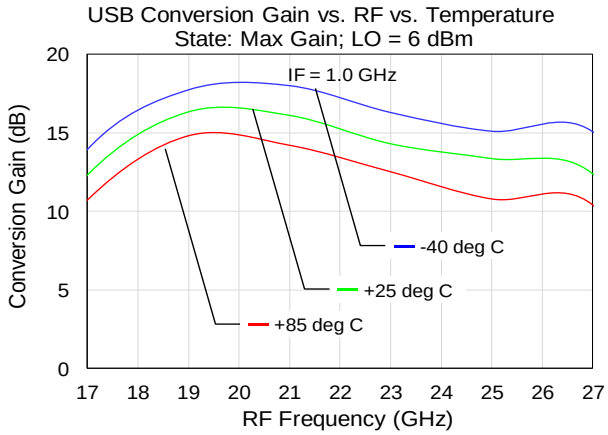
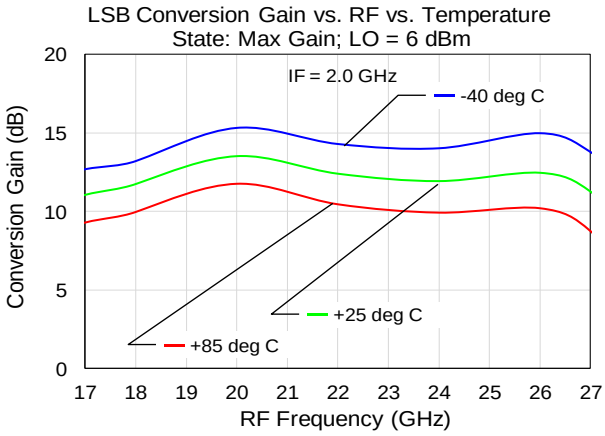
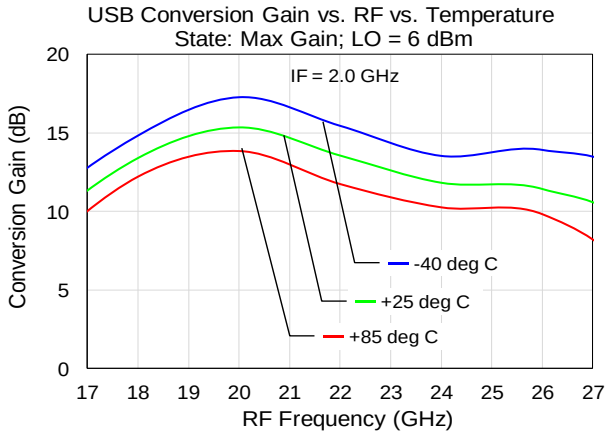
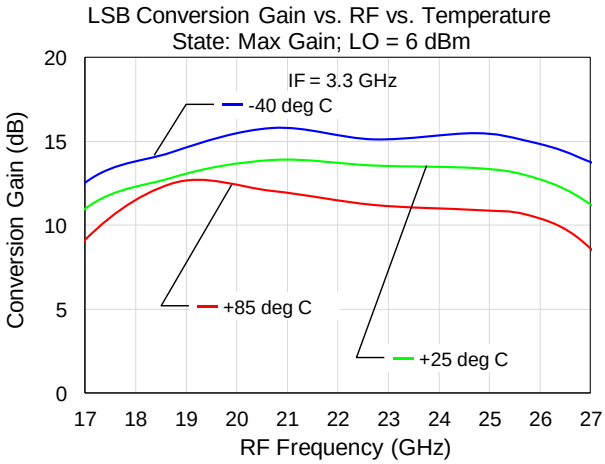
Typical Performance – Conversion Gain vs. Temperature

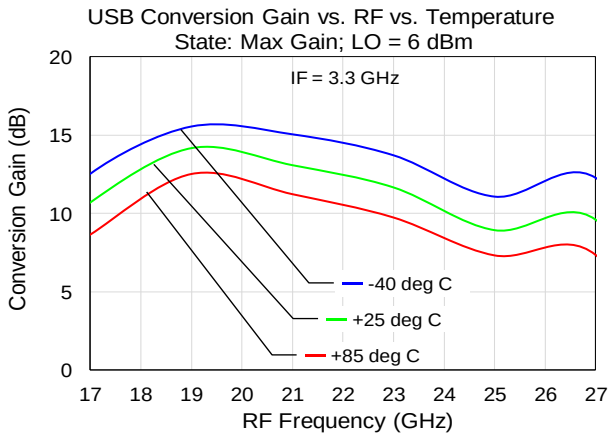












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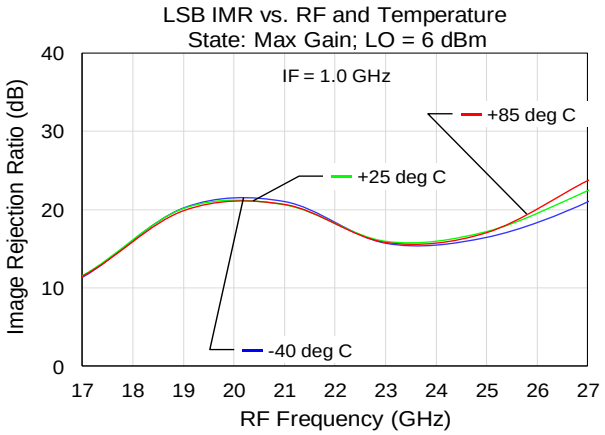
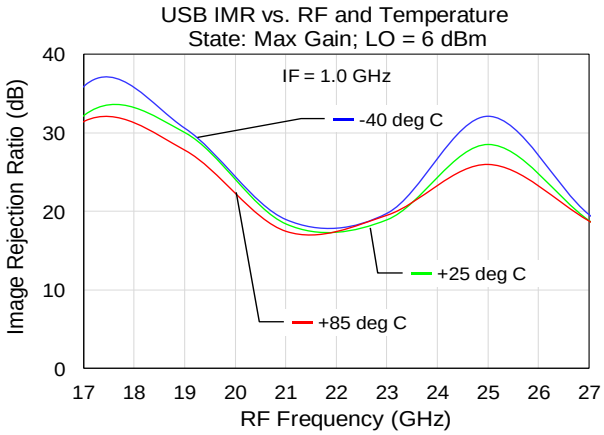
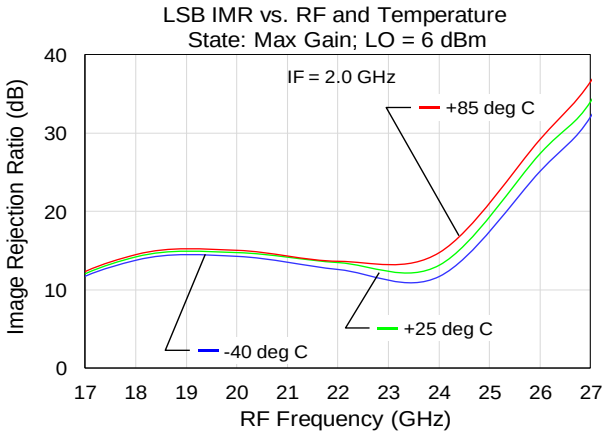
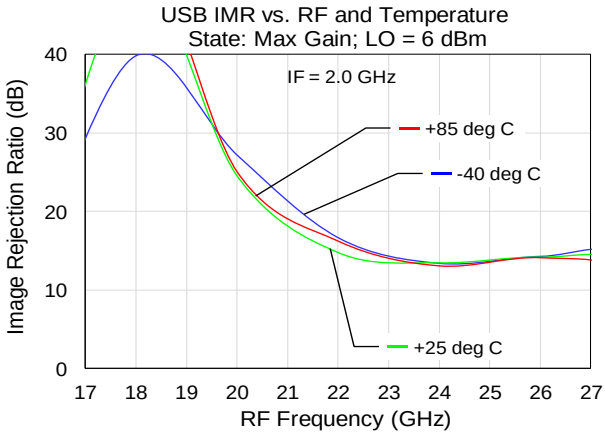
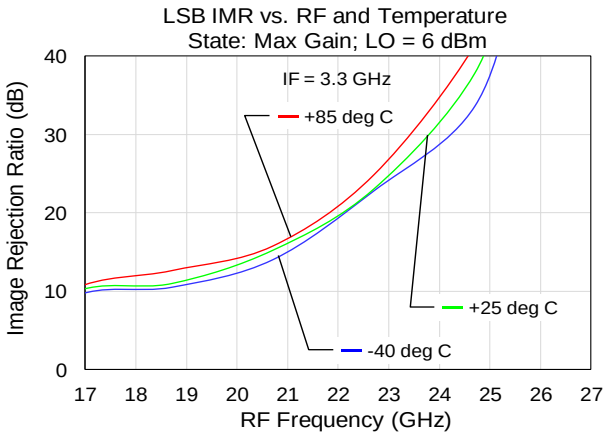
Typical Performance – Image Rejection vs. Temperature

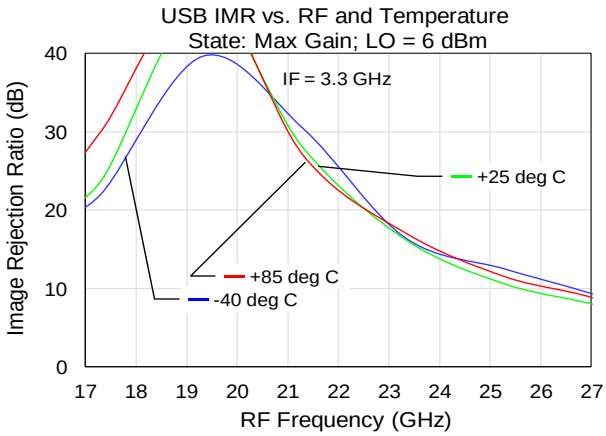












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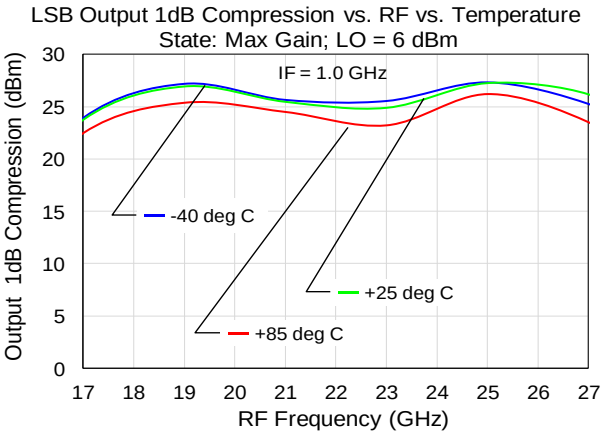
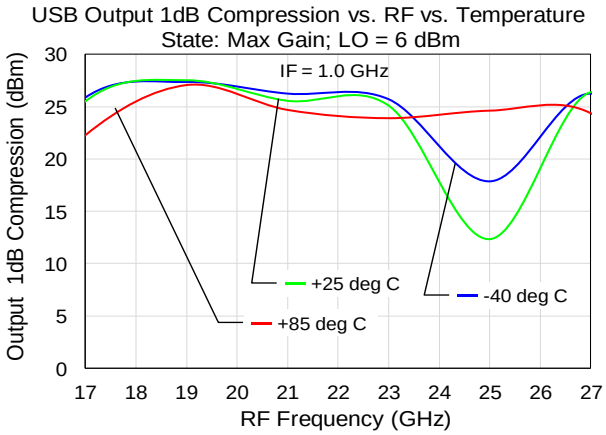
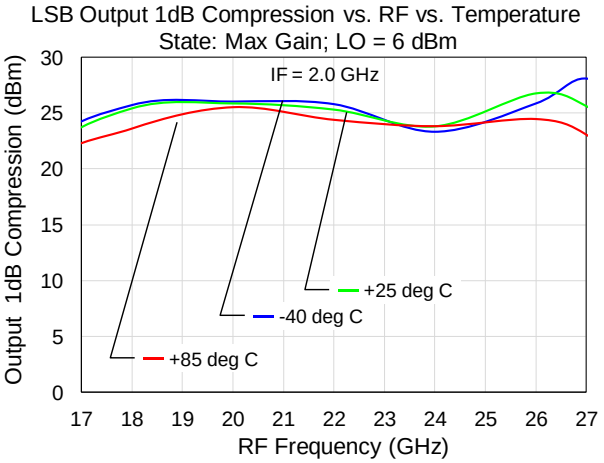
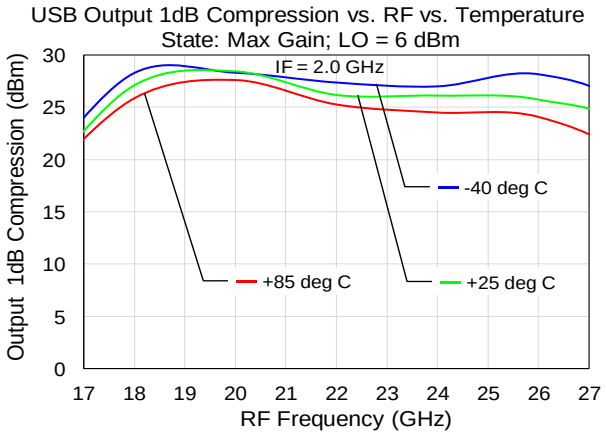
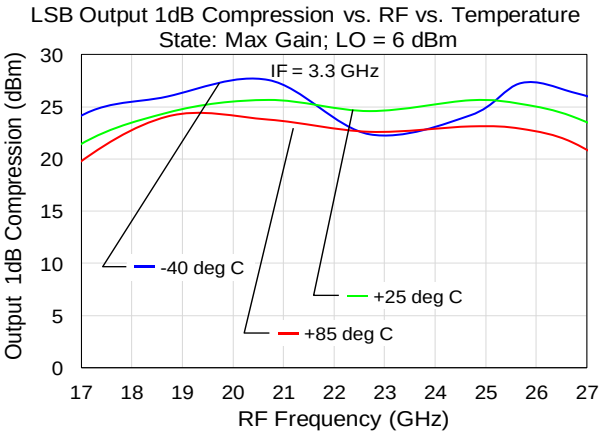
Typical Performance – 1dB Compression vs. Temperature

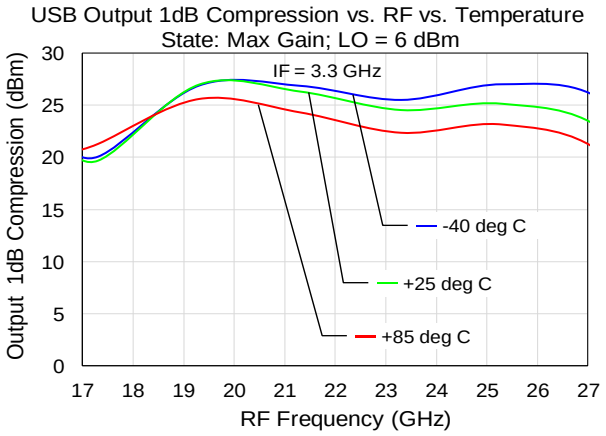












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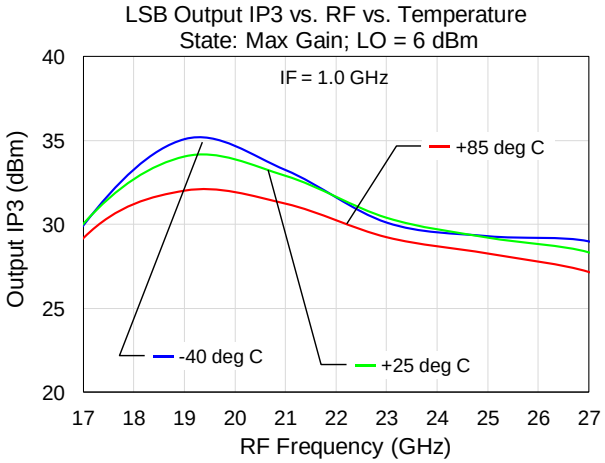
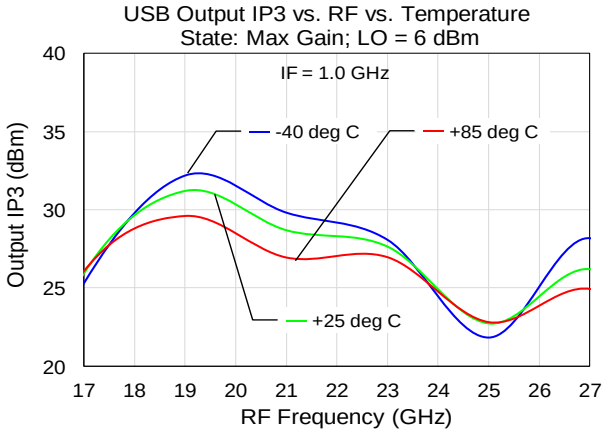
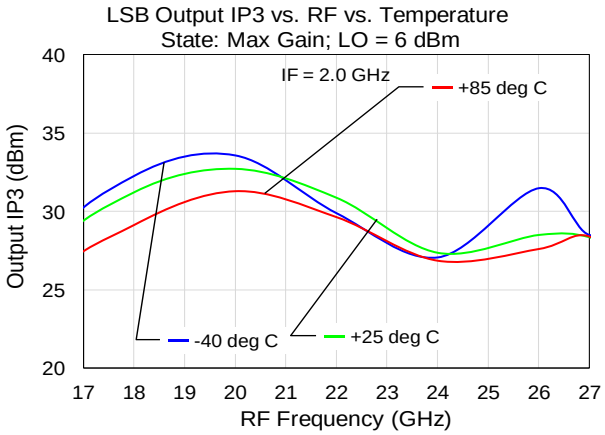
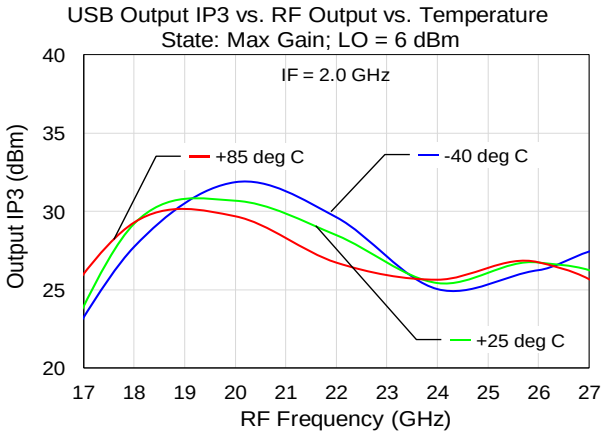
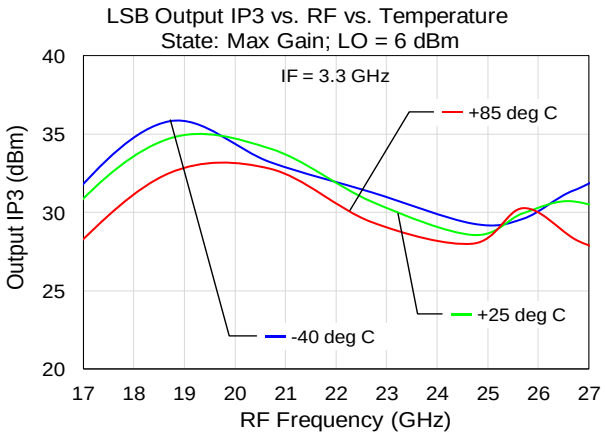
Typical Performance – Output IP3 vs. Temperature

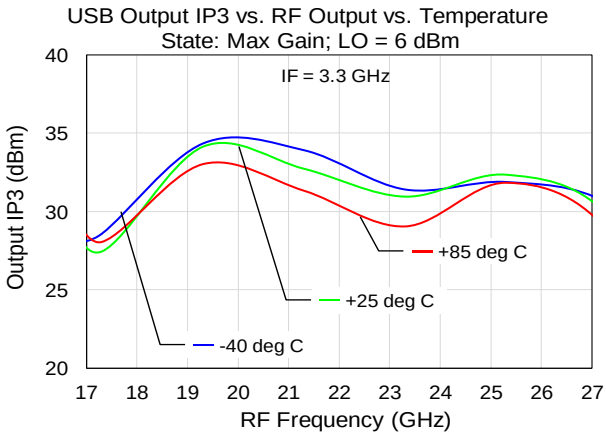












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Typical Performance - Spur Tables, IF 2.0 GHz

Spur Tables

Spur tables are $N \times f_{IF} - M \times f_{LO}$ mixer spurious products for -10 dBm IF input power.

RF is at 1IF x 2LO.

All values in dBc below the RF output power level.

M x N Spurious Outputs for LSB, IF = 2.0 GHz

LO = 9 – 13 GHz, 3 – 9 dBm, 25 °C

		M x f_{LO}					
		0	1	2	3	4	5
	-5	--	86	79	70	60	63
	-4	--	85	76	74	63	61
	-3	--	84	77	70	59	60
	-2	--	82	74	66	64	61
	-1	--	81	0	63	58	61
N	0	--	12	19	4	33	53
	1	89	75	12	63	57	60
	2	83	75	73	61	61	57
	3	82	74	67	60	60	--
	4	79	76	69	63	60	--
	5	84	77	67	59	58	--

M x N Spurious Outputs for USB, IF = 2.0 GHz

LO = 8 –12 GHz, 3 – 9 dBm, 25 °C

		M x f_{LO}					
		0	1	2	3	4	5
	-5	--	89	77	76	65	62
	-4	--	88	76	78	65	62
	-3	--	88	79	73	64	64
	-2	--	84	68	72	61	62
	-1	--	76	14	53	54	65
N	0	--	26	-13	6	32	55
	1	69	59	0	42	61	63
	2	88	77	66	61	63	64
	3	85	79	74	64	59	66
	4	85	79	71	66	65	65
	5	85	79	69	62	63	61

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Typical Performance - Spur Tables, IF 3.3 GHz

Spur Tables

Spur tables are $N \times f_{IF} - M \times f_{LO}$ mixer spurious products for -10 dBm IF input power.

RF is at 1IF x 2LO.

All values in dBc below the RF output power level.

M x N Spurious Outputs for LSB, IF = 3.3 GHz

LO = 10 – 15 GHz, 3 – 9 dBm, 25 °C

		M x f_{LO}					
		0	1	2	3	4	5
	-5	--	84	80	73	64	62
	-4	--	86	79	68	61	64
	-3	--	87	78	70	64	61
	-2	--	83	71	63	61	66
	-1	--	49	0	38	63	65
N	0	--	-3	20	27	37	53
	1	75	37	11	61	62	--
	2	84	77	64	63	63	--
	3	83	75	62	60	58	--
	4	79	74	59	60	--	--
	5	76	69	62	64	--	--

M x N Spurious Outputs for USB, IF = 3.3 GHz

LO = 11 – 15.5 GHz, 3 – 9 dBm, 25 °C

		M x f_{LO}					
		0	1	2	3	4	5
	-5	--	84	87	77	74	61
	-4	--	85	82	77	74	66
	-3	--	88	79	79	69	63
	-2	--	86	72	74	55	63
	-1	--	78	10	43	21	51
N	0	--	25	-14	1	-24	49
	1	59	52	0	35	33	63
	2	86	77	60	64	63	62
	3	85	78	69	63	61	62
	4	80	78	68	61	61	61
	5	77	71	62	60	63	60

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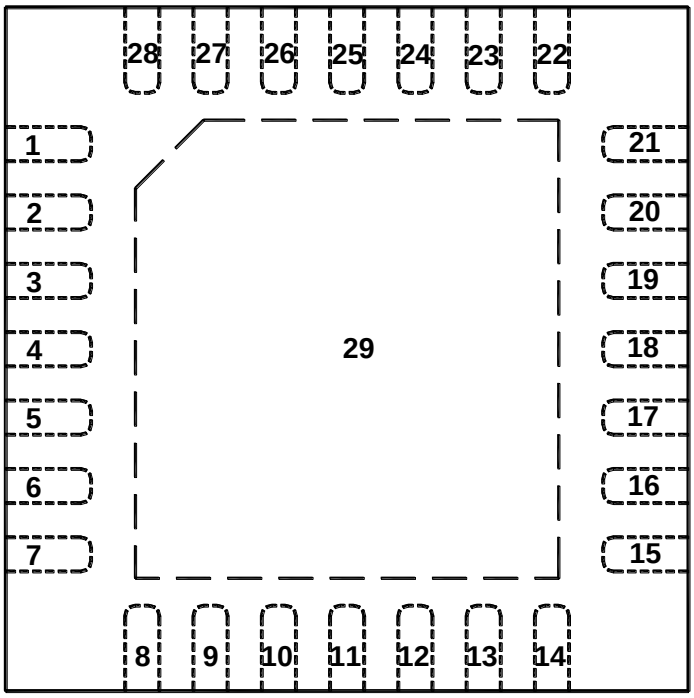
Pin Description



Pin	Symbol	Description
9,13,27	GND	These pins are tied to Pad 29 GND internally.
2	RF OUT	RF input, matched to 50 ohms
3,11,19,20,24	NC	No internal connection; can be grounded on PCB or left open
4	VCTRL2	Variable gain control for RF amplifier
5	VCTRL1	Variable gain control for RF amplifier
6	VGRF	Gate voltage for RF amplifier
10	IF2	IF input for upconverter
12	IF1	IF input for upconverter
16	LO IN	LO input for upconverter.
17	VDLO1	Drain voltage for the first stage of the LO doubler
18	VGLO	Gate bias for VDLO1 and VDLO23.
23	VDLO23	Drain voltage for stages 2 and 3 of LO doubler
25	VGX	Mixer bias voltage
26	VDRF	Drain voltage for the RF amplifier
3,11,19,20,24	N/C	No internal connection; can be grounded on PCB or left open
1,7,8,14,15,21, 22, 28,29	GND	Backside paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see 'PCB Mounting Pattern' on page 25 for suggested footprint.

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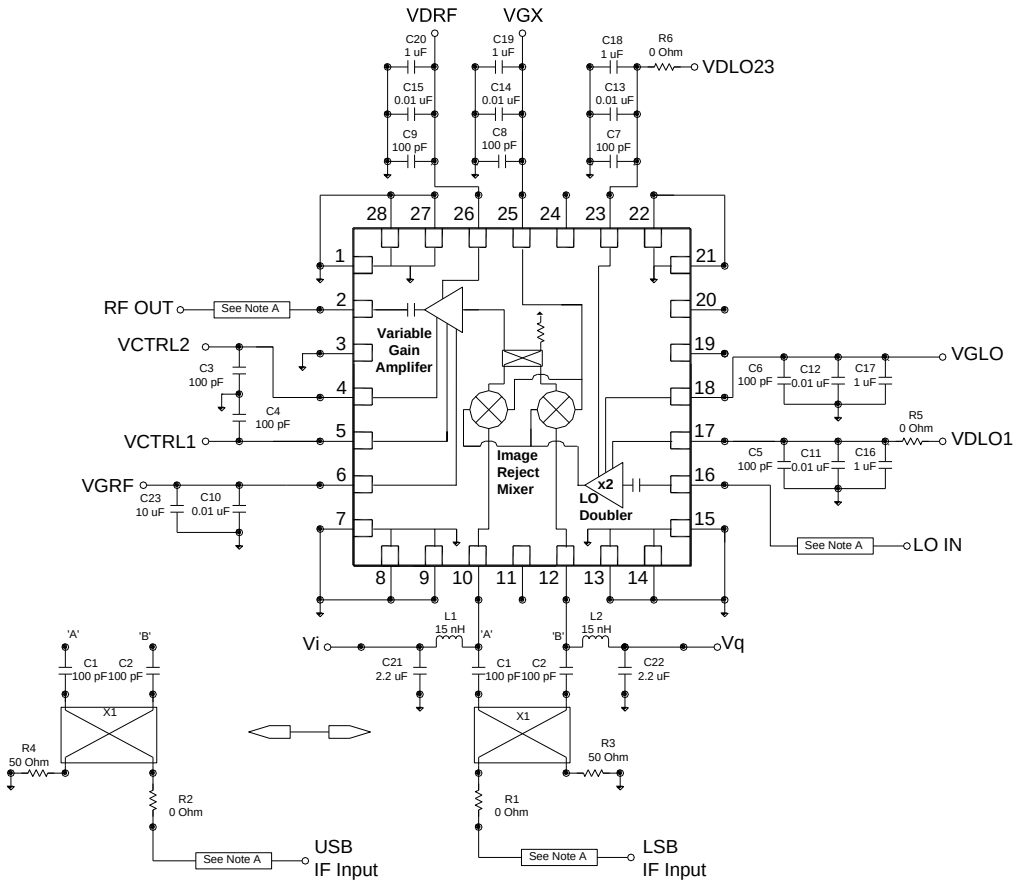
Application Circuit



Note A: 50 Ω microstrip transmission line

Bias-up Procedure	Bias-down Procedure
Set VGX to -1.2 V	Set VDLO1, VDLO23, VDRF to 0 V
Set VCTRL1 to -2.0 V	Set Vi, Vq to 0 V; if used for LO suppression
Set VCTRL2 to 0.0 V	Set VGLO, VGRF, VGX to 0 V
Set VGLO to -1.2 V	Set VCTRL1, VCTRL2 to 0 V
Set VDLO1 and VdLO23 to 3.3 V	
Set VGRF to -1.2 V	
Set VDRF to 5.0 V	
Adjust VGRF from -1.2 V towards -0.2 V until current drawn by VDRF is 345.0 mA	
If using external bias voltages for LO nulling, adjust Vi, Vq to final value for maximum LO suppression. See performance charts on page 13 'Typical Performance – External LO Nulling' for typical voltages	

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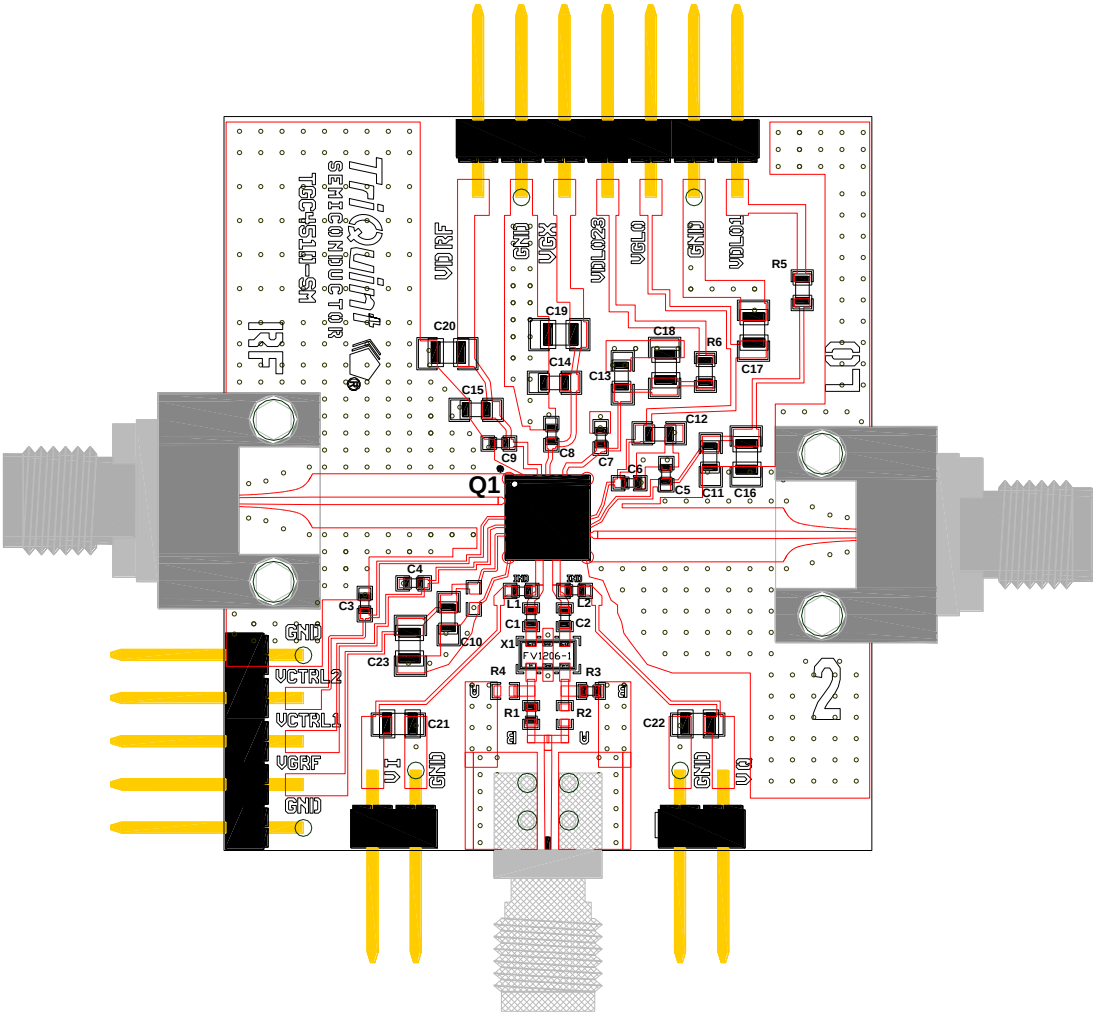
Application Circuit

PC Board Layout

Single core layer board using 0.008" thick Rogers RO4003, Єr = 3.38. Metal layers are 0.5-oz copper with patterning on top layer as shown. Bottom layer is unpatterned and is the RF and DC ground. For further technical information, refer to the TGC4510-SM Product Information page.



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Bill of Material

Ref Des	Value	Description	Manufacturer	Part Number
U1		Ku Band Upconverter	TriQuint	TGC4510-SM
X1	Case FV1206-1 1350-2450MHz	Quadrature Hybrid	MiniCircuits	QCN25+
C1, C1	10 pF	Cap, 0402, 50 V, 5%, C0G SMD		
C3 thru C9	100 pF	Cap, 0402, 50 V, 5%, C0G SMD	various	
C10 thru C15	.01 µF	Cap, 0603, 25 V, 10%, X5R SMD	various	
C16 thru C20	1.0 µF	Cap, 0805, 25 V, 10%, X5R SMD	various	
C21, C22	2.2 µF	Cap, 0805, 25 V, 10%, X5R SMD	various	
C23	2.2 µF	Cap, 0805, 25 V, 10%, X5R SMD	various	
R1 1/	0 Ω	Res, 0402, 0.06 W, 5%, SMD	various	
R3 1/	50 Ω	Res, 0402, 0.06 W, 5%, SMD	various	
R2, R4 1/		No Pop		
R2 2/	0 Ω	Res, 0402, 0.06 W, 5%, SMD		
R4 2/	50 Ω	Res, 0402, 0.06 W, 5%, SMD		
R1, R3 2/		No Pop		
R5, R6	0 Ω	Res, 0603, 0.06 W, 5%, SMD	various	
L1, L2	15 nH	Inductor, 0402	Digi-Key	535-10392-1-ND

1/ Configuration for upconverted RF using Lower Side Band
2/ Configuration for upconverted RF using Upper Side Band

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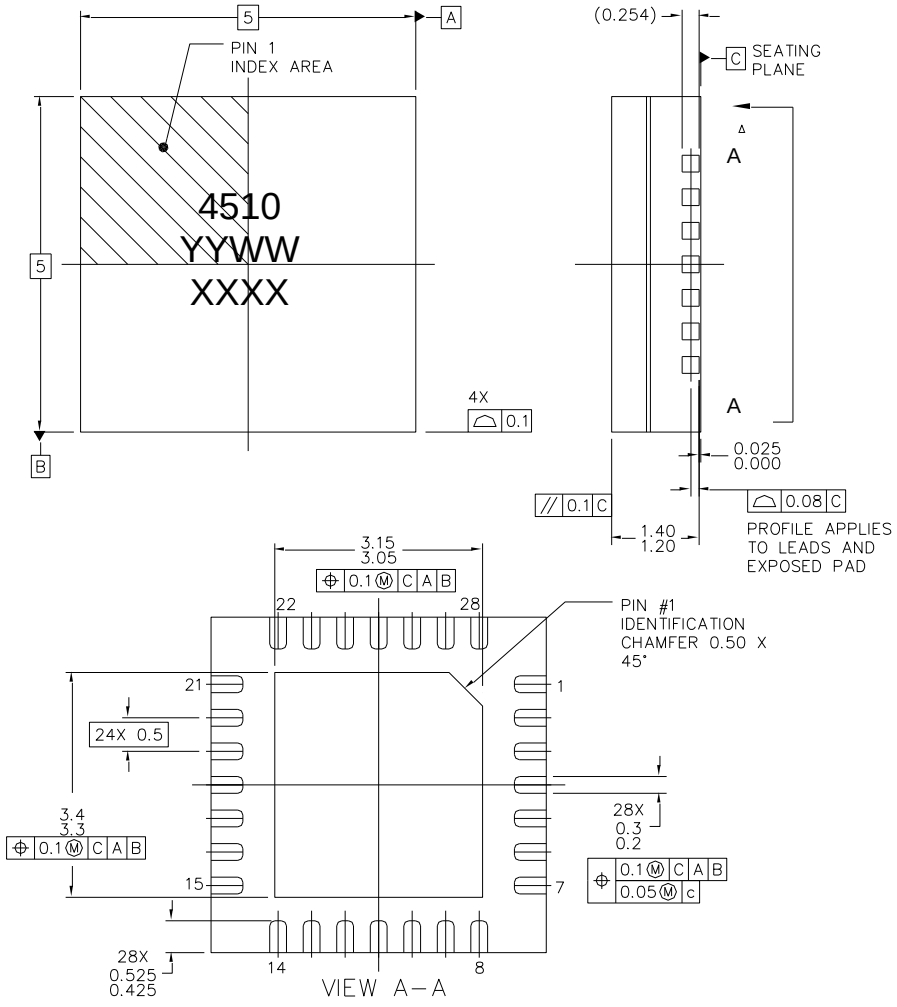
Mechanical Information

Package Marking and Dimensions

All dimensions are in millimeters.



This package is lead-free/RoHS-compliant with a copper alloy base (CDA194), and the plating material on the leads is NiPdAu. It is compatible with lead-free (maximum 260 °C reflow temperature) soldering processes.

The TGC4510-SM will be marked with the “4510” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the year the part was manufactured, the “WW” is the work week, and the “XXXX” is an auto-generated number

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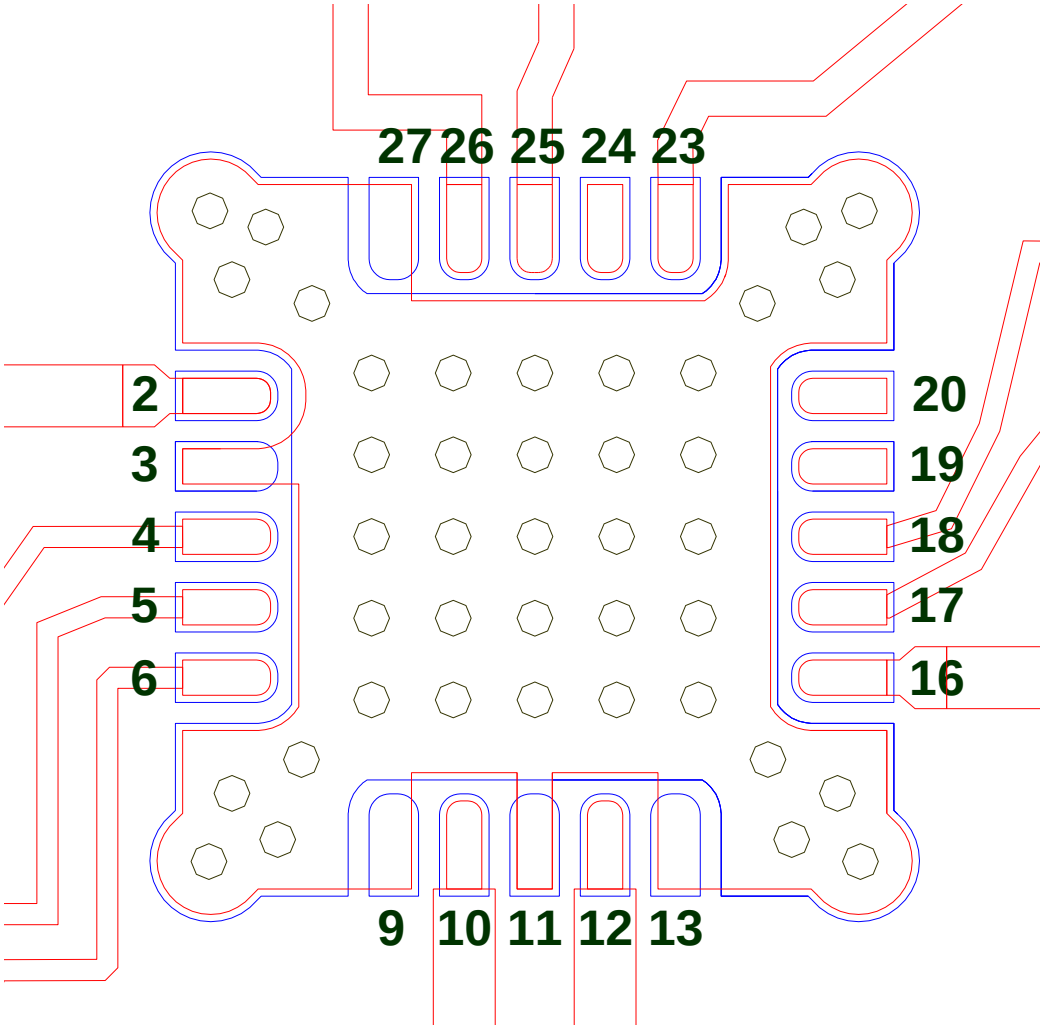
Mechanical Information

PCB Mounting Pattern



Notes:

1. The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
2. Ground vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").

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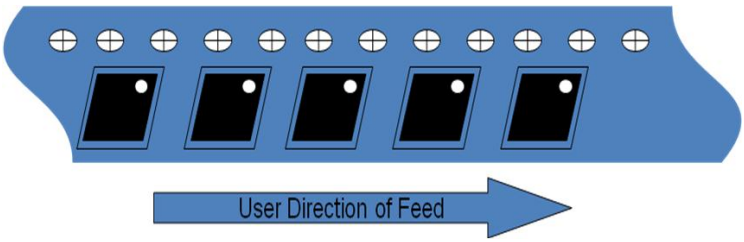
Tape and Reel Information

Tape and reel specifications for this part are also available on the TriQuint website in the “Application Notes” section.

Standard T/R size = 500 pieces on a 7” reel.

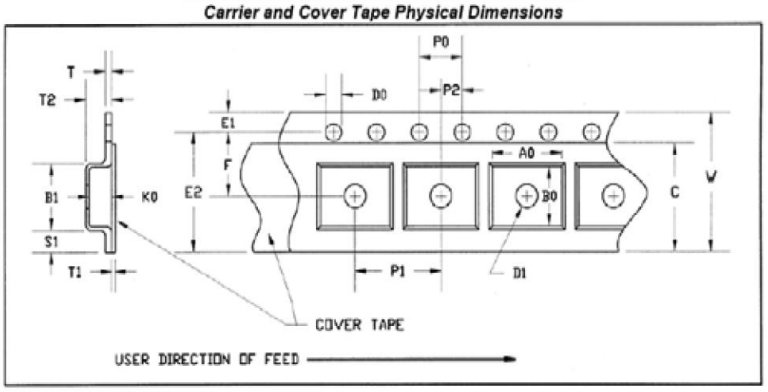


CARRIER AND COVER TAPE DIMENSIONS

Part	Feature	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.209	5.3
	Width	B0	0.209	5.3
	Depth	K0	0.064	1.65
	Pitch	P1	0.315	8.00
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12.00

Vendor: Tek-Pak P/N QFN0500x0500F-L500

Carrier and Cover Tape Physical Dimensions



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Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating: 1A
Value: Passes ≥ 250 V and < 300 V min.
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

Moisture Sensitivity Level (MSL) 1 at 260°C convection reflow per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with lead-free soldering processes, 260° maximum reflow temperature.

Package lead plating: NiPdAu

The use of no-clean solder to avoid washing after soldering is recommended.

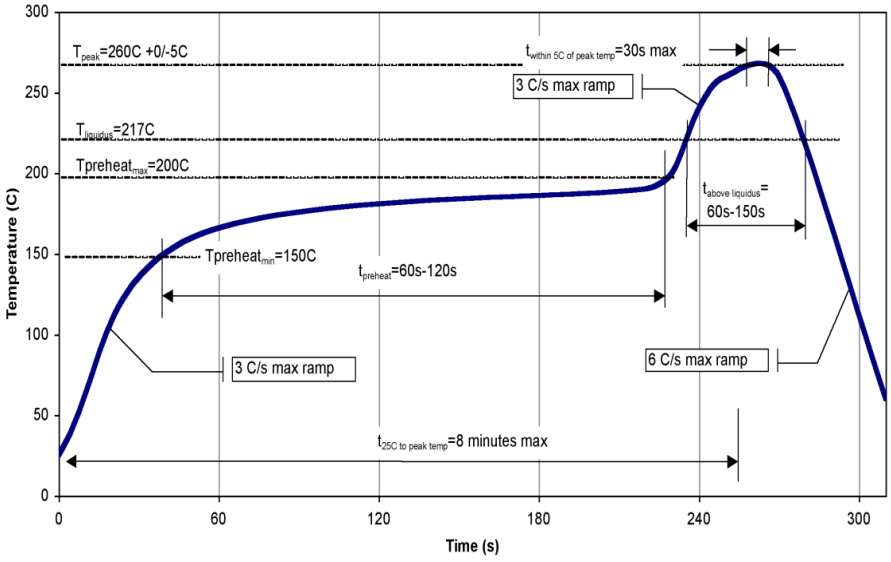
This package is not compatible with solder containing lead.

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:
Lead Free
Halogen Free (Chlorine, Bromine)
Antimony Free
TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
PFOS Free
SVHC Free

Recommended Soldering Temperature Profile



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Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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For technical questions and application information:

Email: info-networks@tqs.com

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