MAIA-009579

Receive Module
2700 - 3500 MHz

Rev. V1

Features

- Designed for Dual Polarization Receiver
- Includes Amplification, 6-bit Digital Phase Shifters and 4-bit Digital Attenuators
- Single Bit for each Phase and Attenuation Control
- High Cross-Polarization Isolation
- -20 dBm Input Power
- +5 V, -5 V Nominal Supply Voltages
- +23 dBm Output IP3
- 1.9 dB Noise Figure
- 50 Ω Impedance
- Halogen-Free “Green” Mold Compound
- RoHS* Compliant and 260°C Reflow Compatible

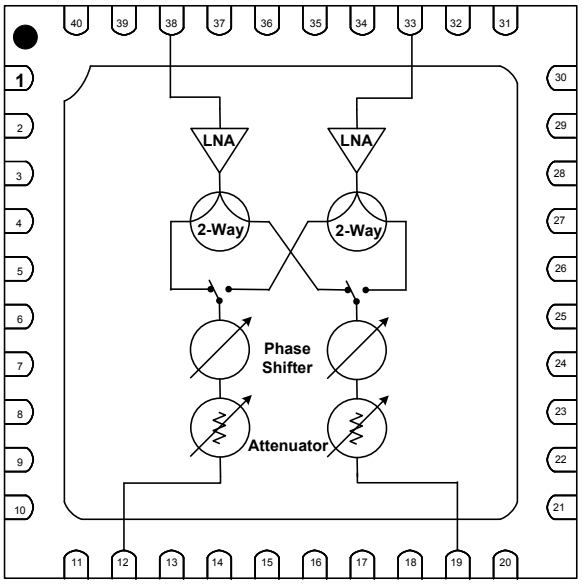
Description

The MAIA-009579 is a 2700 to 3500 MHz receive module, which is designed to be used in TR modules designed for aviation and weather radar. This module includes two channels, for horizontal and vertical inputs. Each path contains multiple amplification stages, a 4-bit digital attenuator and a 6-bit digital phase shifter. The signal path can either be straight or cross over to the opposite channel. The switches at the power divider outputs are absorptive.

This receive module is encapsulated in a low cost, miniature surface mount 6 mm 40-lead PQFN plastic package. The IC utilizes one of MACOM’s advanced 0.5 µm pHEMT processes, which has been optimized for power and low noise amplifiers, passives, and control components. This allows for a high level of integration on a single IC.

This receive module, used in conjunction with MACOM’s MAIA-010365 S-Band radar transmit module, MAAP-011022 S-Band 7 W high power amplifier, and the MADR-011007 driver, provides a complete chipset for S-Band dual polarization air traffic control and weather radar applications.

Functional Block Diagram[1]



1. The ports of the switches that connect to the power dividers are absorptive.

Ordering Information [2]

Part Number	Package
MAIA-009579-TR0500	500 piece reel
MAIA-009579-000SMB	Sample Test Board

2. Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

• **North America** Tel: 800.366.2266 / Fax: 978.366.2266
• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Pin Configuration[3,4,5]

Pin No.	Function	Pin No.	Function
1	RX1-phase 1	21	RX2-atten 4
2	RX1-phase 2	22	RX2-atten 3
3	RX1-phase 3	23	RX2-atten 2
4	RX1-phase 4	24	RX2-atten 1
5	RX1-phase 5	25	RX2-phase 6
6	RX1-phase 6	26	RX2-phase 5
7	RX1-atten 1	27	RX2-phase 4
8	RX1-atten 2	28	RX2-phase 3
9	RX1-atten 3	29	RX2-phase 2
10	RX1-atten 4	30	RX2-phase 1
11	GND	31	+5V_RX2
12	RF_RX1	32	GND
13	GND	33	RX_IN_H
14	SPDT-B	34	GND
15	-5V_LOG	35	-5V_AMP
16	+5V_LOG	36	GND
17	SPDT-A	37	GND
18	GND	38	RX_IN_V
19	RF_RX2	39	GND
20	GND	40	+5V_RX1

3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground. There must also be a way to spread the heat away from under the paddle.
4. Use 0.1 µF bypass capacitors on each bias pin (Pins 15, 16, 31, 35, and 40).
5. RX_IN_H and RX_IN_V have internal DC blocks. RF_RX1 and RF_RX2 do not have internal DC blocks.

Truth Table for Logic Bits

Bit Function	Bit Function @ Logic 0	Bit Function @ Logic 0
RX1-phase 1	Ref Phase	-5.62°
RX2-phase 1	Ref Phase	-5.62°
RX1-phase 2	Ref Phase	-11.25°
RX2-phase 2	Ref Phase	-11.25°
RX1-phase 3	Ref Phase	-22.5°
RX2-phase 3	Ref Phase	-22.5°
RX1-phase 4	Ref Phase	-45°
RX2-phase 4	Ref Phase	-45°
RX1-phase 5	Ref Phase	-90°
RX2-phase 5	Ref Phase	-90°
RX1-phase 6	Ref Phase	-180°
RX2-phase 6	Ref Phase	-180°
RX1-atten 1	Ref Loss	1 dB
RX2-atten 1	Ref Loss	1 dB
RX1-atten 2	Ref Loss	2 dB
RX2-atten 2	Ref Loss	2 dB
RX1-atten 3	Ref Loss	4 dB
RX2-atten 3	Ref Loss	4 dB
RX1-atten 4	Ref Loss	8 dB
RX2-atten 4	Ref Loss	8 dB

Where:

Logic “0” = -5 V and Logic “1” = 0 V

Truth Table, Function for SPDT_A, _B

Function	SPDT_A	SPDT_B	On Paths
Straight	0	0	RX_IN_H to RF_RX2, RX_IN_V to RF_RX1
Sequential V	0	1	RX_IN_H to RF_RX2, RX_IN_H to RF_RX1
Sequential H	1	0	RX_IN_V to RF_RX2, RX_IN_V to RF_RX1
Crossover	1	1	RX_IN_H to RF_RX1, RX_IN_V to RF_RX2

Where:

Logic “0” = -5 V and Logic “1” = 0 V

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Receive Module
2700 - 3500 MHz

Rev. V1

Electrical Specifications[6]: Freq: 2700 - 2900 MHz, T_A = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	Any Through or Crossover Path 2.7 - 3.0 GHz 3.0 - 3.5 GHz	dB	 21 18	 23 21	 26 26
Channel-to-Channel Gain Variation	Any Through or Crossover Path	dB	-1.2	-	1.2
Attenuation Accuracy	Individual Bits All Bits Combined	dB	-0.55 -1.0	-	+0.55 +1.0
Attenuation Accuracy (RMS)	RMS error of all attenuation states relative to the reference attenuation state	dB	-	0.15	-
Phase Variation (As Attenuation Changes)	Phase shift variation over all attenuation settings	deg	-	3	-
Phase Accuracy	RMS error of all phase states relative to the reference phase state	deg	-	4	-
Gain Variation (As Phase Changes)	Gain variation over all phase shift settings	dB	-	-1.3, +0.4	-
Isolation (Through Path On) RF_RX1 (relative to RF_RX2) RF_RX2 (relative to RF_RX1)	 RX_IN_H to RF_RX2 “On” RX_IN_V to RF_RX1 “On”	dB	-	 37 37	-
Isolation (Crossover Path On) RF_RX2 (relative to RF_RX1) RF_RX1 (relative to RF_RX2)	 RX_IN_H to RF_RX1 “On” RX_IN_V to RF_RX2 “On”	dB	-	 35 35	-
Input VSWR	Through or Crossover Path “On”	Ratio	-	1.6:1	-
Output VSWR	Through or Crossover Path “On”	Ratio	-	1.2:1	-
Noise Figure	Either input (RX_IN_V or RX_IN_H) to either output (RF_RX1 or RF_RX2) Reference Attenuation State 2.7 - 3.0 GHz 3.0 - 3.5 GHz 8 dB Attenuation State	dB	-	 2.0 2.4 2.0	 2.5 3.0 -
Output IP3	Either input (RX_IN_V or RX_IN_H) to either output (RF_RX1 or RF_RX2)	dBm	20	23	-
V_{IL} V_{IH}	LOW-level input voltage HIGH-level input voltage	V	-5.0 -0.2	-	-4.8 0.0
-5 V_AMP -5 V_LOG +5 V_RX1 +5 V_RX2 +5 V_LOG	- - - - -	V	-5.10 -5.25 4.75 4.75 4.75	-5.0 -5.0 5.0 5.0 5.0	-4.90 -4.75 5.25 5.25 5.25
I_-5 V_AMP I_-5 V_LOG I_+5 V_RX1 I_+5 V_RX2 I_+5 V_LOG	-5 V_AMP = -5 V -5 V_LOG = -5 V +5 V_AMPH = +5 V +5 V_AMPV = +5 V +5 V_LOG = +5 V	mA	-	2 4 155 155 6	-

6. Unless otherwise noted:
+5 V_RX1 = +5 V_RX2 = +5 V_LOG = +5 V, -5 V_AMP = -5 V_LOG = -5 V, RX_In_Vert or RX_In_Horiz = -20 dBm

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Absolute Maximum Ratings[7,8]

Parameter	Absolute Maximum
-5 V_AMP, -5 V_LOG	-6.0 V to +0.5 V
+5 V_RX1, +5 V_RX2, +5 V_LOG	-0.5 V to +6.0 V
All RX… Controls	-5 V_AMP - 0.5 V to +0.5 V
RX_IN_V, RX_IN_H	+18 dBm
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +125°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

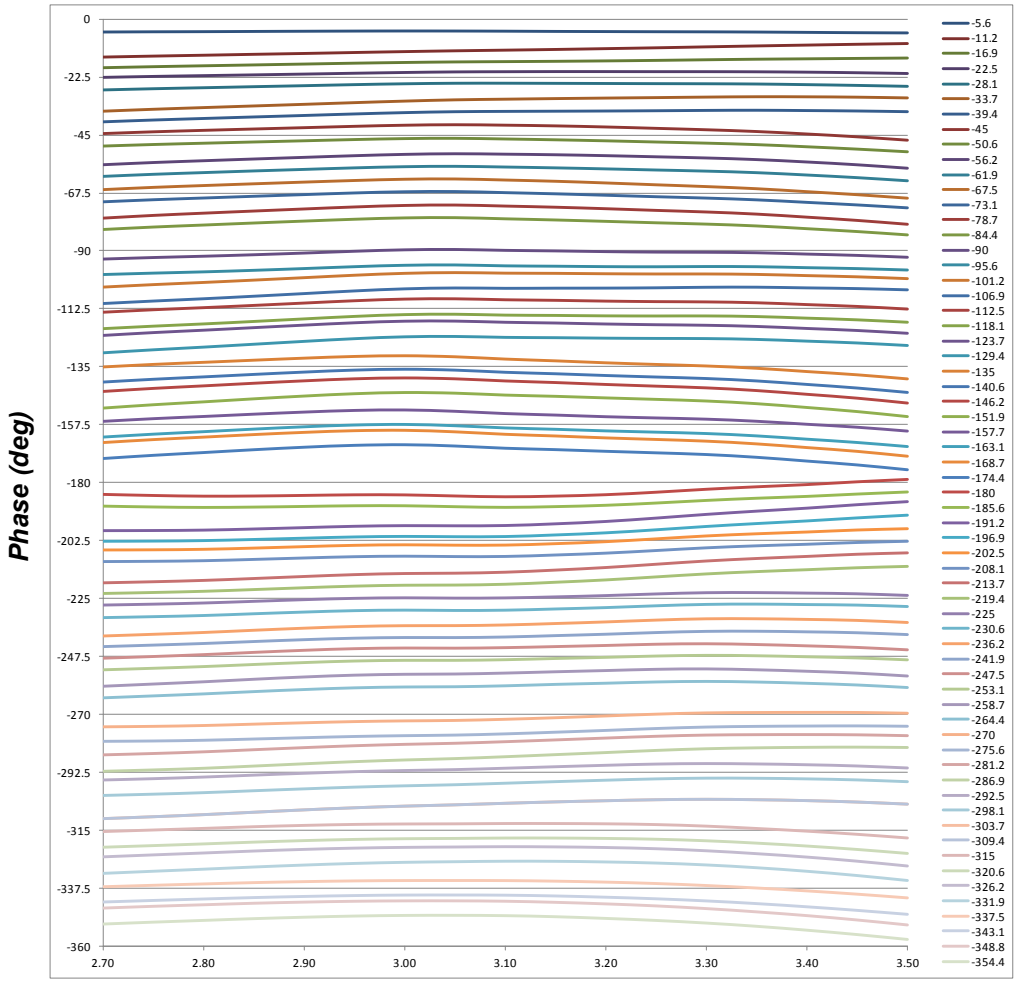
Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1A HBM devices.

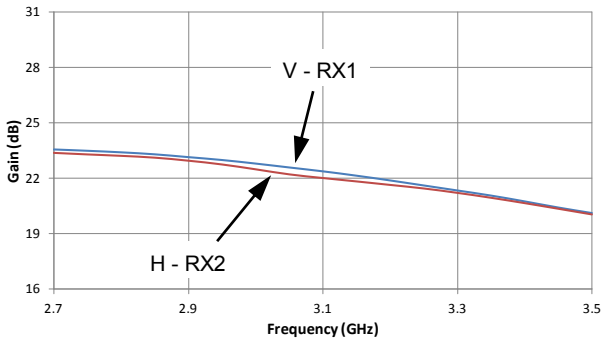
Typical Performance Curves

All Phase States at 0 dB Attenuation

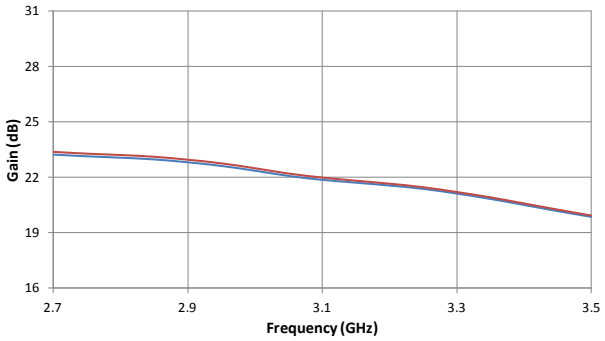


Typical Performance Curves

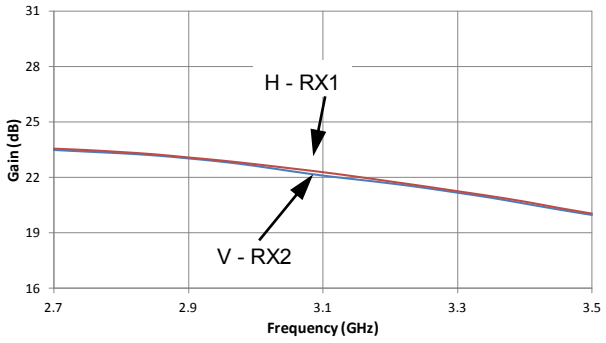
Gain - Straight Path



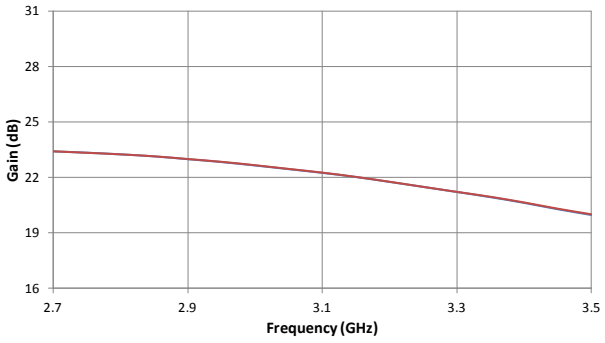
Gain - Sequential V



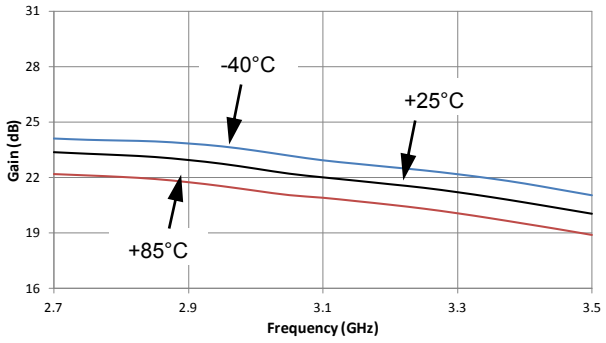
Gain - Crossover Path



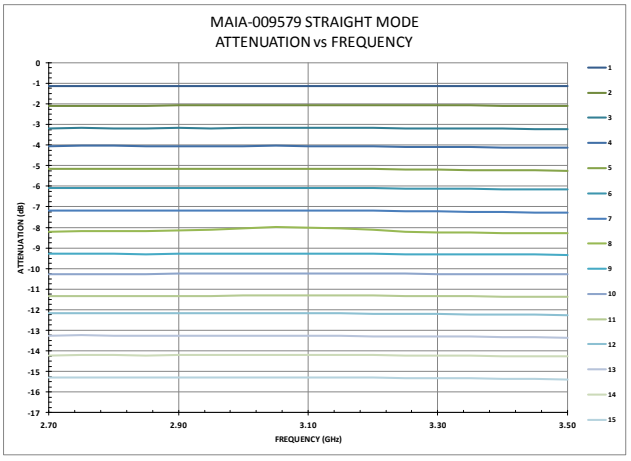
Gain - Sequential H



Gain - Straight Path Variation over Temperature



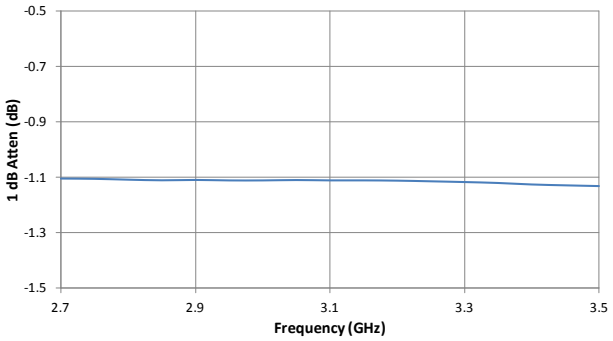
All Attenuation States at 0° Phase Shift



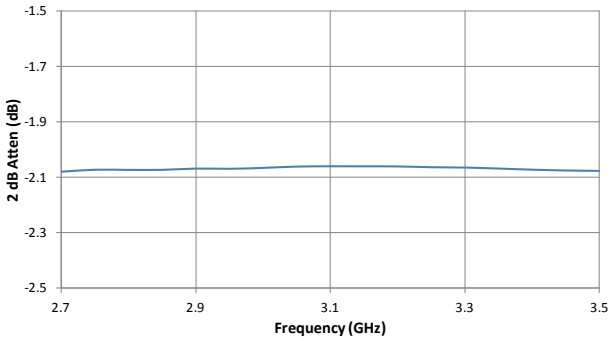
Typical Performance Curves:

Plots are for "RXINV to RFRX1" and "RXINH to RFRX2" (through path).

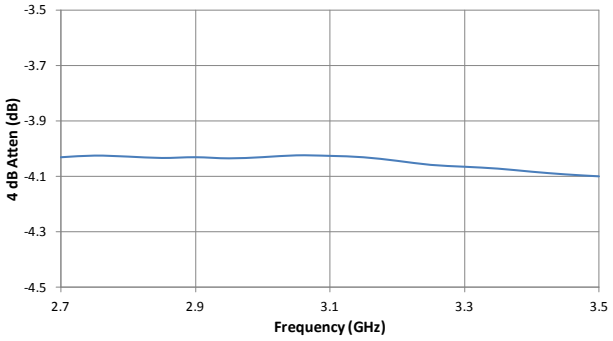
Attenuation 1 dB Bit:



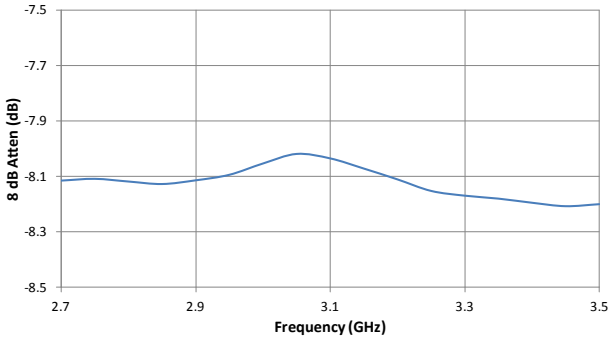
Attenuation 2 dB Bit



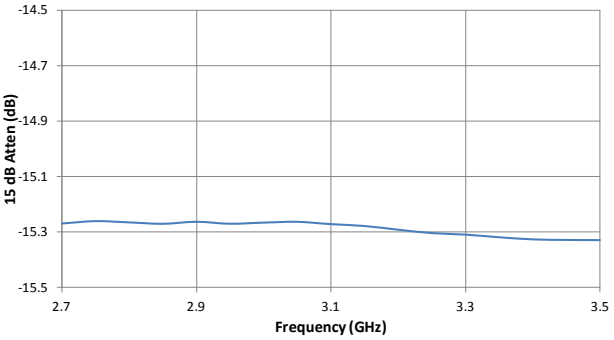
Attenuation 4 dB Bit



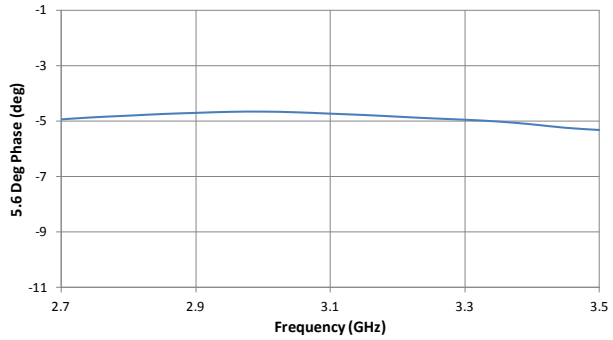
Attenuation 8 dB Bit



Attenuation @ Max. Atten. (15 dB Nominal)



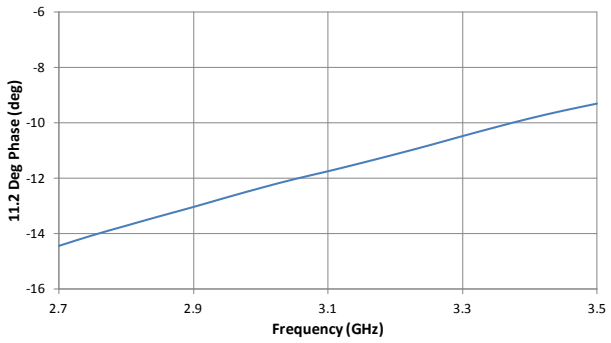
Phase 5.6 deg Bit



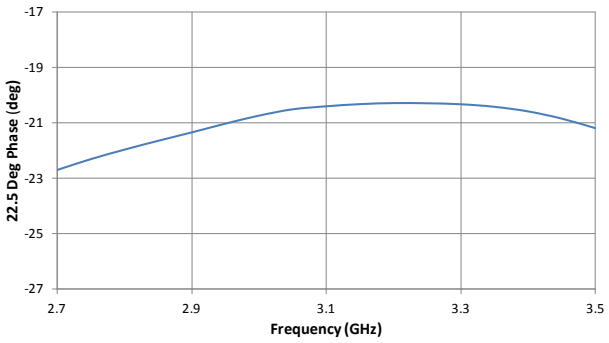
Typical Performance Curves:

Plots are for "RXINV to RFRX1" and "RXINH to RFRX2" (through path).

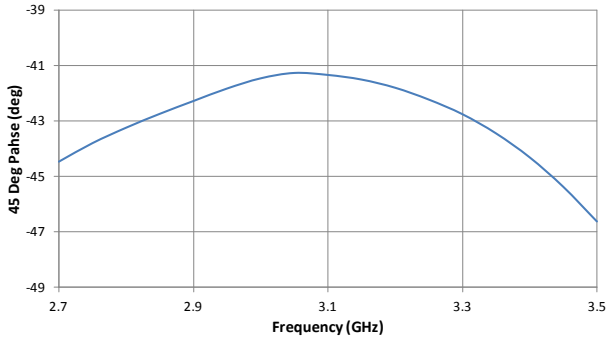
Phase 11.2 deg Bit



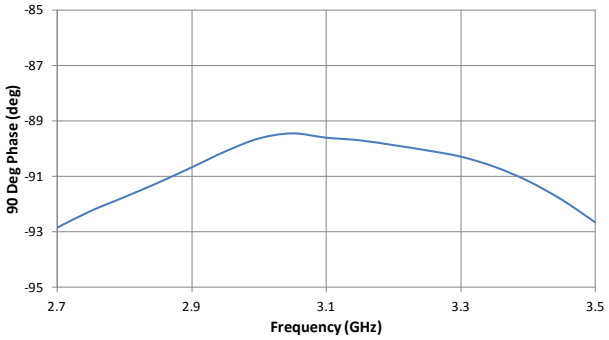
Phase 22.5 deg Bit



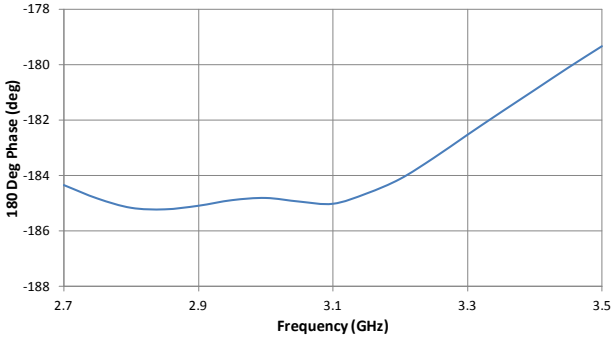
Phase 45 deg Bit



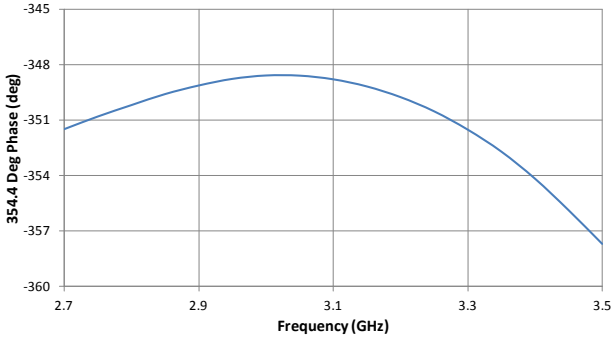
Phase 90 deg Bit



Phase 180 deg Bit

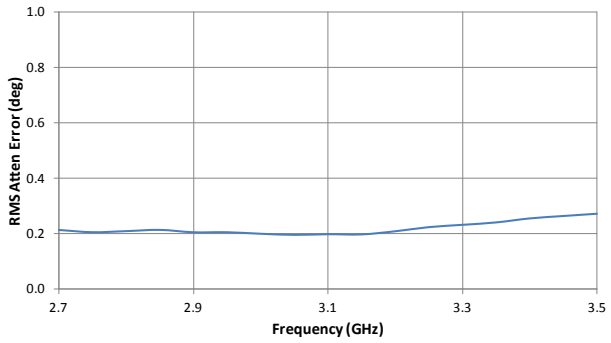


Phase @ Max. Phase (354.4° Nominal)

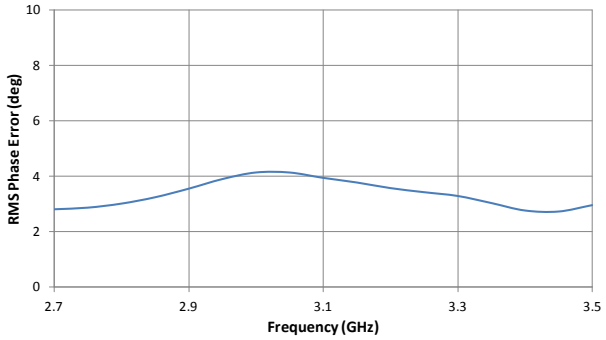


Typical Performance Curves

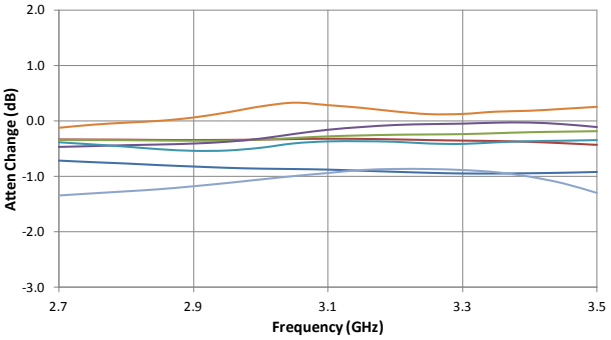
RMS Attenuation Error
All Phase States (-5.6° through –354.4°)



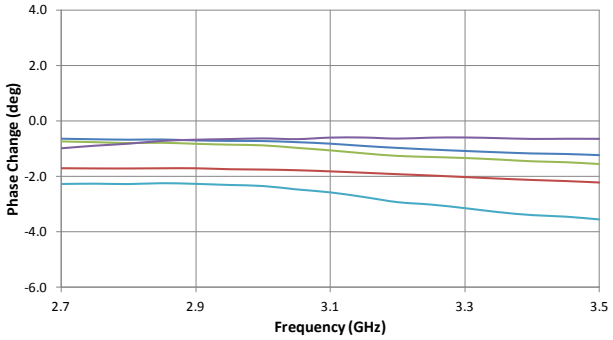
RMS Phase Error
All Attenuation States (1 dB through 15 dB)



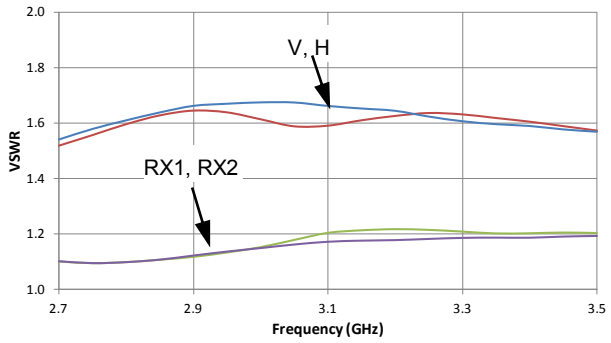
Attenuation Change vs. Phase State; (Reference Attenuation State) (Individual and Sum of Bits)



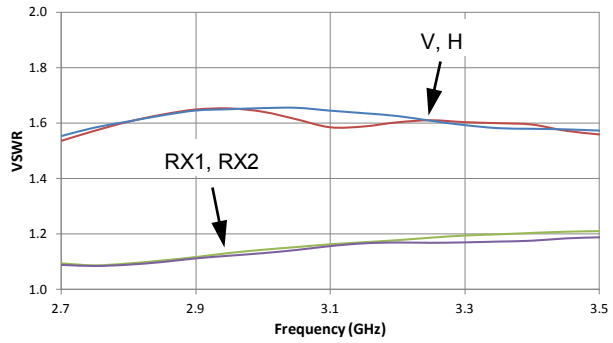
Phase Change vs. Attenuation State; Reference Phase State) (Individual and Sum of Bits)



VSWR:
Through Paths, Reference State

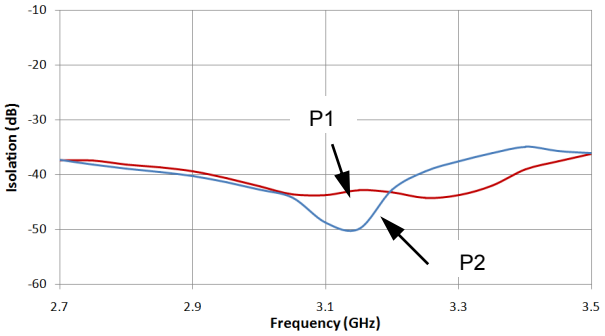


VSWR:
Crossover Paths, Reference State

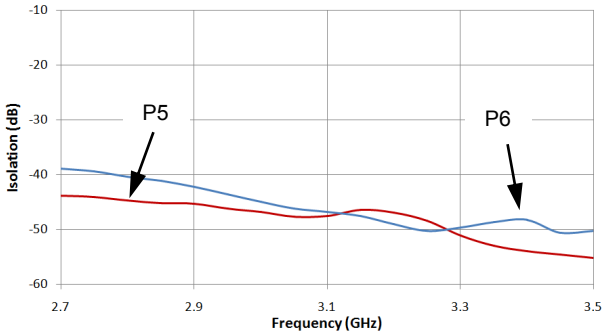


Typical Performance Curves

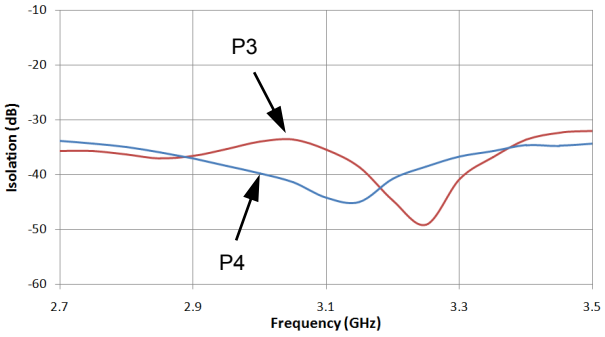
Isolation—Through Path [9,10]



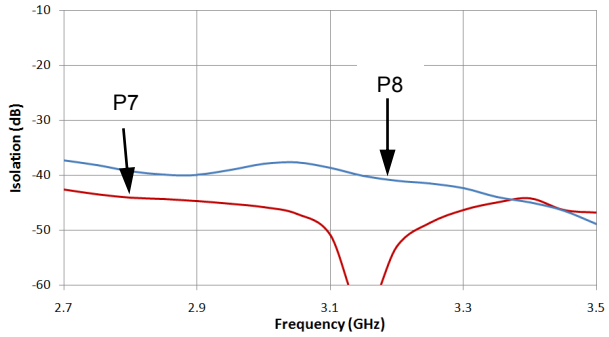
Isolation—Sequential V [13,14]



Isolation—Crossover Path [11,12]



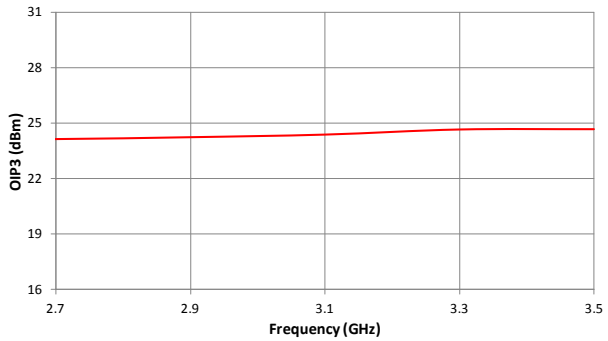
Isolation—Sequential H [15,16]



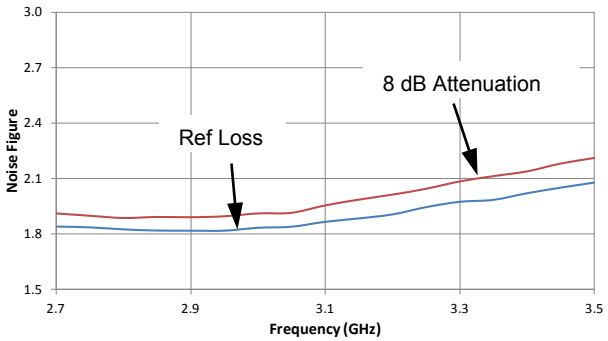
9. (P1) is how far the RFRX2 output is below RFRX1 when RXINV to RFRX1 as the "ON" state.
10. (P2) is how far the RFRX1 output is below RFRX2 when RXINH to RFRX2 as the "ON" state.
11. (P3) is how far the RFRX2 output is below RFRX1 when RXINH to RFRX1 as the "ON" state.
12. (P4) is how far the RFRX1 output is below RFRX2 when RXINV to RFRX2 as the "ON" state.

13. (P5) is the isolation from RFRX1 to RFRX2 when RXINV to RFRX1 and RXINV to RFRX2 are in the "ON" state.
14. (P6) is the isolation from RFRX2 to RFRX1 when RXINV to RFRX1 and RXINV to RFRX2 are in the "ON" state.
15. (P7) is the isolation from RFRX2 to RFRX1 when RXINH to RFRX1 and RXINH to RFRX2 are in the "ON" state.
16. (P8) is the isolation from RFRX1 to RFRX2 when RXINH to RFRX1 and RXINH to RFRX2 are in the "ON" state.

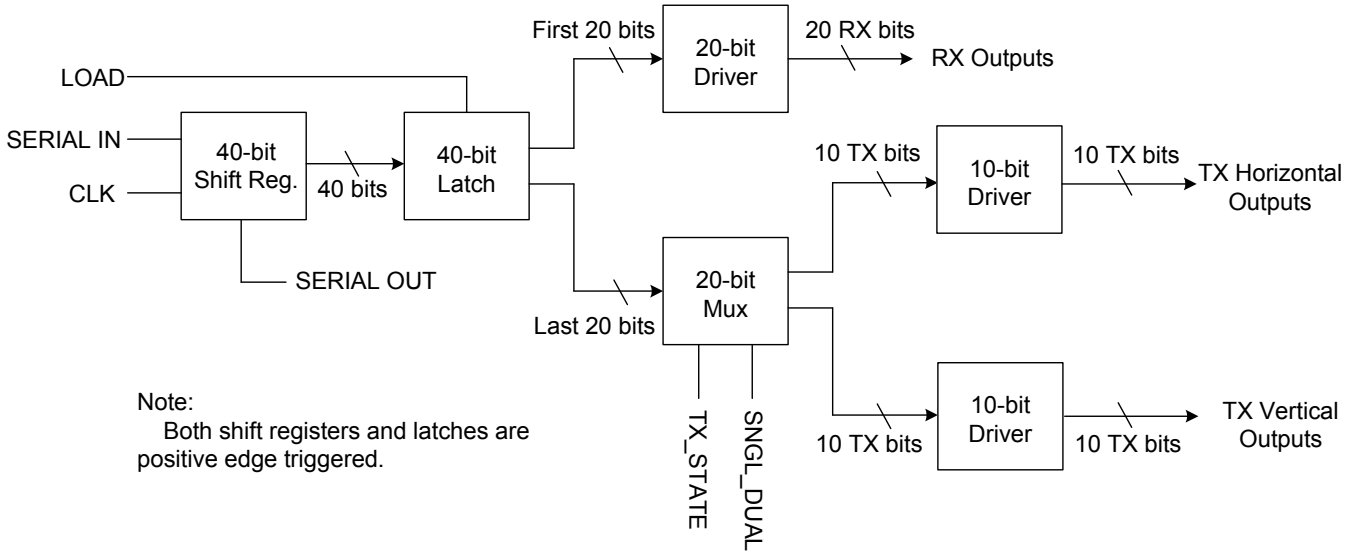
Output IP3



Noise Figure (Reference State and 8 dB Attenuation)



Functional Diagram of Companion MADR-011007 Driver



Note:
Both shift registers and latches are positive edge triggered.

Serial Bit Stream Definition[17,18]

Bit No.	Bit Function	Bit No.	Bit Function
1	RX2-phase 1	21	TX-phase 1-A
2	RX2-phase 2	22	TX-phase 1-B
3	RX2-phase 3	23	TX-phase 2-A
4	RX2-phase 4	24	TX-phase 2-B
5	RX2-phase 5	25	TX-phase 3-A
6	RX2-phase 6	26	TX-phase 3-B
7	RX2-atten 1	27	TX-phase 4-A
8	RX2-atten 2	28	TX-phase 4-B
9	RX2-atten 3	29	TX-phase 5-A
10	RX2-atten 4	30	TX-phase 5-B
11	RX1-phase 1	31	TX-phase 6-A
12	RX1-phase 2	32	TX-phase 6-B
13	RX1-phase 3	33	TX-atten 1-A
14	RX1-phase 4	34	TX-atten 1-B
15	RX1-phase 5	35	TX-atten 2-A
16	RX1-phase 6	36	TX-atten 2-B
17	RX1-atten 1	37	TX-atten 3-A
18	RX1-atten 2	38	TX-atten 3-B
19	RX1-atten 3	39	TX-atten 4-A
20	RX1-atten 4	40	TX-atten 4-B

17. Bit No.1 should be the first bit going into the serial interface.
18. Only bits 1-20 are used for the receive module. All 40 bits need to be provided for the driver to control the receive module. Bits 21-40 are “X” (don’t care), but must be high or low.

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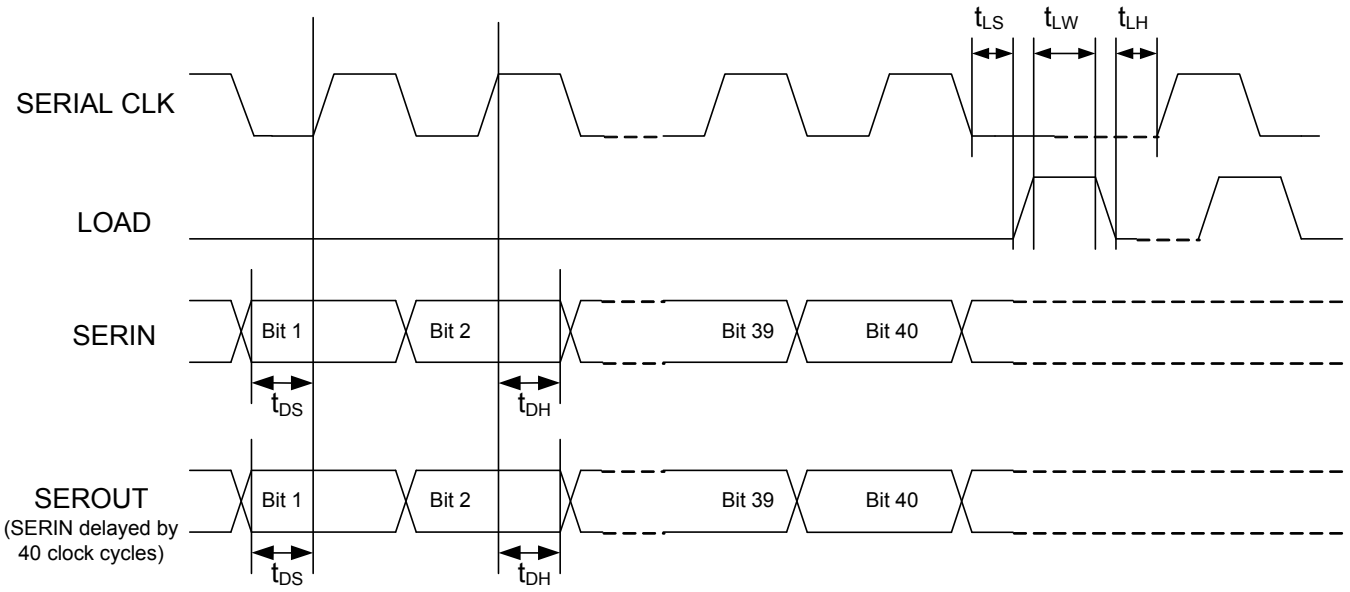
Serial Interface Timing Diagram



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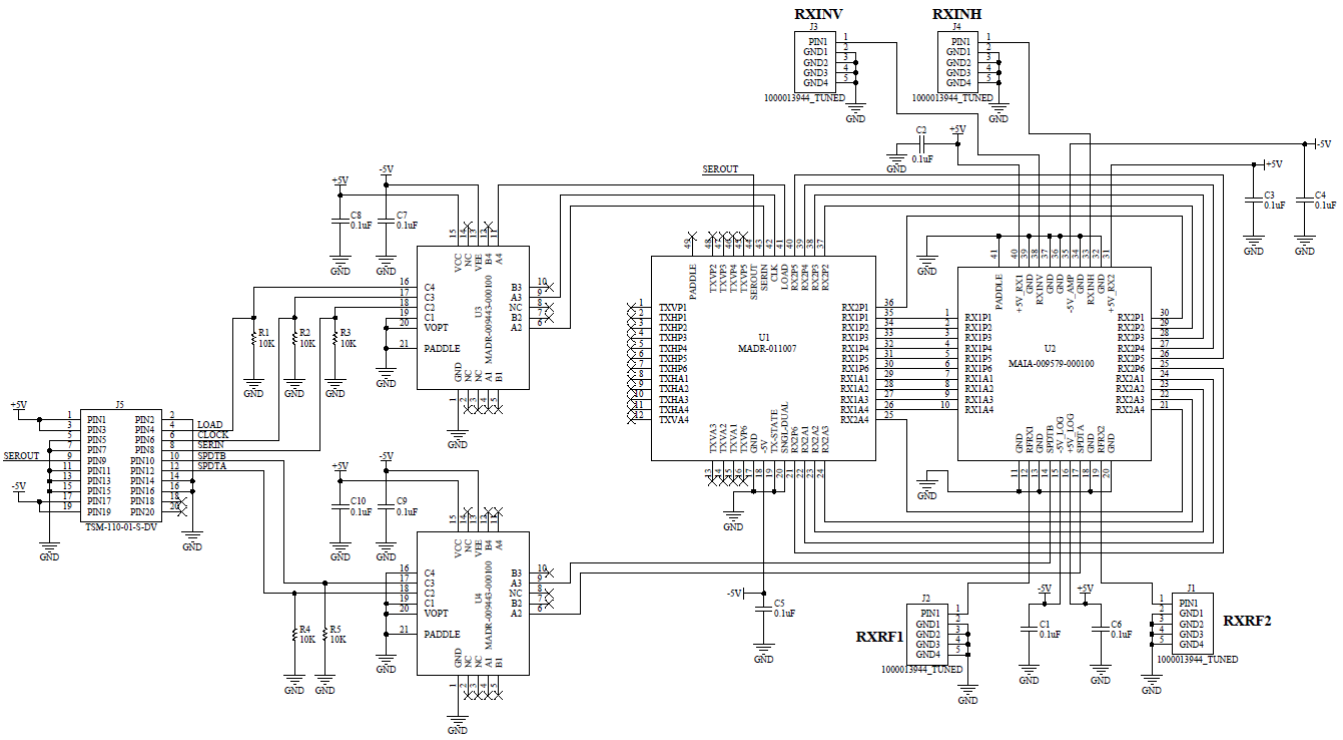
Sample Board Schematic with Off-Chip Components



Sample Board Pin BOM

Qty	Name	Mfg	Description	Ref Des
1	MAIA-009579-000100	M/A-COM Tech	RX IC,Limit,PD,Amp,Phase/Atten Cont.	U2
5			Resistor,0402,1%,1/16W,10K Ohms,SMT	R1-R5
10			Capacitor,0402,16V,X7R,10%,0.1uF,SMT	C1-C10
2	MADR-009443-000100	M/A-COM Tech	Quad FET and PIN driver, 4x4 mm PQFN	U3, U4
1	MADR-011007-000100	M/A-COM Tech	Driver, MPAR Digital Control	U1

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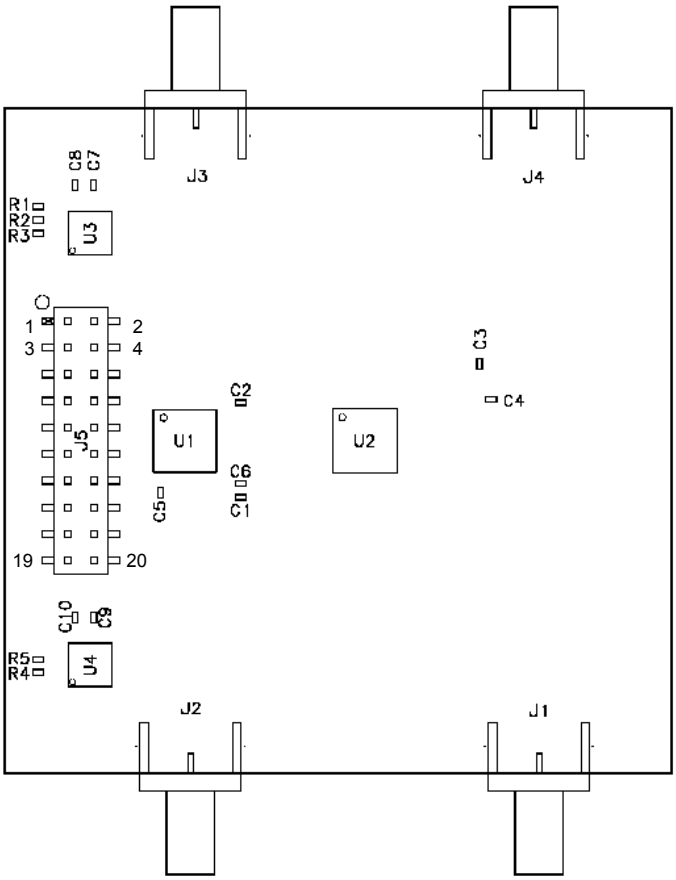
Sample Board Pin Configuration



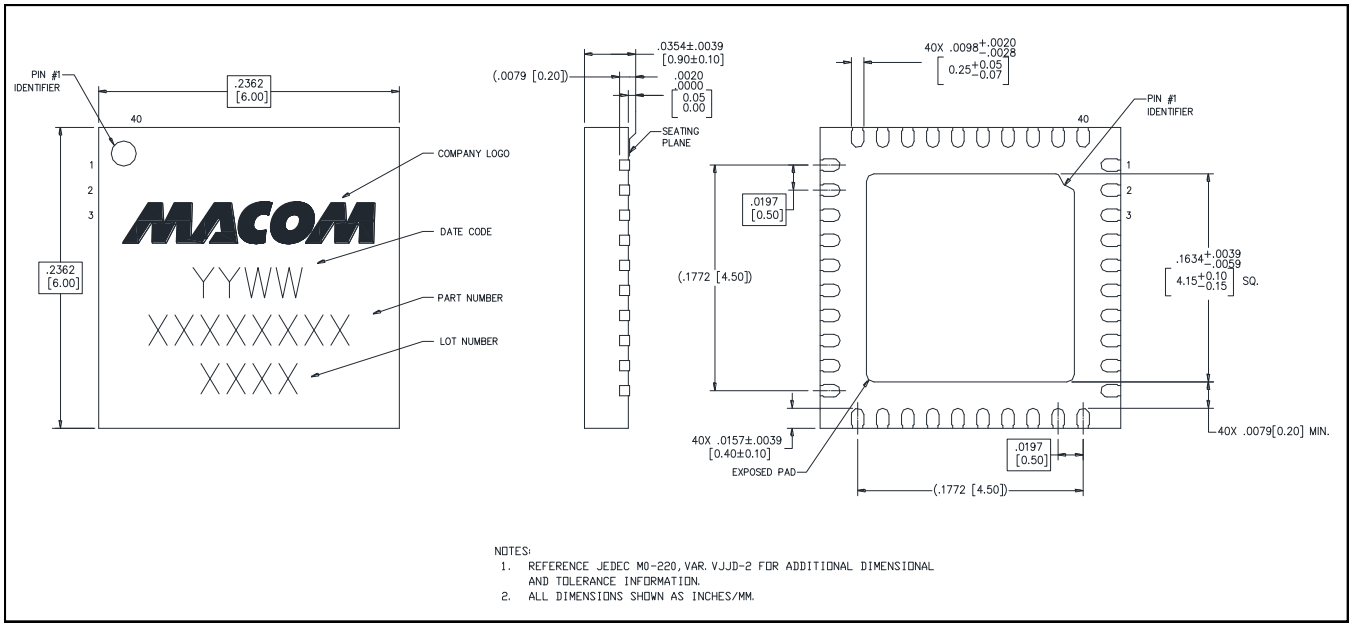
RF Pin Configuration

Connector Ref Des	Port Name
J1	RF_RX2
J2	RF_RX1
J3	RX_IN_V
J4	RX_IN_H

Pin Configuration J5

Pin No.	Function	Pin No.	Function
1	+5V	11	GND
2	GND	12	SPDTA
3	+5V	13	GND
4	LOAD	14	GND
5	GND	15	GND
6	CLOCK	16	GND
7	GND	17	-5V
8	SERIN	18	NC
9	SEROUT	19	-5V
10	SPDTB	20	NC

Lead-Free 6 mm 40-Lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is NiPdAuAg.

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