MAIA-010365

Transmit Module
2700 - 3500 MHz

Rev. V1

Features

- Provides Outputs for Vertical and Horizontal Polarizations
- Includes Amplification, Digital Phase Shifters and Digital Attenuators
- Single Bit for Each Phase and Attenuation Control
- High Output to Output and Output to Input Isolation
- +5 V, -5 V Nominal Supply Voltages
- +23 dBm Output P_{1dB}
- 50 Ohm Impedance
- Halogen-Free "Green" Mold Compound
- RoHS Compliant and 260°C Reflow Compatible

Description

The MAIA-010365 is a 2700 to 3500 MHz transmit module, which is designed for TR modules used in aviation and weather radar. This module includes an input power divider which is used to feed vertical and horizontal gain cascades. Each path contains multiple amplification stages, digital attenuators and digital phase shifters. The transmit module is encapsulated in a low cost, miniature surface mount PQFN, 6 mm square, 40 lead plastic package. The IC utilizes one of MACOM's advanced 0.5 µm pHEMT processes, which has been optimized for power and low noise amplifiers, passives, and control components. This allows for a high level of integration on a single IC.

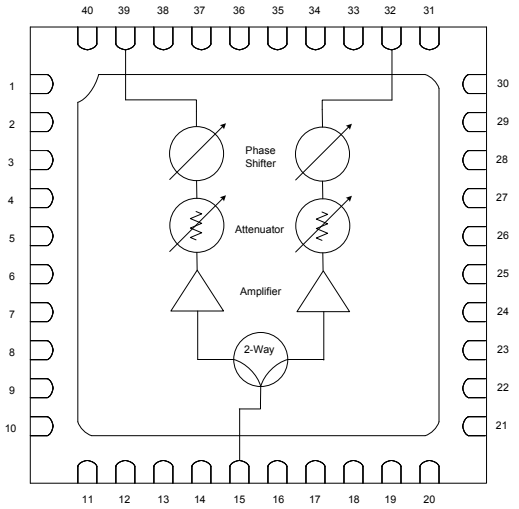
The transmit module, used in conjunction with MACOM's MAIA-009579 S-Band radar receive module, MAAP-011022 S-Band 6.5 W high power amplifier, and the MADR-011007 driver, provides a complete chipset for S-Band dual polarization air traffic control and weather radar applications.

Ordering Information[1]

Part Number	Package
MAIA-010365-TR0500	500 piece reel
MAIA-010365-001SMB	Sample Test Board

1. Reference Application Note M513 for reel size information.

Functional Block Diagram



Pin Configuration[2,3,4]

Pin No.	Function	Pin No.	Function
1	TX2-phase 1	21	TX1-atten 4
2	TX2-phase 2	22	TX1-atten 3
3	TX2-phase 3	23	TX1-atten 2
4	TX2-phase 4	24	TX1-atten 1
5	TX2-phase 5	25	TX1-phase 6
6	TX2-phase 6	26	TX1-phase 5
7	TX2-atten 1	27	TX1-phase 4
8	TX2-atten 2	28	TX1-phase 3
9	TX2-atten 3	29	TX1-phase 2
10	TX2-atten 4	30	TX1-phase 1
11, 13, 14, 16, 18, 20	GND	31, 33, 35, 37, 38, 40	GND
12	+5 V_AMPV	32	TX_OUT_H
15	BMFMR_IN	34	-5 V_LOG
17	-5 V_AMP	36	+5 V_LOG
19	+5 V_AMPH	39	TX_OUT_V

2. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground. There must also be a way to spread the heat away from under the paddle.
3. Use 0.1 µF bypass capacitors on each bias pin (Pins 12, 17, 19, 34, and 36).
4. None of the RF Ports (BMFMR_IN, TX_OUT_H, and TX_OUT_V) have internal DC blocks.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Transmit Module
2700 - 3500 MHz

Rev. V1

Electrical Specifications: (Unless otherwise noted)
Freq. = 2700 - 3500 MHz, T_A = 25°C, Z_0 = 50 Ω,
BMFMR_IN = +5 dBm,+5 V_AMPH = +5 V_AMPV = +5 V, -5 V_AMP = -5.0 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	-	dB	9.0	10.5	-
Gain Variation	Channel-to-Channel	dB	-1.2	-	1.2
Attenuation Accuracy	Individual Bits All Bits Combined	dB	-0.55 -1.0	-	+0.55 +1.0
Phase Variation (As Attenuation Changes)	Phase shift variation over all attenuation settings	deg	-	3	-
Phase Accuracy	-	deg rms	-	6	-
Gain Variation (As Phase Changes)	Gain variation over all phase shift settings	dB	-	-1.3, +0.4	-
Isolation (Output to Output) TXOUTH to TXOUTV TXOUTV to TXOUTH	-	dB	-	 45 45	-
Isolation (Output to Input) TXOUTH to BMFMR_IN TXOUTV to BMFMR_IN	-	dB	-	 70 70	-
Input VSWR	-	Ratio	-	1.5:1	-
Output VSWR	-	Ratio	-	1.5:1	-
1 dB Compression Point	-	dBm	-	+22	-
Output IP3	-	dBm	-	+30	-
V_{IL} V_{IH}	LOW-level input voltage HIGH-level input voltage	V	-5.0 -0.2	— —	-4.8 0.0
-5 V_AMP -5 V_LOG +5 V_AMPH +5 V_AMPV +5 V_LOG	-	V	-5.10 -5.25 4.75 4.75 4.75	-5.0 -5.0 5.0 5.0 5.0	-4.90 -4.75 5.25 5.25 5.25
I_-5 V_AMP I_-5 V_LOG I_+5 V_AMPH I_+5 V_AMPV I_+5 V_LOG	-5 V_AMP = -5 V -5 V_LOG = -5 V +5 V_AMPH = +5 V +5 V_AMPV = +5 V +5 V_LOG = +5 V	mA	-	4 2 265 265 5	-

Absolute Maximum Ratings[5,6]

Parameter	Absolute Maximum
-5 V_AMP, -5 V_LOG	-6.0 V to +0.5 V
+5 V_AMPH, +5 V_AMPV, +5 V_LOG	-0.5 V to +6.0 V
All TX… Controls	-5 V_AMP - 0.5 V to +0.5 V
BMFMR_IN	+18 dBm
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +125°C

5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1A HBM devices.

Truth Table for Logic Bits

Bit Function	Bit Function @ Logic 0	Bit Function @ Logic 1
TX1-phase 1	Ref Phase	-5.62°
TX2-phase 1	Ref Phase	-5.62°
TX1-phase 2	Ref Phase	-11.25°
TX2-phase 2	Ref Phase	-11.25°
TX1-phase 3	Ref Phase	-22.5°
TX2-phase 3	Ref Phase	-22.5°
TX1-phase 4	Ref Phase	-45°
TX2-phase 4	Ref Phase	-45°
TX1-phase 5	Ref Phase	-90°
TX2-phase 5	Ref Phase	-90°
TX1-phase 6	Ref Phase	-180°
TX2-phase 6	Ref Phase	-180°
TX1-atten 1	Ref Loss	1 dB
TX2-atten 1	Ref Loss	1 dB
TX1-atten 2	Ref Loss	2 dB
TX2-atten 2	Ref Loss	2 dB
TX1-atten 3	Ref Loss	4 dB
TX2-atten 3	Ref Loss	4 dB
TX1-atten 4	Ref Loss	8 dB
TX2-atten 4	Ref Loss	8 dB

Where:

Logic “0” = -5 V
Logic “1” = 0 V

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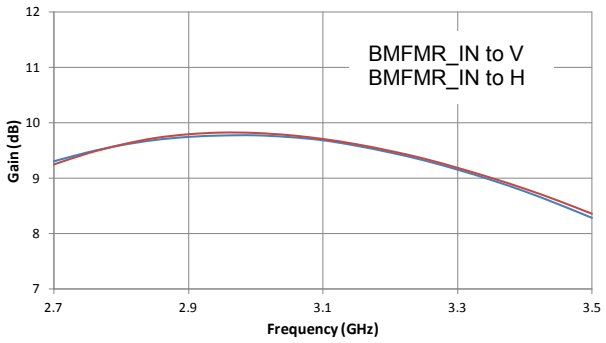
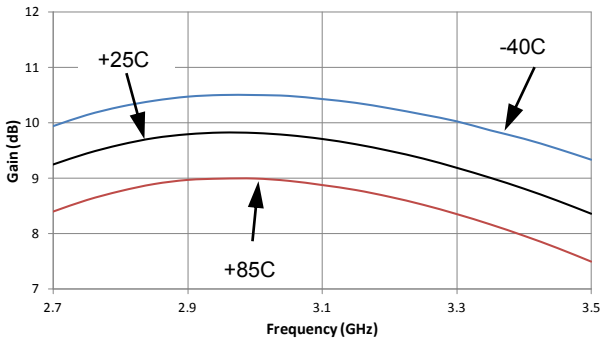
Typical Performance Curves

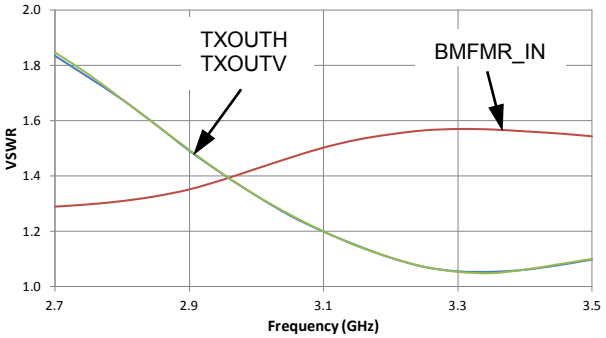
Gain



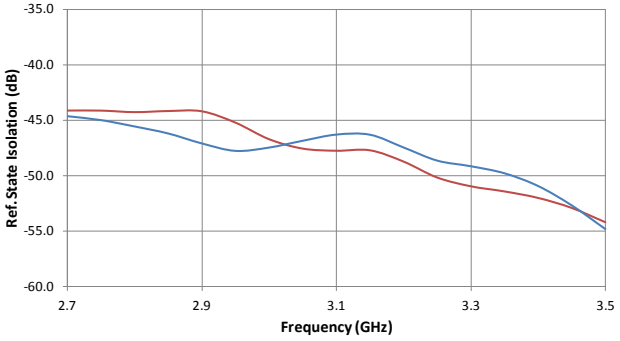
Gain Over Temperature



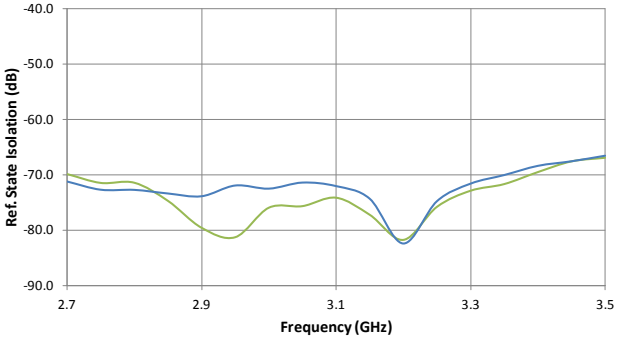
VSWR - BMFMR_IN to TXOUTV (Reference State)



Isolation - Output to Output

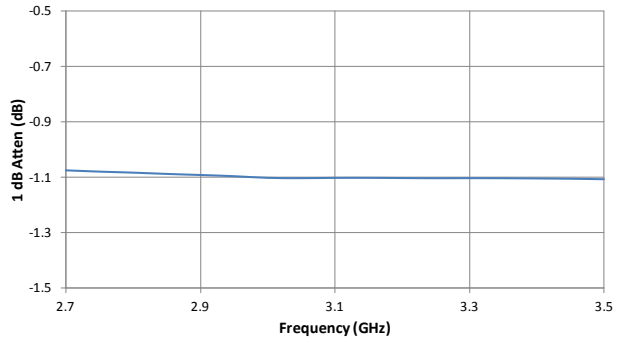


Isolation - Output to Input

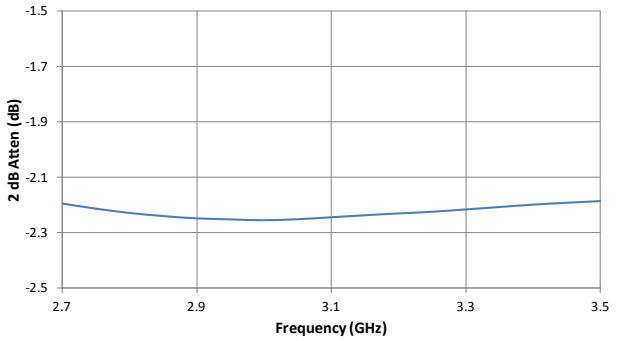


Typical Performance Curves

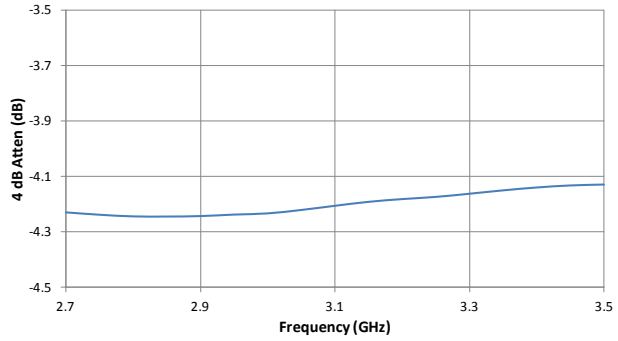
Attenuation 1 dB Bit



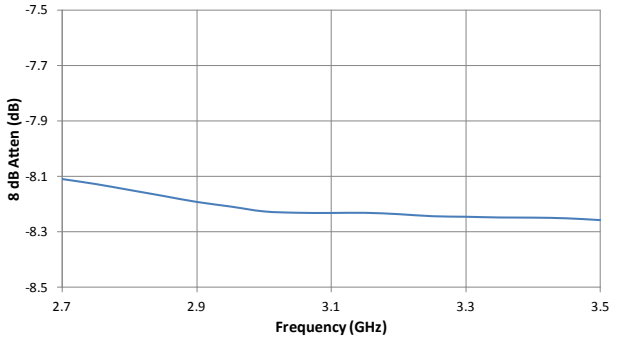
Attenuation 2 dB Bit



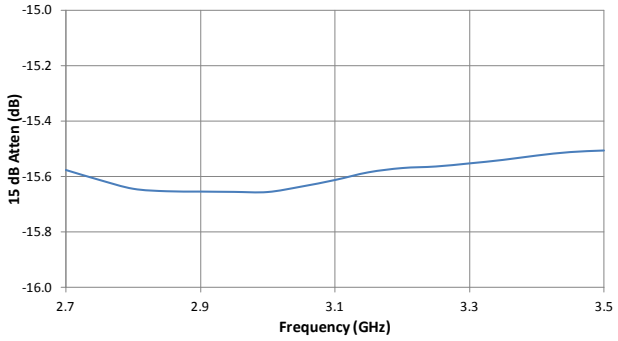
Attenuation 4 dB Bit



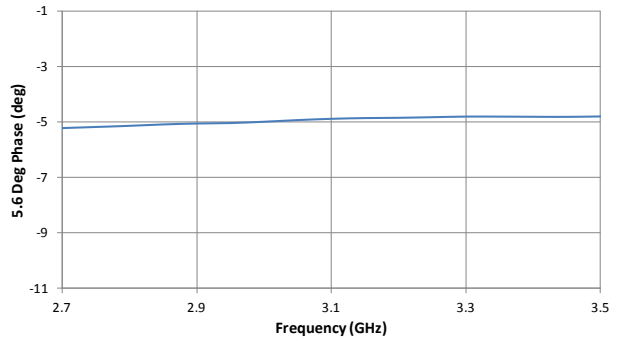
Attenuation 8 dB Bit



Attenuation @ Max. Atten. (15 dB Nominal)

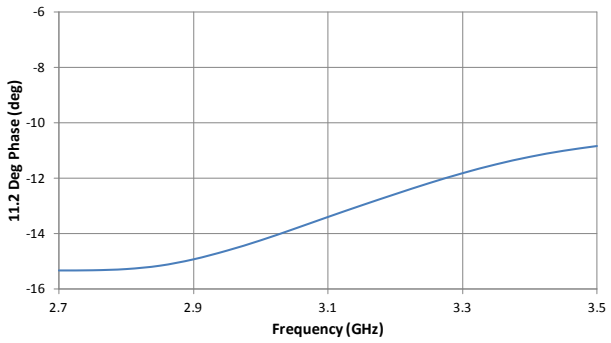


Phase 5.6 deg Bit

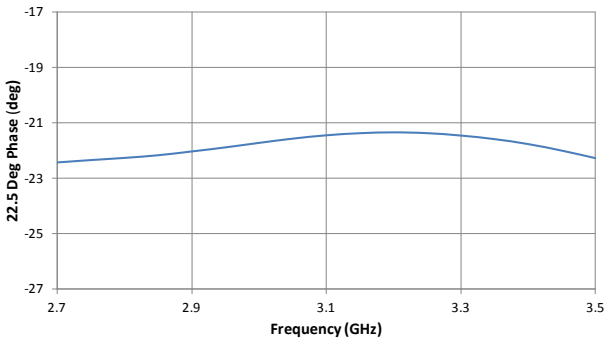


Typical Performance Curves

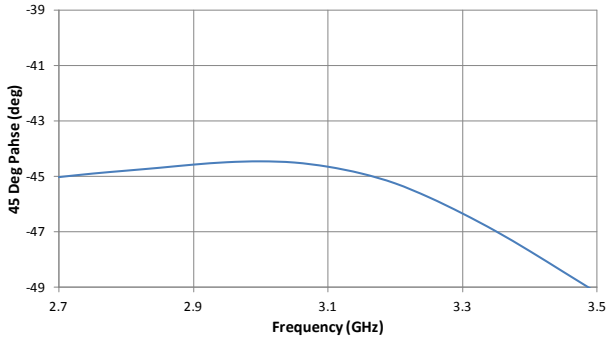
Phase 11.2 deg Bit



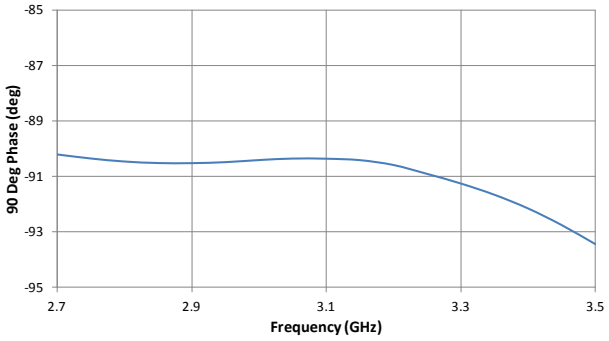
Phase 22.5 deg Bit



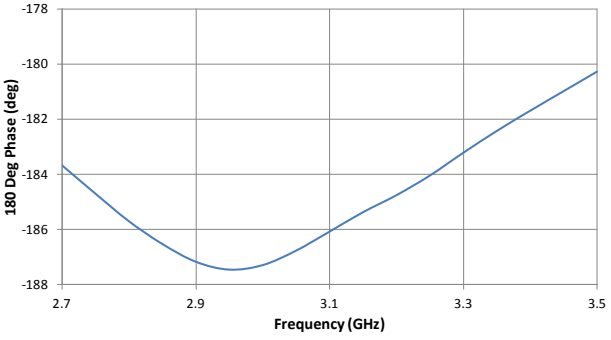
Phase 45 deg Bit



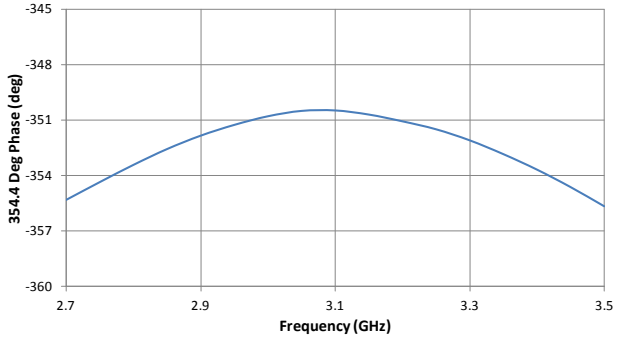
Phase 90 deg Bit



Phase 180 deg Bit

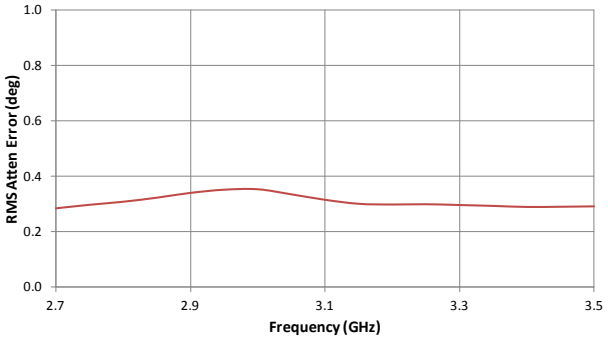


Phase @ Max. Phase (354.4° Nominal)

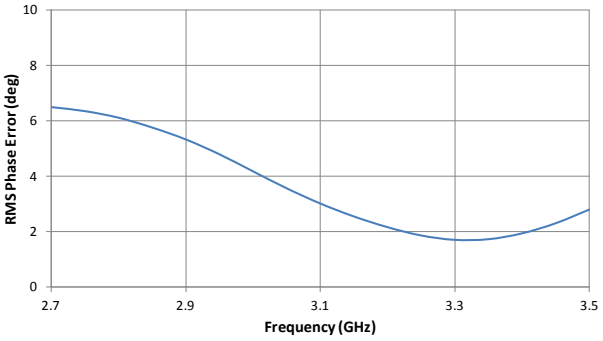


Typical Performance Curves

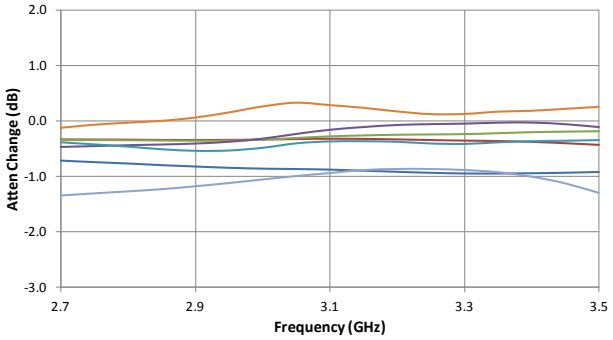
RMS Attenuation Error
All Attenuation States (1 dB through 15 dB)



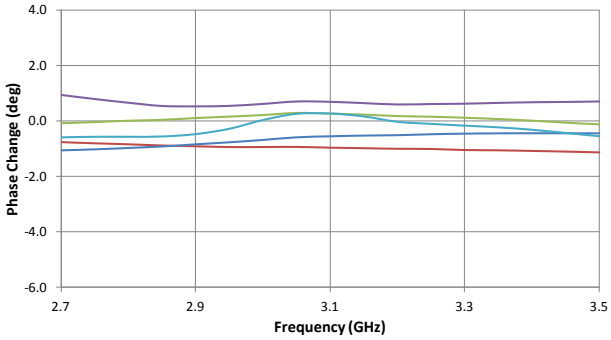
RMS Phase Error
All Phase States (-5.6° through –354.4°)



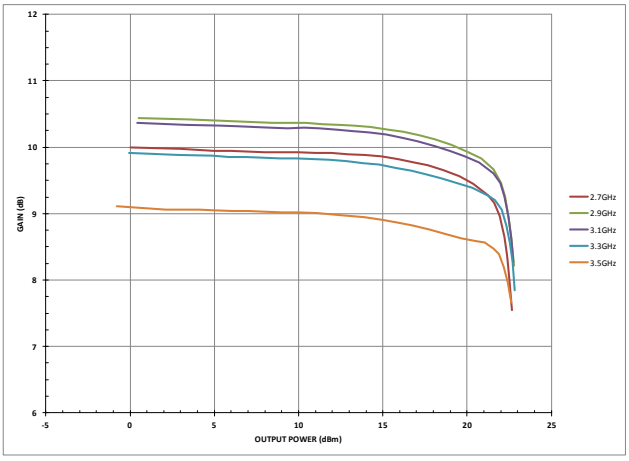
Attenuation Change vs. Phase State; (Reference Attenuation State) (Individual and Sum of Bits)



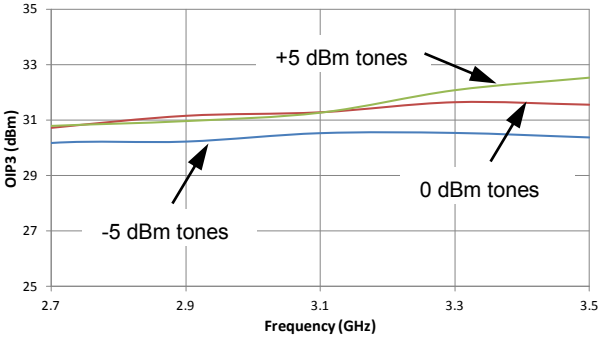
Phase Change vs. Attenuation State; Reference Phase State) (Individual and Sum of Bits)



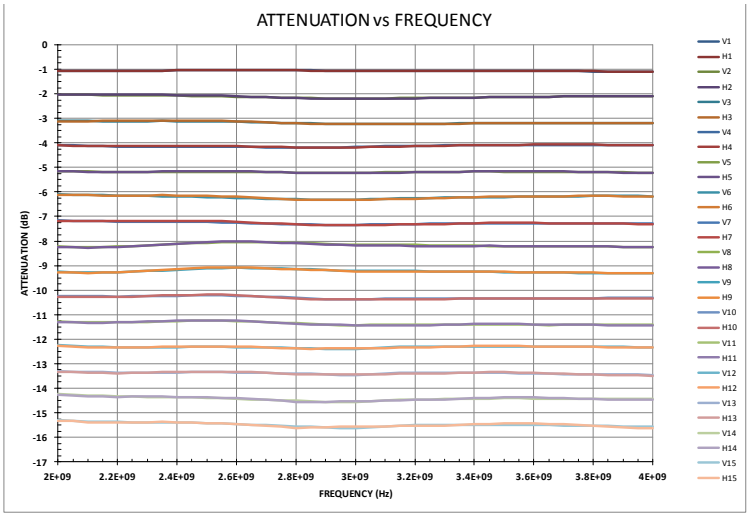
Output P1dB



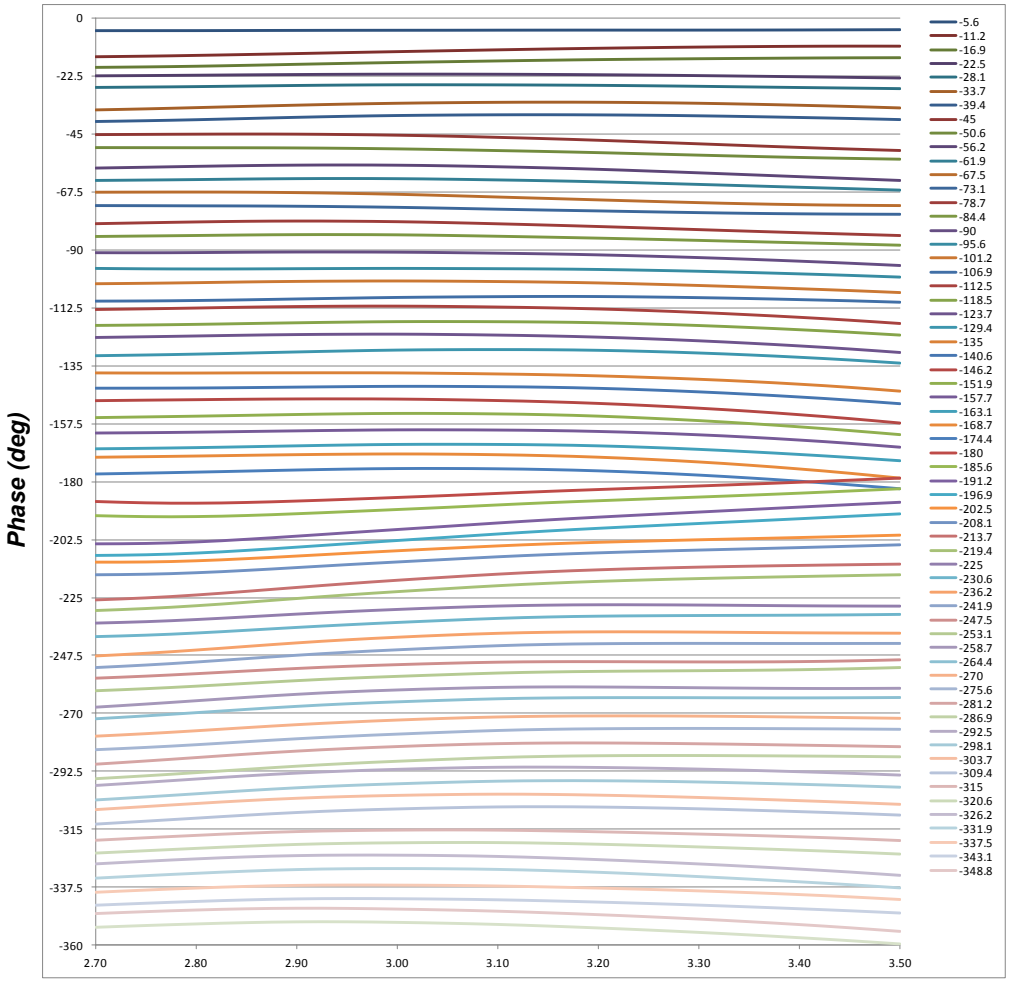
Output IP3



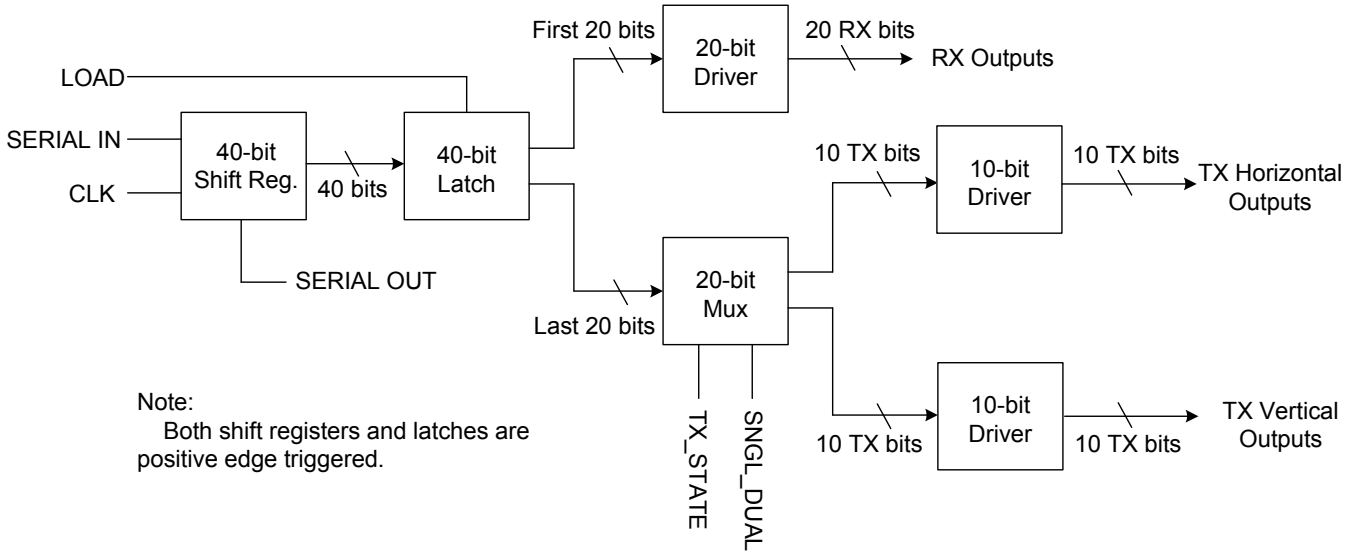
All Attenuation States at 0° Phase Shift



All Phase States at 0 dB Attenuation



Functional Diagram of Companion MADR-011007 Driver



Note:
Both shift registers and latches are positive edge triggered.

Serial Bit Stream Definition[7,8]

Bit No.	Bit Function	Bit No.	Bit Function
1	RX2-phase 1	21	TX-phase 1-A
2	RX2-phase 2	22	TX-phase 1-B
3	RX2-phase 3	23	TX-phase 2-A
4	RX2-phase 4	24	TX-phase 2-B
5	RX2-phase 5	25	TX-phase 3-A
6	RX2-phase 6	26	TX-phase 3-B
7	RX2-atten 1	27	TX-phase 4-A
8	RX2-atten 2	28	TX-phase 4-B
9	RX2-atten 3	29	TX-phase 5-A
10	RX2-atten 4	30	TX-phase 5-B
11	RX1-phase 1	31	TX-phase 6-A
12	RX1-phase 2	32	TX-phase 6-B
13	RX1-phase 3	33	TX-atten 1-A
14	RX1-phase 4	34	TX-atten 1-B
15	RX1-phase 5	35	TX-atten 2-A
16	RX1-phase 6	36	TX-atten 2-B
17	RX1-atten 1	37	TX-atten 3-A
18	RX1-atten 2	38	TX-atten 3-B
19	RX1-atten 3	39	TX-atten 4-A
20	RX1-atten 4	40	TX-atten 4-B

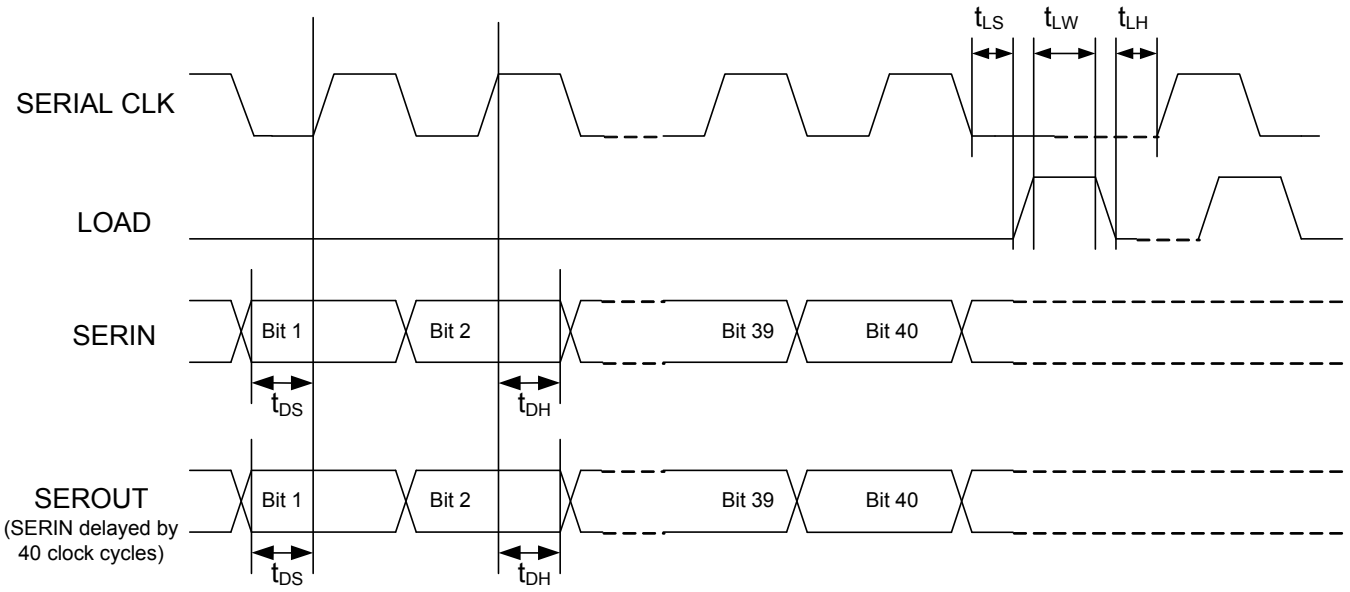
TX Multiplexer Truth Table

Vertical Beam Bits		SNGL_DUAL	
		L	H
TX_STATE	L[9]	A[10]	B[10]
	H[9]	A	A

Horizontal Beam Bits		SNGL_DUAL	
		L	H
TX_STATE	L	B	A
	H	B	B

7. Bit No.1 should be the first bit going into the serial interface.
8. Only bits 1-20 are used for the receive module. All 40 bits need to be provided for the driver to control the receive module. Bits 21-40 are “X” (don’t care), but must be high or low.
9. For V_{EE} = -5 V, Logic “L” = -5 V, and Logic “H” = 0 V.
10. “A” represents odd bits of the 20-bit TX bit stream, and “B” represents even bits of the 20-bit TX bit stream.

Serial Interface Timing Diagram



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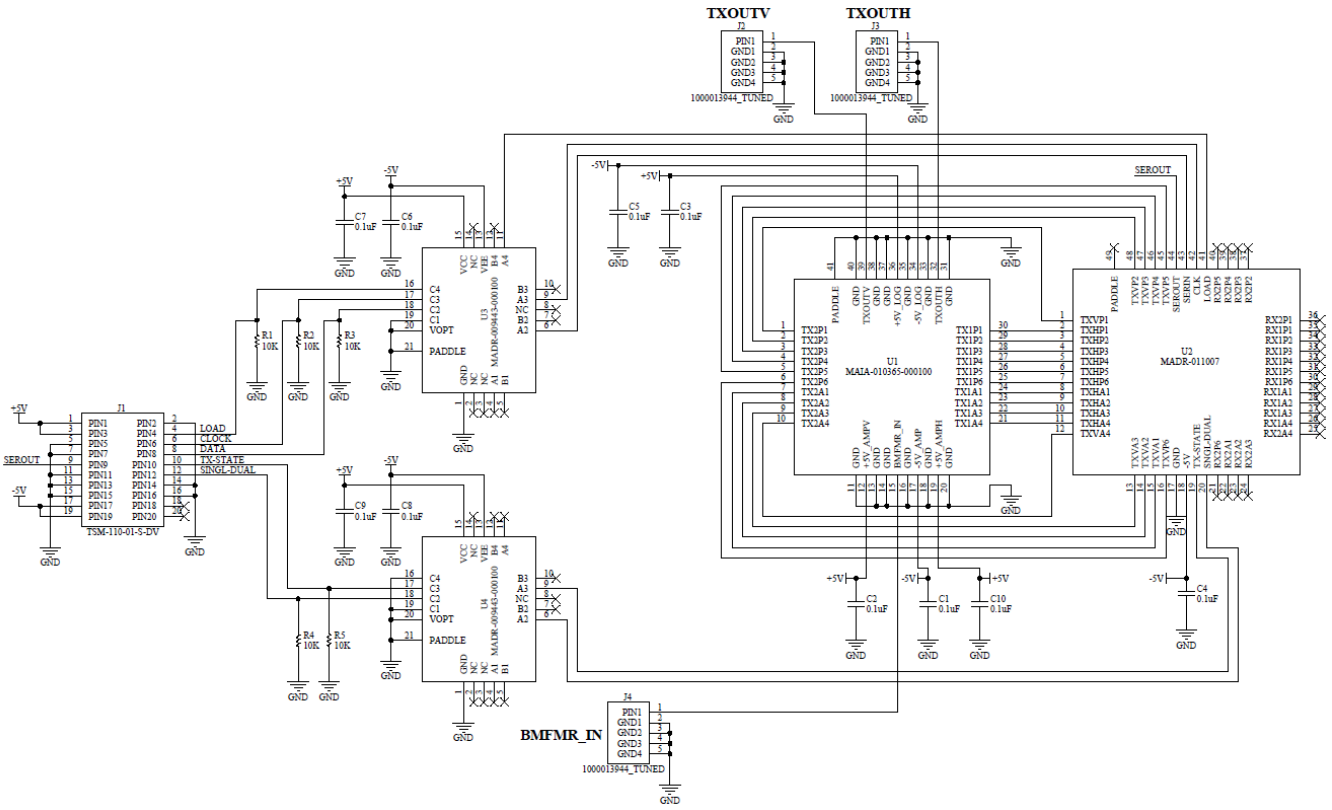
Sample Board Schematic with Off-Chip Components



Sample Board Pin BOM

Qty	Name	Mfg.	Description	Ref Des
1	MAIA-010365-000100	M/A-COM Tech	TX IC,PD,Preamp,Phase/Amp Control	U1
5			Resistor,0402,1%,1/16W,10K Ohms,SMT	R1-R5
10			Capacitor,0402,16V,X7R,10%,0.1uF,SMT	C1-C10
2	MADR-009443-000100	M/A-COM Tech	Quad FET and PIN driver, 4x4 mm PQFN	U3,U4
1	MADR-011007-000100	M/A-COM Tech	Driver, MPAR Digital Control	U2

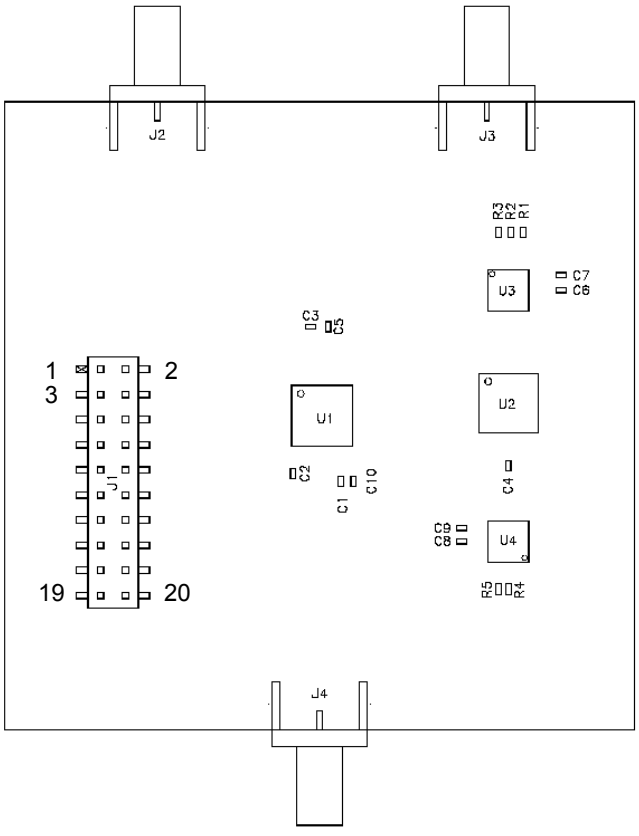
Sample Board Pin Configuration

Pin Configuration J1

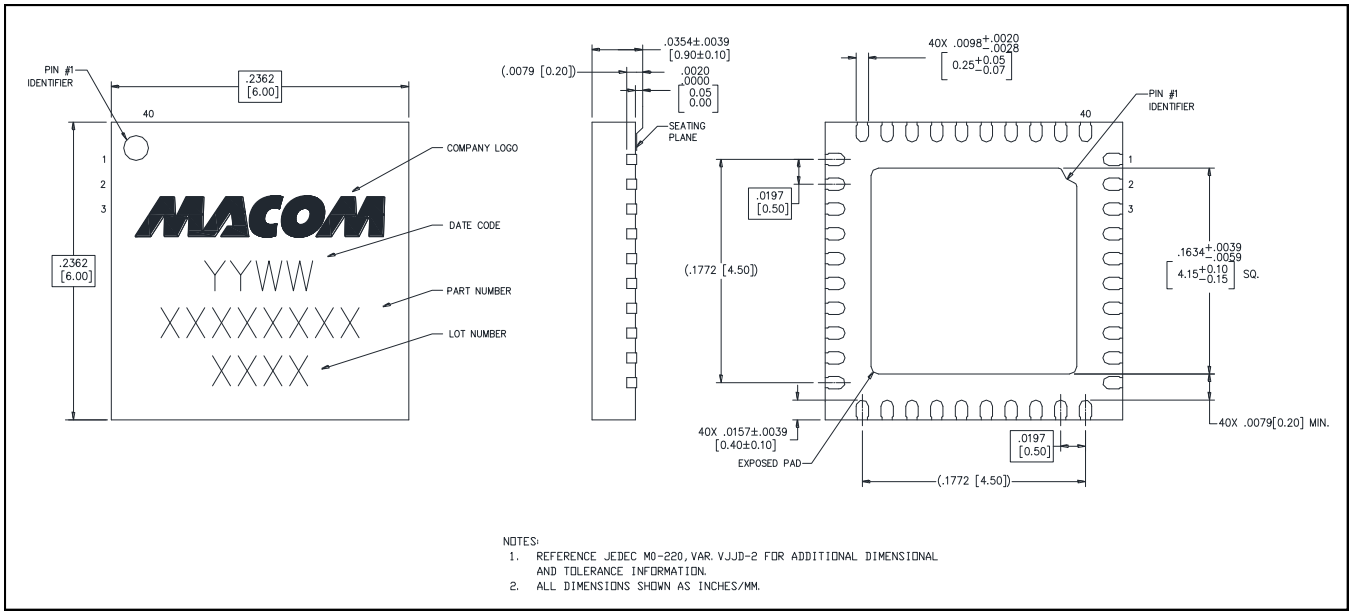
Pin No.	Function	Pin No.	Function
1	+5 V	11	GND
2	GND	12	SINGLE-DUAL
3	+5 V	13	GND
4	LOAD	14	GND
5	GND	15	GND
6	CLOCK	16	GND
7	GND	17	-5 V
8	SERIN	18	NC
9	SEROUT	19	-5 V
10	TX-STATE	20	NC

RF Pin Configuration

Connector Ref Des	Port Name
J2	TXOUTV
J3	TXOUTH
J4	BMFMR_IN



Lead-Free 6 mm, 40-Lead PQFN†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is NiPdAuAg.

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