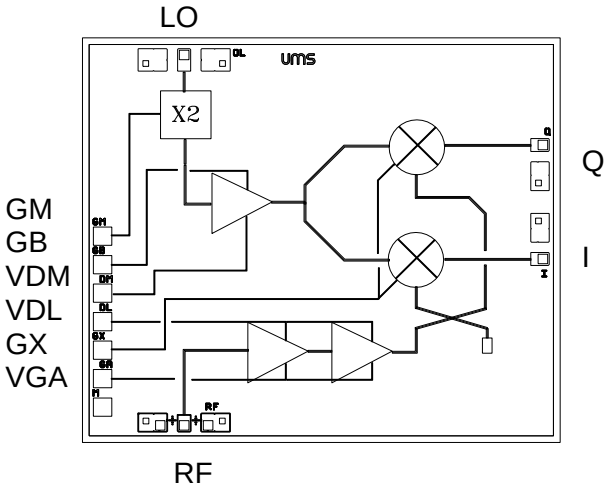
12-17GHz Integrated Down Converter

GaAs Monolithic Microwave IC

Description

The CHR2291 is a multifunction chip which integrates a LO time two multiplier, a balanced cold FET mixer, and a RF LNA. It is designed for a wide range of applications, typically commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

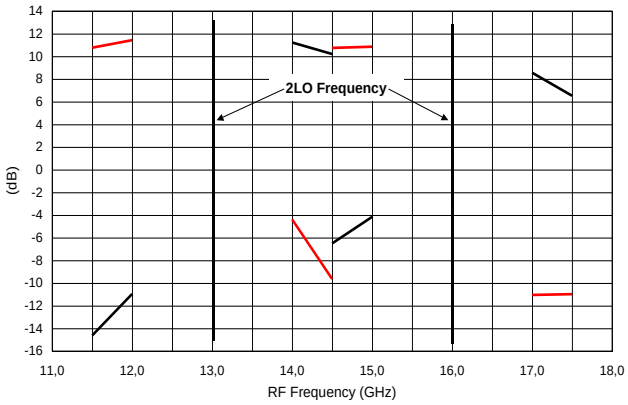
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Typical on wafer measurement:
Conversion Gain & Image suppression @ IF=1& 1.5GHz

Main Features

- Broadband performances : 12-17GHz
- 10 dB conversion gain
- 3.5dB noise figure
- 10dBm LO input power
- -8dBm RF input power (1dB gain comp.)
- Low DC power consumption, 130mA@3.5V
- Chip size : 2.49 X 2.13 X 0.10 mm



Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	12		17	GHz
F_{LO}	LO frequency range	5.25		7.75	GHz
F_{IF}	IF frequency range	DC		1.5	GHz
G_c	Conversion gain		+10		dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd = 3.5V ,Idl=50mA, Idm=50mA

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	12		17	GHz
F_{LO}	LO frequency range	5.25		7.75	GHz
F_{IF}	IF frequency range	DC		1.5	GHz
G_c	Conversion gain (1)		+10		dB
NF	Noise Figure (1)		3.5		dB
P_{LO}	LO Input power		+10		dBm
Img Sup	Image Suppression		15		dBc
P1dB	Input power at 1dB gain compression		-8		dBm
LO VSWR	Input LO VSWR (1)		2.0:1		
RF VSWR	Input RF VSWR (1)		2.0:1		
Id	Bias current (2)		100		mA

(1) On Wafer measurements
(2) Current source biasing network is recommended. Optimum performances for Idm= 50mA and Idl= 50mA

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage	4.0	V
Id	Maximum drain bias current	180	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Vdg	Maximum drain to gate voltage (Vd– Vg)	+5	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Tch	Maximum channel temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

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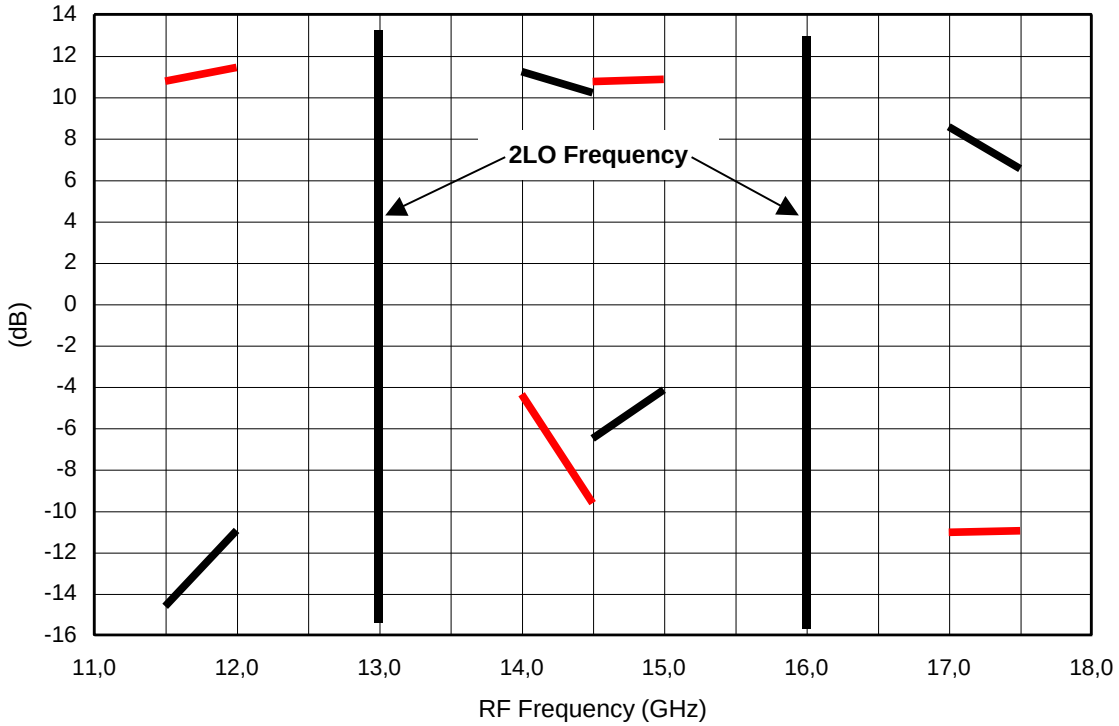
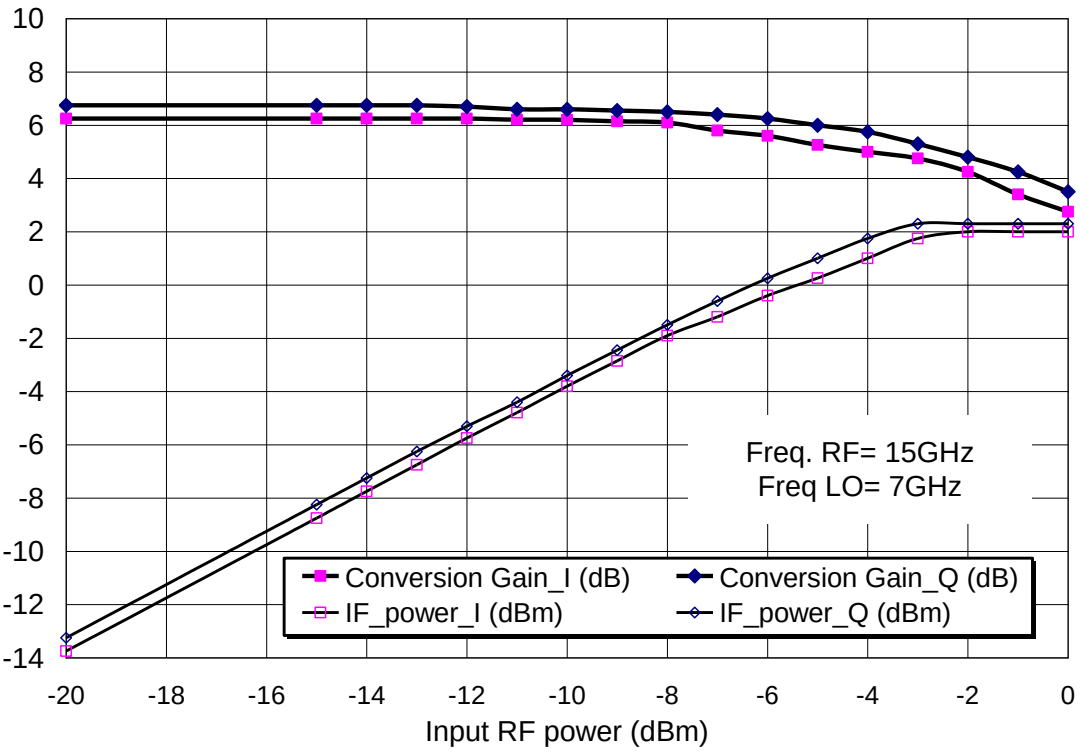
Typical On-wafer Measurements

Bias Conditions: Vdm= Vdl= 3.5 V, Vgm= -0.7V, Vgb= -0.4V, Vgx= -0.6V, Vga= -0.4V



Conversion gain & Image suppression with a 90° IQ combiner @ IF=1 & 1.5GHz



Input RF compression by channel

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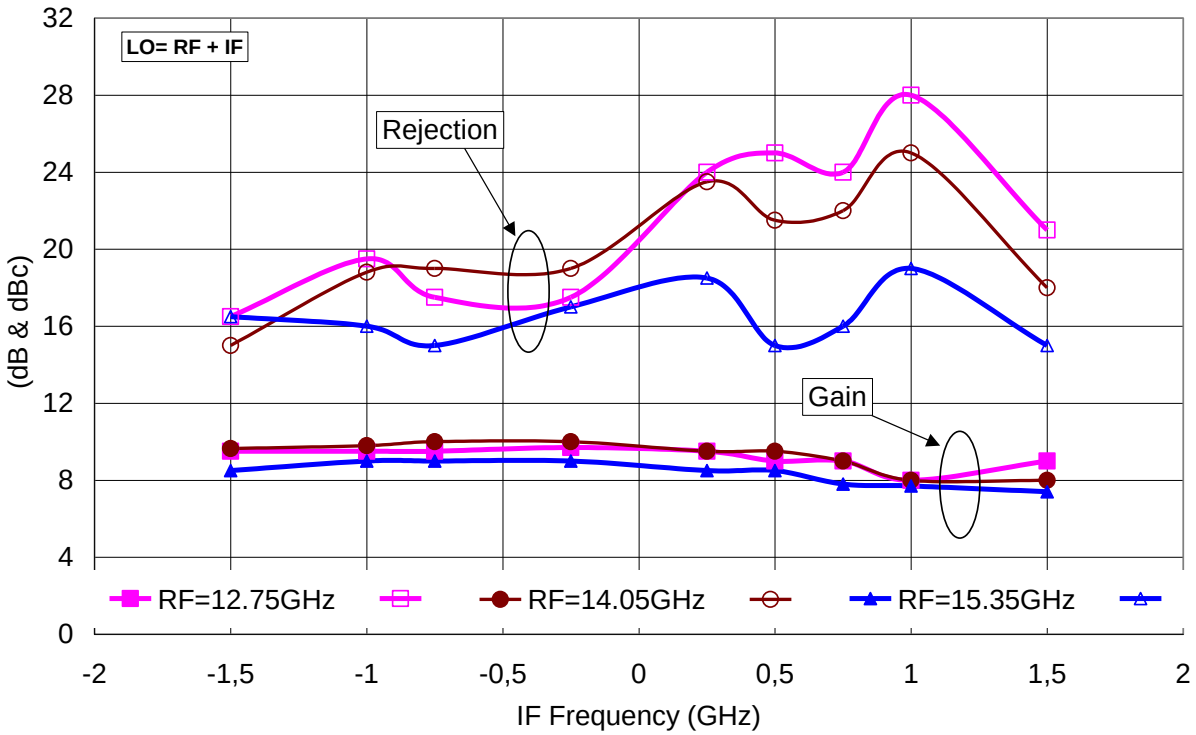
Typical On-board Measurements

Bias Conditions: Vdm= Vdl= 3.5 V, Vgm= -0.7V, Vgb= -0.4V, Vgx= -0.6V, Vga= -0.4V



Conversion Gain & Image Rejection with a 90° IQ combiner

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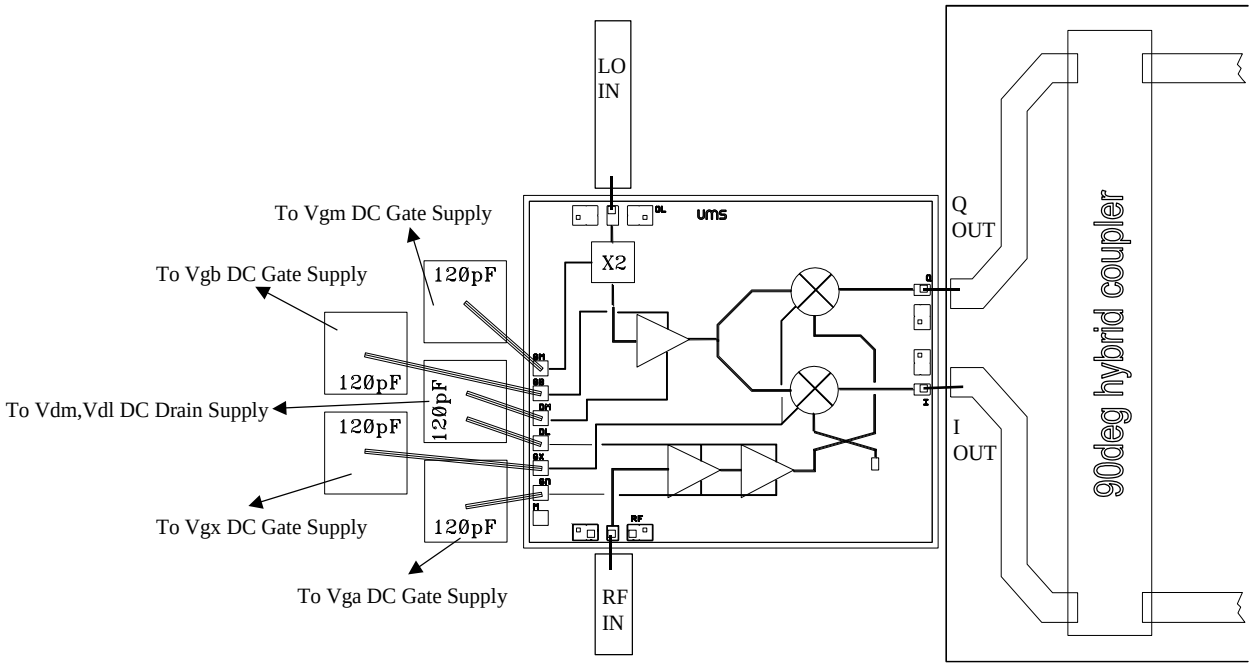
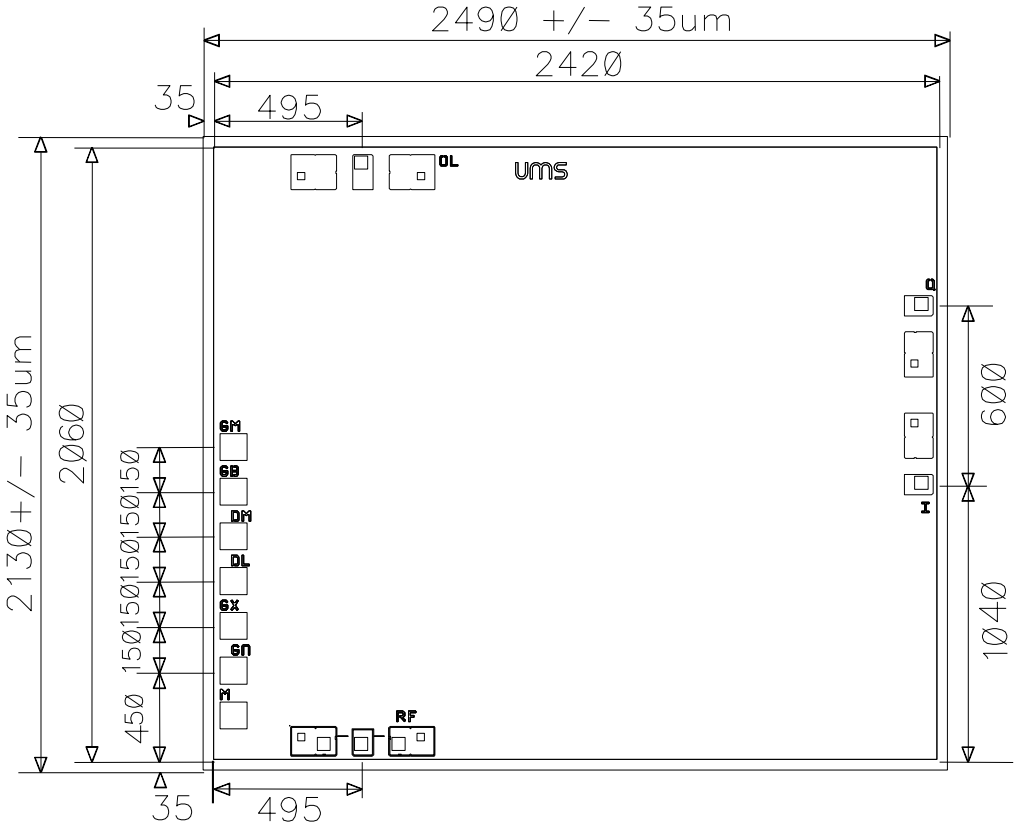
Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended



Bonding pad positions

(Chip thickness : 100µm. All dimensions are in micrometers)

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Ordering Information

Chip form : CHR2291-99F/00

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