36-40GHz Integrated Down Converter

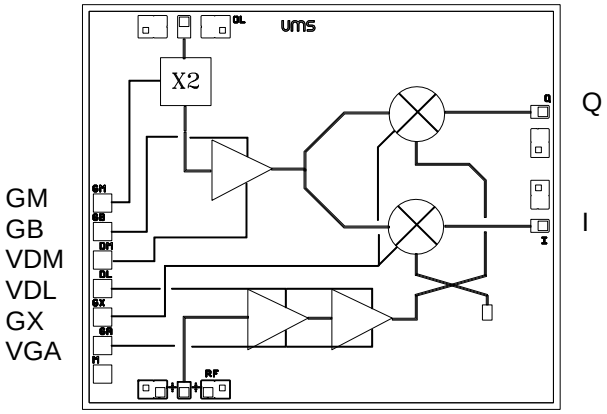
GaAs Monolithic Microwave IC

Description

The CHR2296 is a multifunction chip which integrates a LO time two multiplier, a balanced cold FET mixer, and a RF LNA. It is designed for a wide range of applications, typically commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.

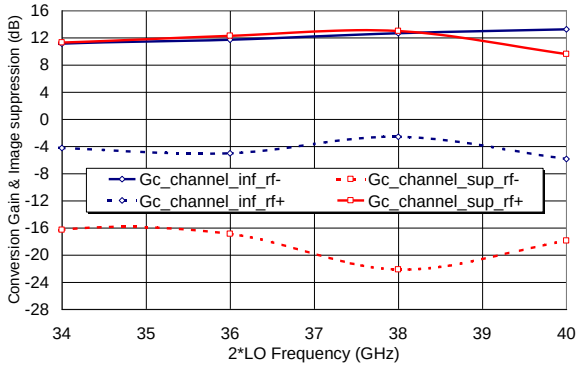
LO



Main Features

- Broadband performances: 36-40GHz
- 11 dB conversion gain
- 5dB noise figure
- 10dBm LO input power
- -10dBm RF input power (1dB gain comp.)
- Low DC power consumption, 110mA@3.5V
- Chip size: 2.49 X 1.97 X 0.10mm

Typical on wafer measurement:
Conversion Gain & Image suppression
@ IF=1GHz



Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	36		40	GHz
F_{LO}	LO frequency range	17		20	GHz
F_{IF}	IF frequency range	DC		1.5	GHz
G_c	Conversion gain	9	11		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	36		40	GHz
F_{LO}	LO frequency range	17		20	GHz
F_{IF}	IF frequency range	DC		1.5	GHz
G_c	Conversion gain (1)	9	11		dB
NF	Noise Figure (1)		5		dB
P_{LO}	LO Input power		+10		dBm
Img Sup	Image Suppression	13	15		dBc
P1dB	Input power at 1dB gain compression		-10		dBm
LO VSWR	Input LO VSWR (1)		2.0:1		
RF VSWR	Input RF VSWR (1)		3.0:1		
Id	Bias current (2)		110		mA

(1) On Wafer measurements
(2) Current source biasing network is recommended. Optimum performances for Idm = 50mA and Idl = 60mA

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage	4.0	V
Id	Maximum drain bias current	200	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Vgd	Minimum negative gate drain voltage (Vg – Vd)	-5	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Tch	Maximum channel temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

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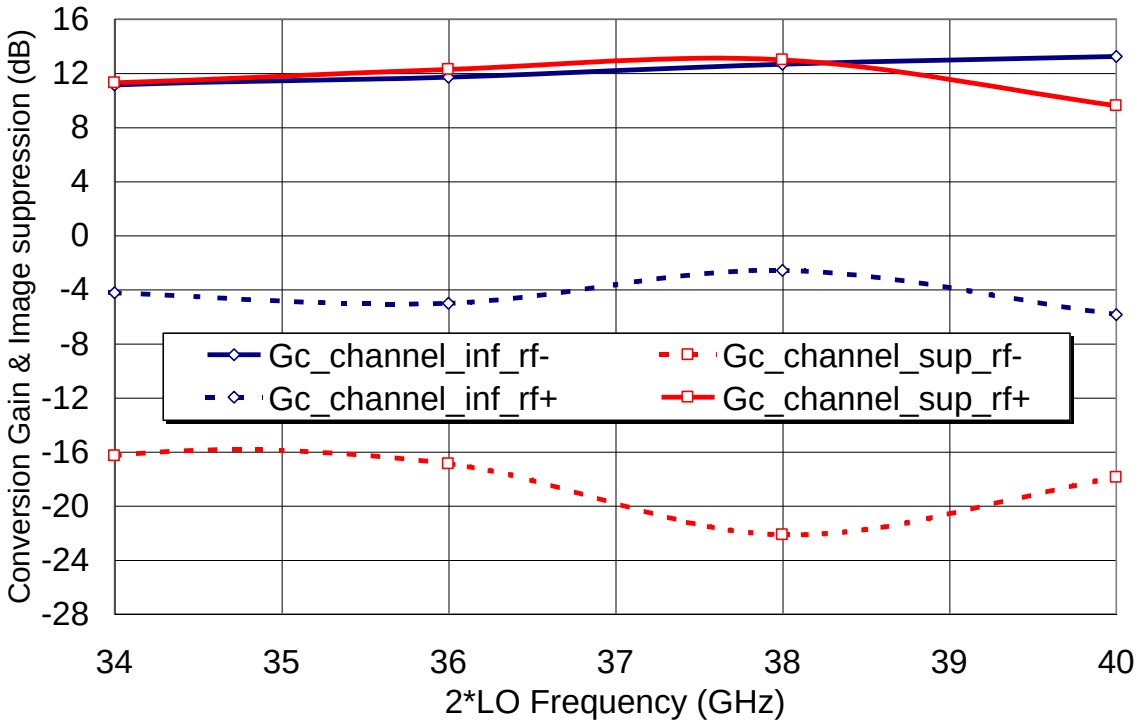
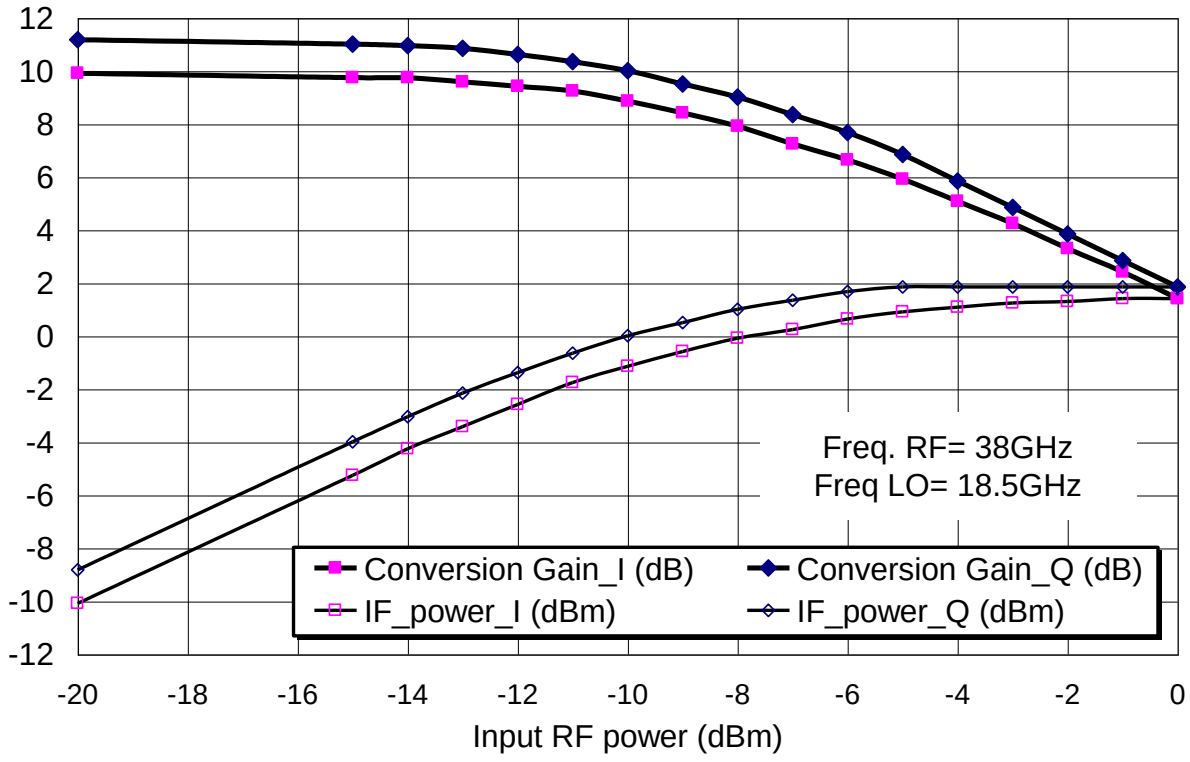
Typical On-wafer Measurements

Bias Conditions : Vdm= Vdl= 3.5 V, Vgm= -0.9V, Vgb= -0.4V, Vgx= -0.8V, Vga= -0.5V



Conversion gain & Image suppression with a 90° IQ combiner @ IF=1GHz



Input RF compression by channel

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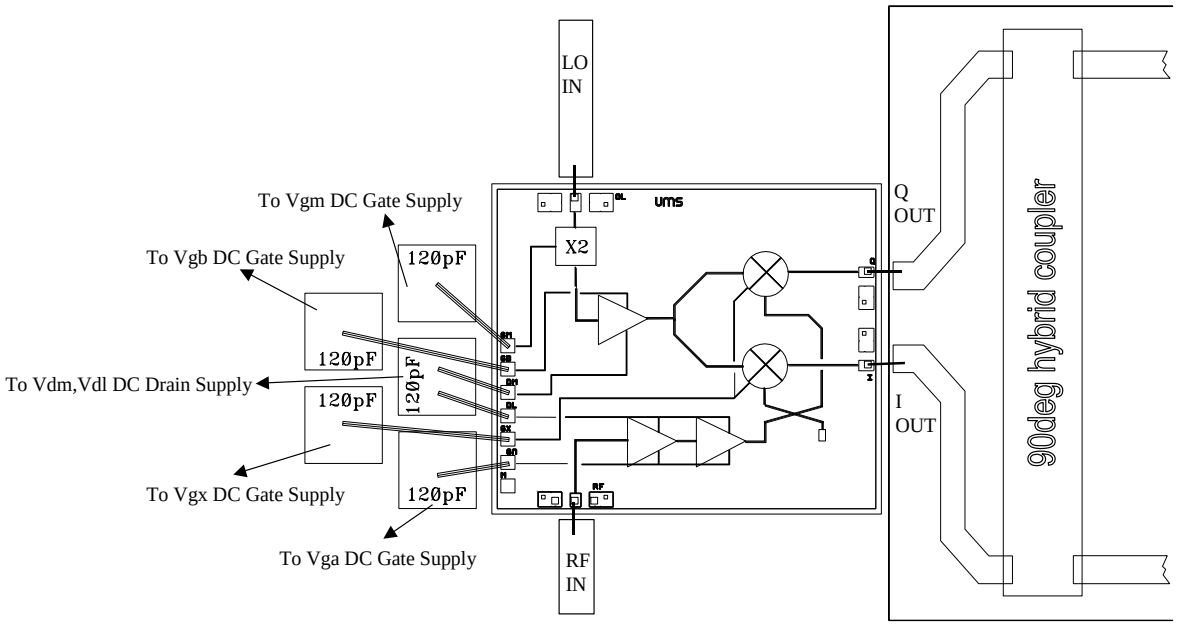
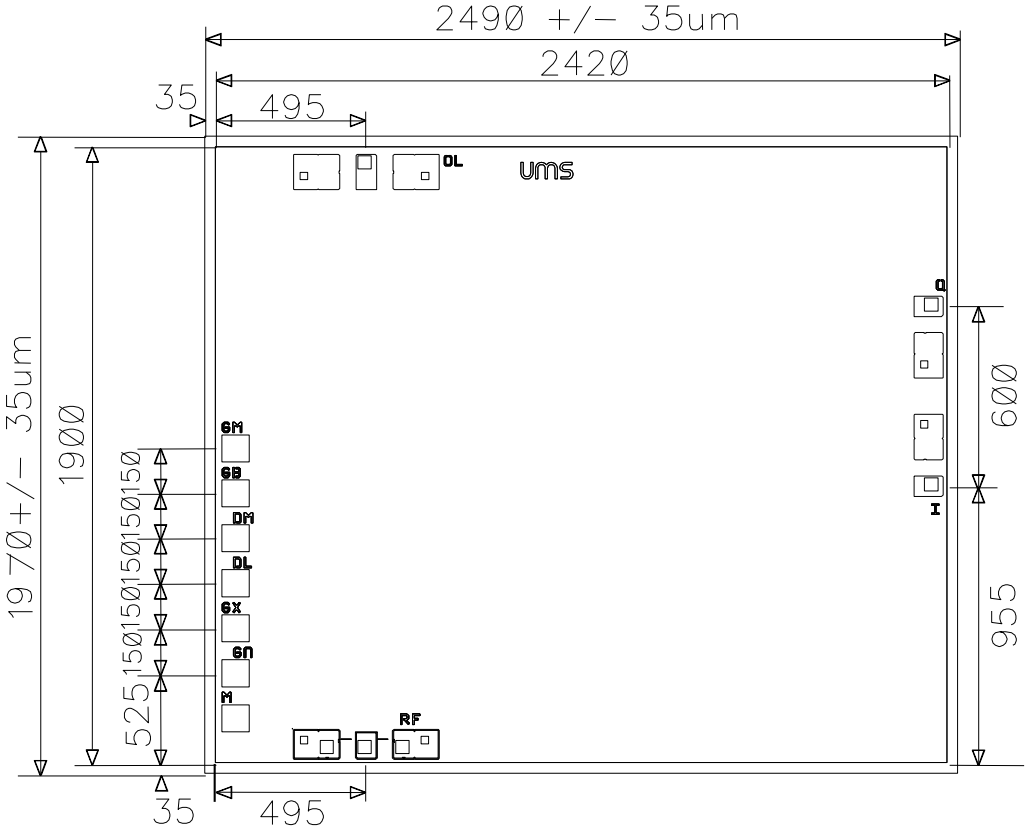
Chip Assembly and Mechanical Data



Note: Supply feed should be bypassed. 25µm diameter gold wire is recommended



Bonding pad positions
(Chip thickness: 100µm. All dimensions are in micrometers)

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Notes

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form: CHR2296-99F/00

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