

## 36-40GHz Integrated Down Converter

### GaAs Monolithic Microwave IC

#### Description

The CHR2296 is a multifunction chip which integrates a LO time two multiplier, a balanced cold FET mixer, and a RF LNA. It is designed for a wide range of applications, typically commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25 $\mu$ m gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.

#### Main Features

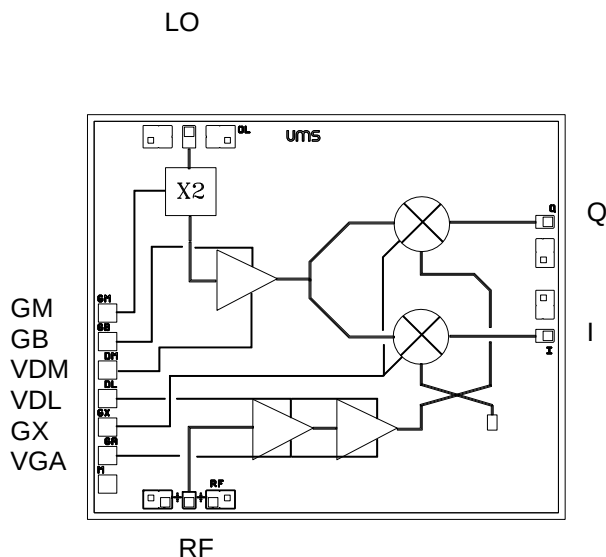
- Broadband performances: 36-40GHz
- 11 dB conversion gain
- 5dB noise figure
- 10dBm LO input power
- -10dBm RF input power (1dB gain comp.)
- Low DC power consumption, 110mA@3.5V
- Chip size: 2.49 X 1.97 X 0.10mm

#### Main Characteristics

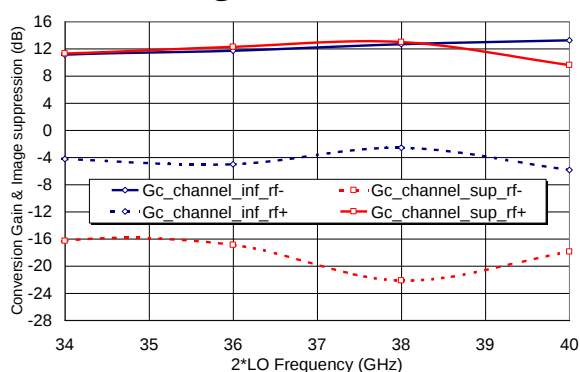
T<sub>amb.</sub> = 25°C

| Symbol          | Parameter          | Min | Typ | Max | Unit |
|-----------------|--------------------|-----|-----|-----|------|
| F <sub>RF</sub> | RF frequency range | 36  |     | 40  | GHz  |
| F <sub>LO</sub> | LO frequency range | 17  |     | 20  | GHz  |
| F <sub>IF</sub> | IF frequency range | DC  |     | 1.5 | GHz  |
| G <sub>c</sub>  | Conversion gain    | 9   | 11  |     | dB   |

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!



Typical on wafer measurement:  
Conversion Gain & Image suppression  
@ IF=1GHz



## Electrical Characteristics for Broadband Operation

T<sub>amb</sub> = +25°C, V<sub>d</sub> = 3.5V

| Symbol          | Parameter                           | Min | Typ   | Max | Unit |
|-----------------|-------------------------------------|-----|-------|-----|------|
| F <sub>RF</sub> | RF frequency range                  | 36  |       | 40  | GHz  |
| F <sub>LO</sub> | LO frequency range                  | 17  |       | 20  | GHz  |
| F <sub>IF</sub> | IF frequency range                  | DC  |       | 1.5 | GHz  |
| G <sub>c</sub>  | Conversion gain <sup>(1)</sup>      | 9   | 11    |     | dB   |
| NF              | Noise Figure <sup>(1)</sup>         |     | 5     |     | dB   |
| P <sub>LO</sub> | LO Input power                      |     | +10   |     | dBm  |
| Img Sup         | Image Suppression                   | 13  | 15    |     | dBc  |
| P1dB            | Input power at 1dB gain compression |     | -10   |     | dBm  |
| LO VSWR         | Input LO VSWR <sup>(1)</sup>        |     | 2.0:1 |     |      |
| RF VSWR         | Input RF VSWR <sup>(1)</sup>        |     | 3.0:1 |     |      |
| I <sub>d</sub>  | Bias current <sup>(2)</sup>         |     | 110   |     | mA   |

(1) On Wafer measurements

(2) Current source biasing network is recommended. Optimum performances for I<sub>dm</sub> = 50mA and I<sub>dl</sub> = 60mA

## Absolute Maximum Ratings

T<sub>amb.</sub> = 25°C (1)

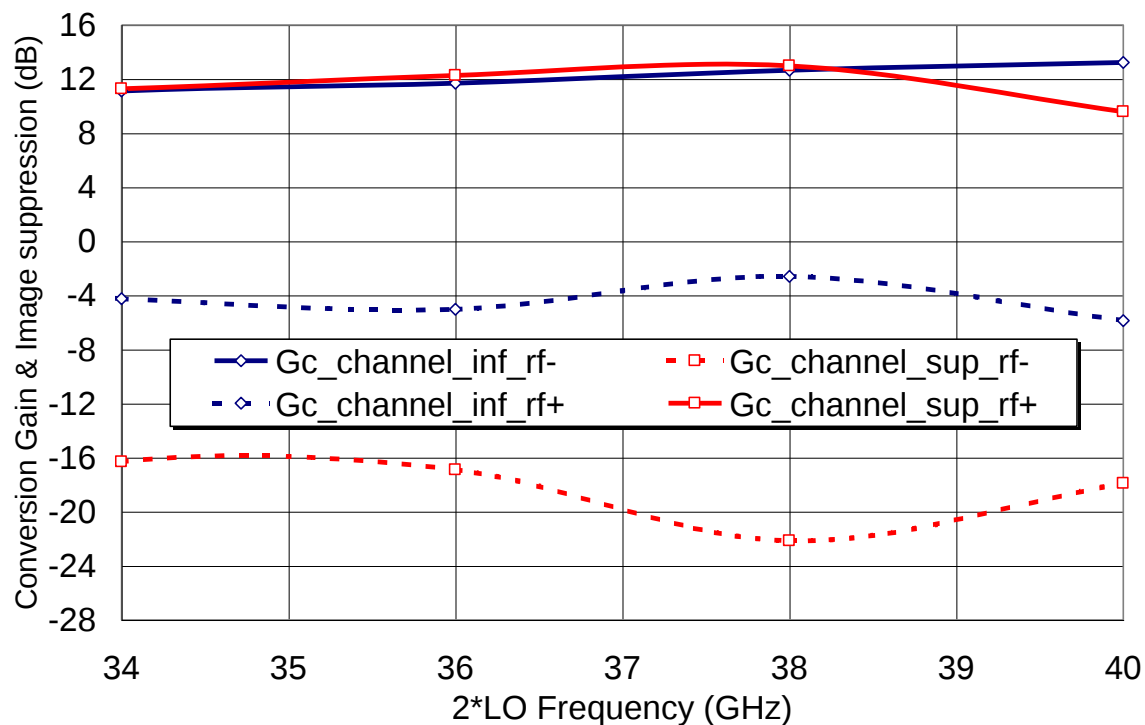
| Symbol           | Parameter                                                               | Values       | Unit |
|------------------|-------------------------------------------------------------------------|--------------|------|
| V <sub>d</sub>   | Maximum drain bias voltage                                              | 4.0          | V    |
| I <sub>d</sub>   | Maximum drain bias current                                              | 200          | mA   |
| V <sub>g</sub>   | Gate bias voltage                                                       | -2.0 to +0.4 | V    |
| V <sub>gd</sub>  | Minimum negative gate drain voltage ( V <sub>g</sub> – V <sub>d</sub> ) | -5           | V    |
| P <sub>in</sub>  | Maximum peak input power overdrive (2)                                  | +15          | dBm  |
| T <sub>ch</sub>  | Maximum channel temperature                                             | 175          | °C   |
| T <sub>a</sub>   | Operating temperature range                                             | -40 to +85   | °C   |
| T <sub>stg</sub> | Storage temperature range                                               | -55 to +125  | °C   |

(1) Operation of this device above anyone of these parameters may cause permanent damage.

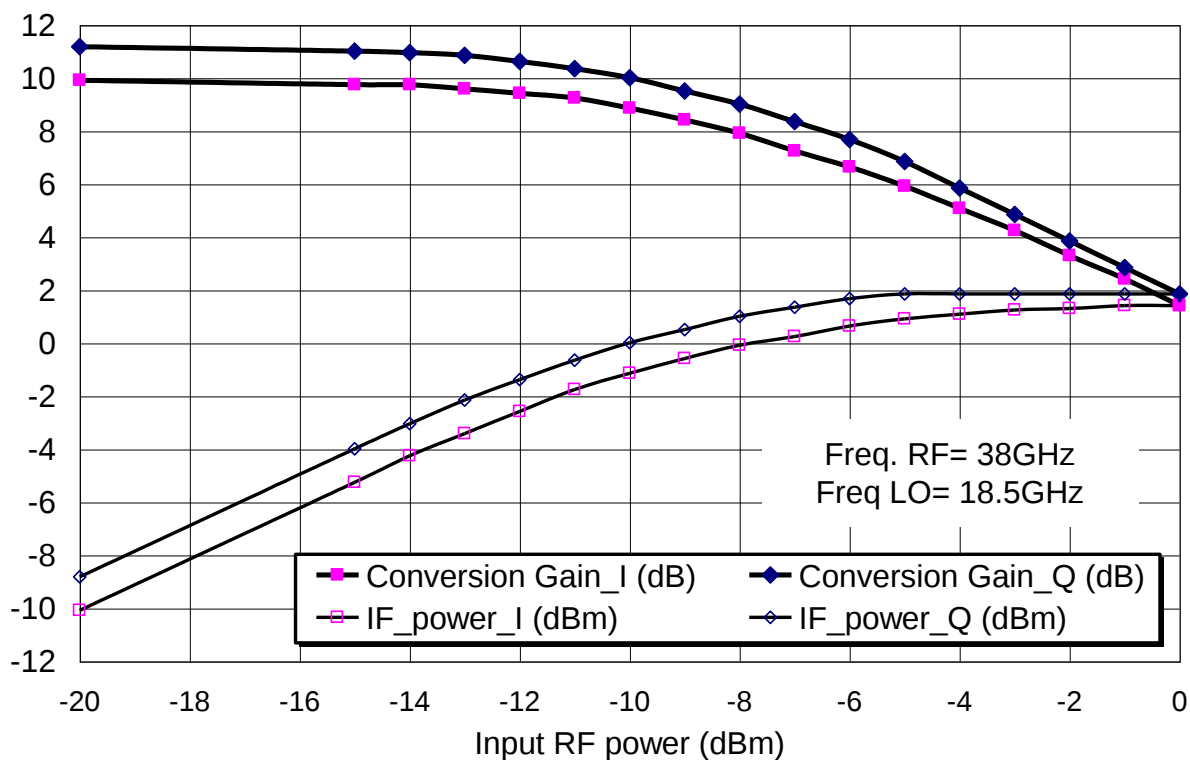
(2) Duration < 1s.

## Typical On-wafer Measurements

Bias Conditions :  $V_{dm} = V_{dl} = 3.5\text{ V}$ ,  $V_{gm} = -0.9\text{ V}$ ,  $V_{gb} = -0.4\text{ V}$ ,  $V_{gx} = -0.8\text{ V}$ ,  $V_{ga} = -0.5\text{ V}$



Conversion gain & Image suppression with a 90° IQ combiner @ IF=1GHz



Input RF compression by channel

LO IN

RF IN

ums

X2

120pF

120pF

120pF

120pF

120pF

120pF

To Vgm DC Gate Supply

To Vgb DC Gate Supply

To Vdm,Vdl DC Drain Supply

To Vgx DC Gate Supply

To Vga DC Gate Supply

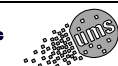
Q OUT

I OUT

90deg hybrid coupler

Top view of the PCB layout. Dimensions are given in millimeters (mm). The overall dimensions are 2490 ± 35 mm (width) and 1970 ± 35 mm (height). The layout includes a central rectangular area with a width of 2420 mm and a height of 1900 mm. The layout is divided into four quadrants by a horizontal and a vertical centerline. The components are labeled as follows: **OL** (Optical Lens) at the top center, **UMS** (Universal Machine System) at the top right, **GM** (General Machine) at the bottom left, **GB** (General Board) at the bottom center, **DFI** (Digital Filter Interface) at the bottom right, **DL** (Digital Lens) at the bottom left, **EX** (External) at the bottom center, **EN** (External Network) at the bottom right, **M** (Motor) at the bottom left, **RF** (Radio Frequency) at the bottom center, **I** (Input) at the top right, and **Q** (Output) at the top left. The layout also shows a series of small rectangular components along the bottom edge, labeled **GM**, **GB**, **DFI**, **DL**, **EX**, **EN**, and **M**. The layout is divided into four quadrants by a horizontal and a vertical centerline. The components are labeled as follows: **OL** (Optical Lens) at the top center, **UMS** (Universal Machine System) at the top right, **GM** (General Machine) at the bottom left, **GB** (General Board) at the bottom center, **DFI** (Digital Filter Interface) at the bottom right, **DL** (Digital Lens) at the bottom left, **EX** (External) at the bottom center, **EN** (External Network) at the bottom right, **M** (Motor) at the bottom left, **RF** (Radio Frequency) at the bottom center, **I** (Input) at the top right, and **Q** (Output) at the top left. The layout also shows a series of small rectangular components along the bottom edge, labeled **GM**, **GB**, **DFI**, **DL**, **EX**, **EN**, and **M**.

(Chip thickness: 100 $\mu$ m. All dimensions are in micrometers)



**Notes**

## Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

## Ordering Information

Chip form: CHR2296-99F/00

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