

36-44GHz Multifunction Down-Converter

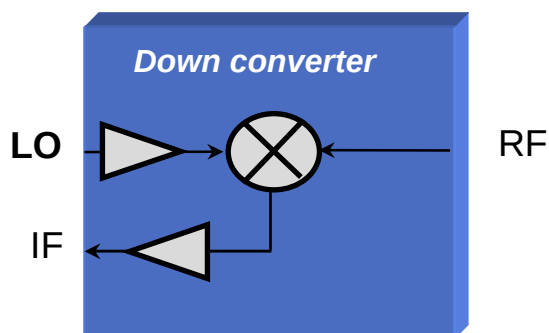
GaAs Monolithic Microwave IC

Description

The CHR2297 is a multifunction chip (MFC) which integrates a LO buffer amplifier, an IF amplifier and a single cold FET mixer. It is usable for down-conversion. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps to simplify the assembly process.

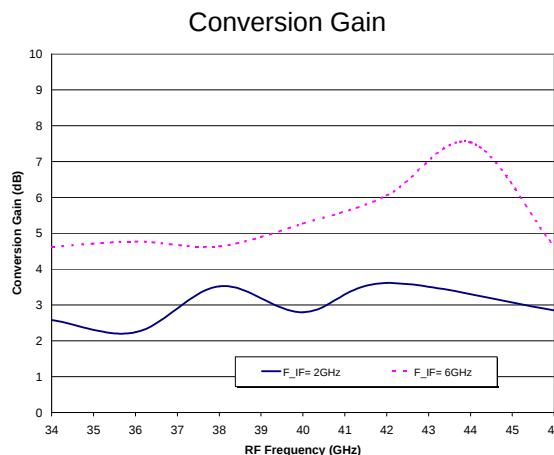
The circuit is manufactured with a pHEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- Broadband performance: 36-44GHz
- 2.5dB conversion gain
- 0dBm LO input power
- +4dBm input power (1dB gain comp.)
- DC power consumption, 65mA @ 4V
- Chip size: 1.33x1.68x0.10mm



Main Characteristics

T_{amb.} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	36		44	GHz
F _{LO}	LO frequency range	30		39	GHz
F _{IF}	IF frequency range	2		6	GHz
G _c	Conversion Gain		2.5		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Electrical Characteristics

Tamb=+25°C

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF frequency range	36		44	GHz
F _{LO}	LO frequency range	30		39	GHz
F _{IF}	IF frequency range	2		6	GHz
G _c	Conversion Gain		2.5		dB
P _{LO}	LO Input power		0		dBm
LO_IF Lk	LO Leakage on IF (for P _{LO} =0dBm)		-28		dBm
LO_RF Lk	LO Leakage on RF (for P _{LO} =0dBm)		-22		dBm
RF_IF Lk	RF Leakage on IF (for P _{RF} =-5dBm)		-50		dBm
P1dB	Input power at 1dB gain compression		+4		dBm
LO Match	LO Matching ⁽¹⁾		2.0:1		
RF Match	RF Matching ⁽¹⁾		2.0:1		
IF Match	IF Matching		2.0:1		
Vd	Drain bias voltage (pads Vd1, Vd2)		4		V
Vg	Gate bias voltage (pad Vg)		-1		V
Id	Drain bias current		65		mA

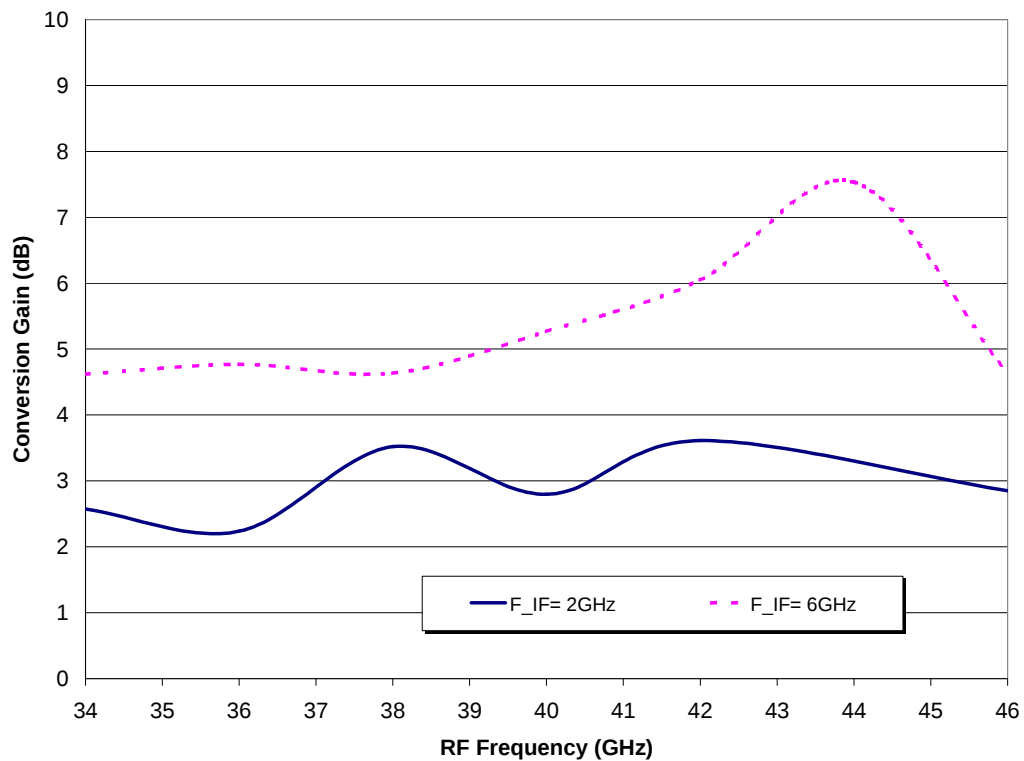
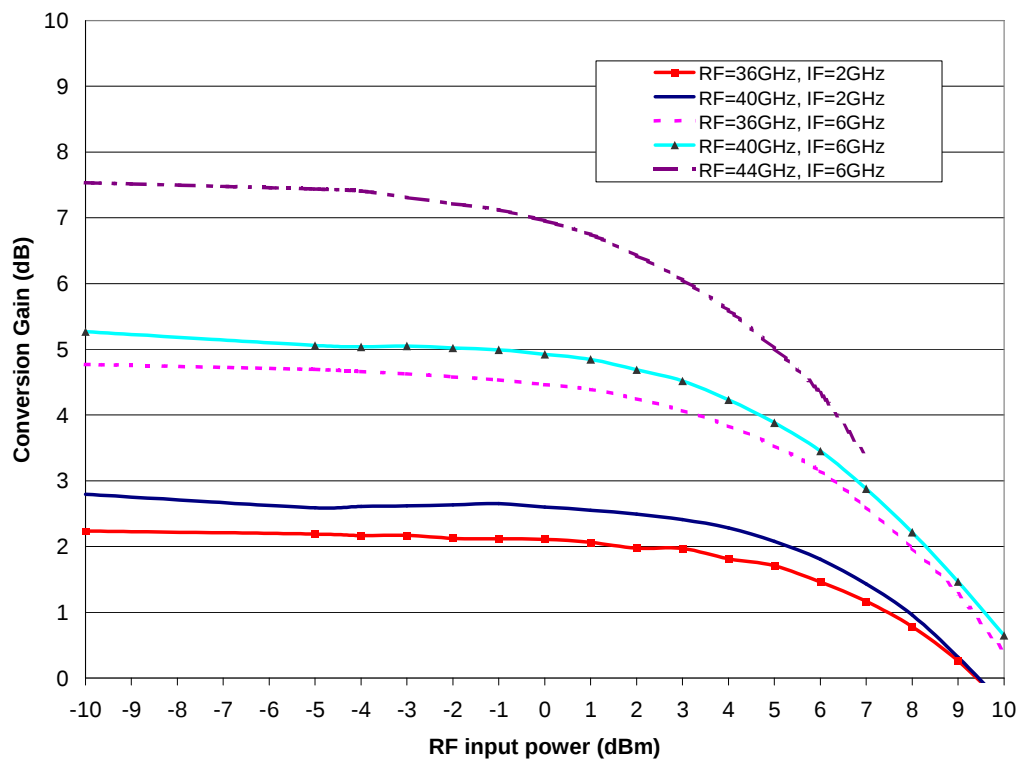
(1) A wire bond of typically 0.1 to 0.15 nH will improve the input and output matching.

Absolute Maximum Ratings ⁽¹⁾

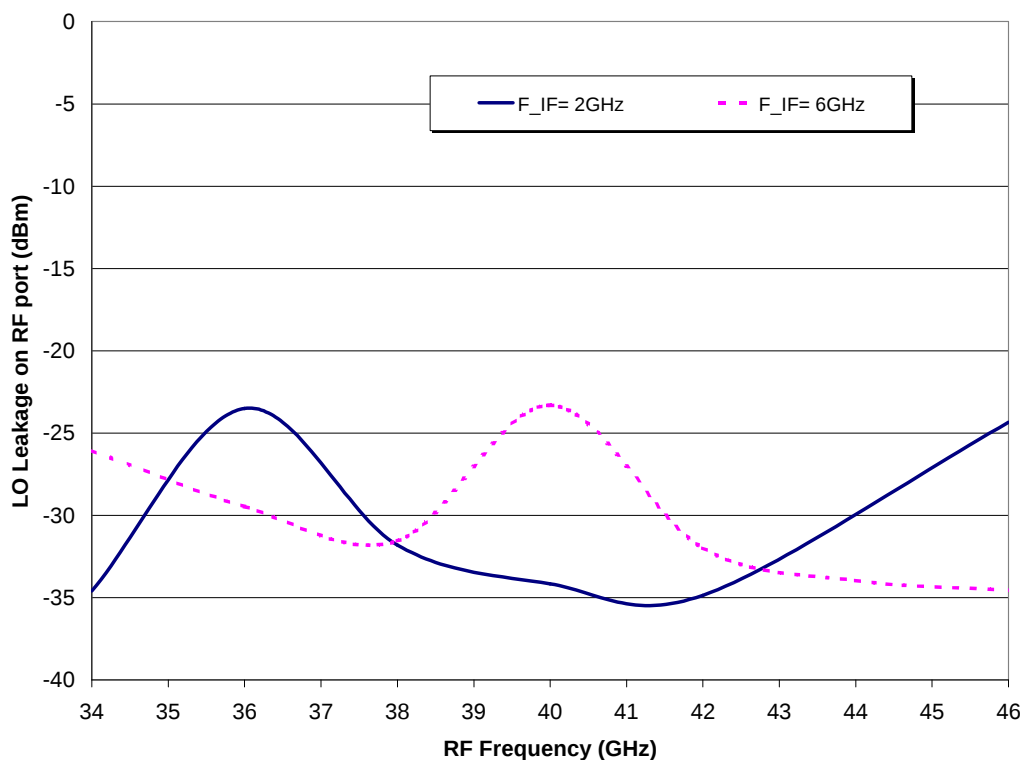
Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Id	Drain bias current	100	mA
P _{LO}	Maximum LO input power	5	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

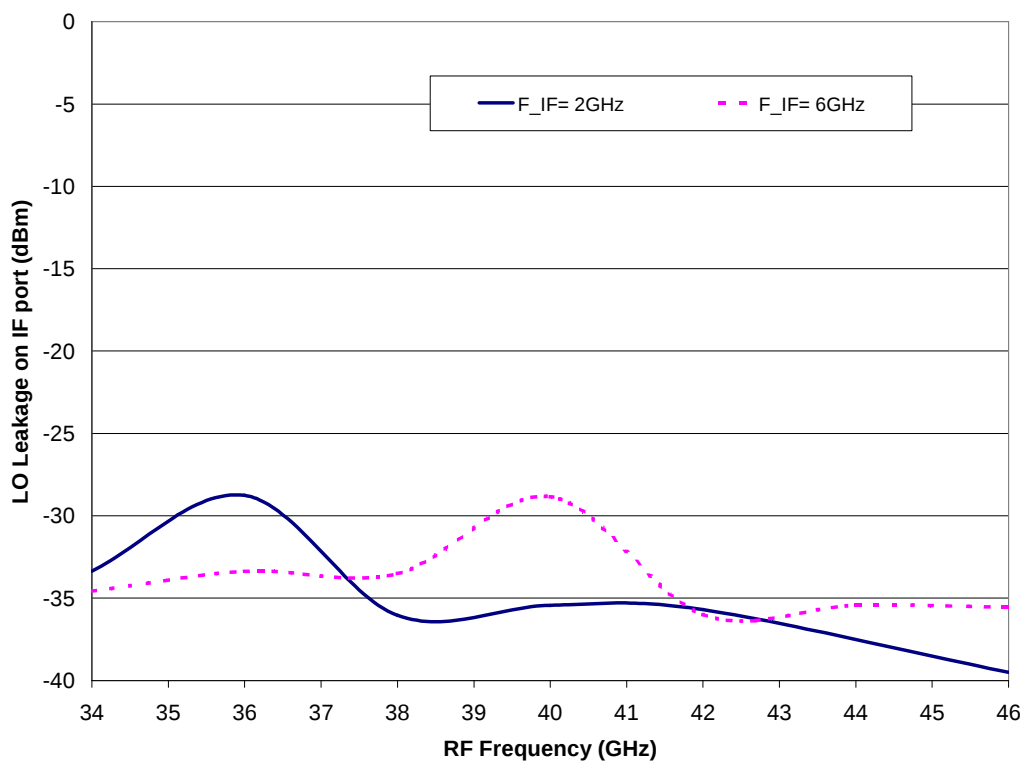
(1) Operation of device above any one of these parameters may cause permanent damage.

Typical on wafer measurementT_{amb}: 25°C, V_d=4V, V_g= -1V, P_{LO}= 0dBm**Conversion gain versus RF frequency****Conversion gain versus RF input power**

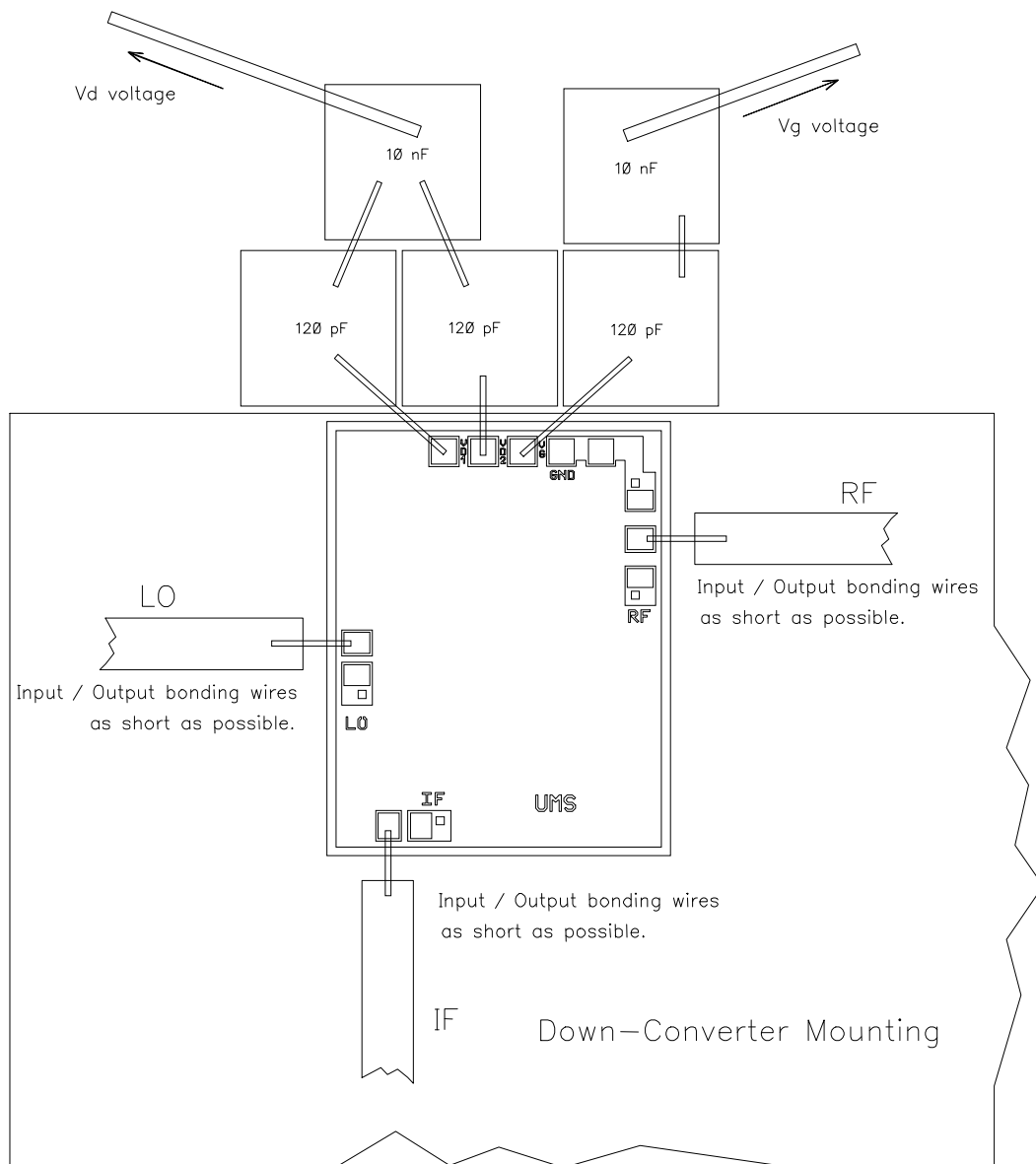
LO Leakage on RF port



LO Leakage on IF port



Recommended assembly plan

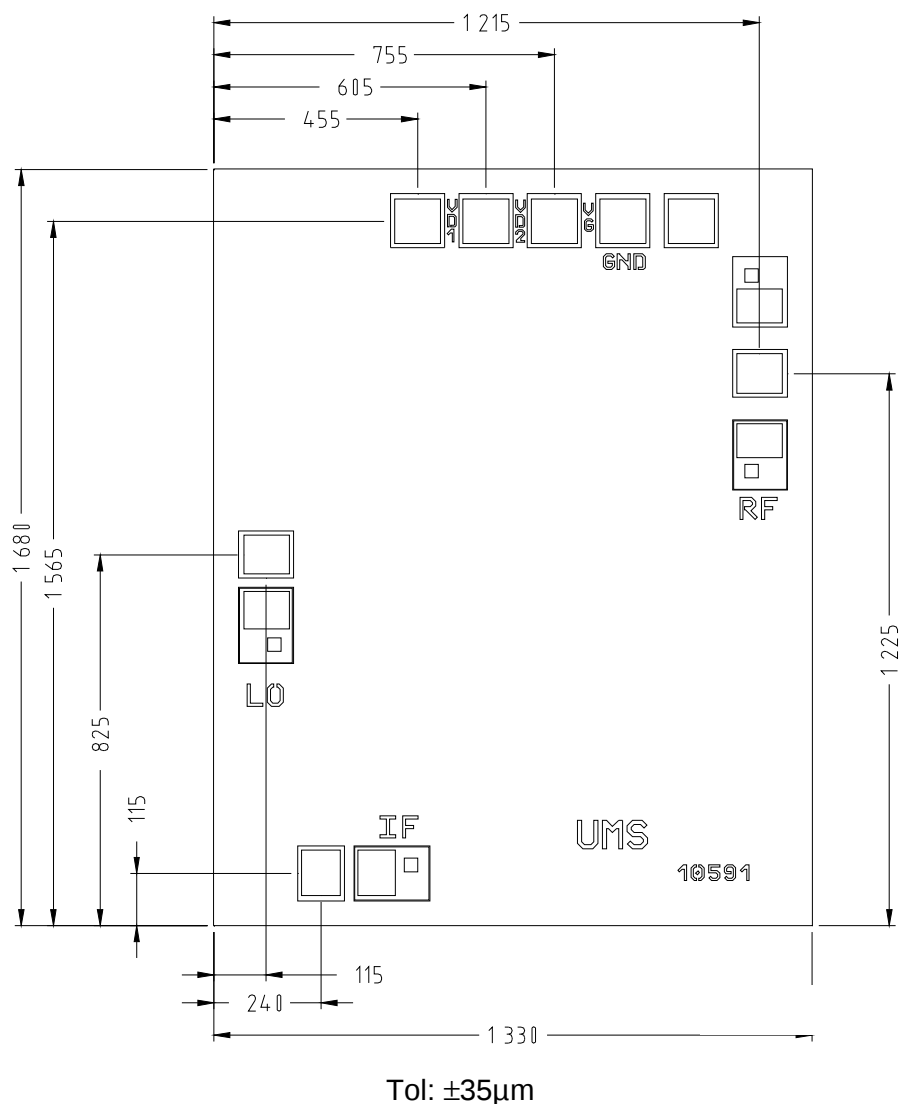


25µm wedge bonding is recommended

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

Mechanical data



(Chip thickness: 100µm. All dimensions are in micrometers)

Ordering Information

Chip form : CHR2297-98F/00

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