17-27GHz Integrated Down Converter

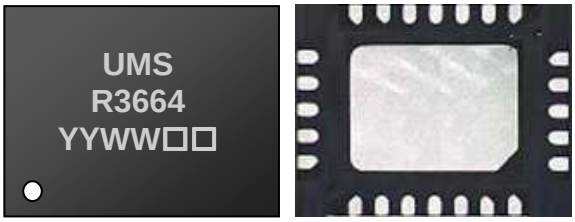
GaAs Monolithic Microwave IC in SMD package

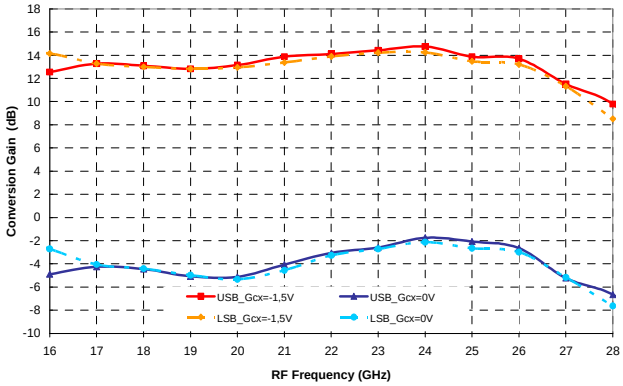
Description

The CHR3664-QEG is a multifunction part, which integrates a balanced cold FET mixer, a multiplier by two, and a RF LNA including gain control. It is designed for a wide range of applications, typically ISM and commercial communication systems.

The circuit is manufactured on a robut high volume pHEMT process, 0.25µm gate length.

It is supplied in lead-free SMD package.





Main Features

- Broadband RF performance 17-27GHz
- 13dB conversion gain
- 2dBm Input IP3
- 16dB Gain Control
- 15dBc Image Rejection
- 24LQFN4x5 – MSL1
- ESD protected

Main Characteristics

Tamb = +25°C, Vd = 4.5V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	17		26.5	GHz
F_{LO}	LO frequency range	7		15.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G_c	Conversion gain		13		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Tamb = +25℃, VD = VDL = 4.5V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	17.0		26.5	GHz
F_{LO}	LO frequency range	7.0		15.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G_c	Conversion gain@ min. attenuation	9	13		dB
ΔG	Gain control range		16		dB
NF	Noise Figure@ min. att. from 17 to 24GHz		3.2	3.7	dB
	Noise Figure@ min. att. from 24 to 26.5GHz		4.0	4.5	dB
Im_rej	Image rejection (1)		15		dBc
P_{LO}	LO Input power		0	5	dBm
IIP3	Input IP3 @ min. attenuation	0	2		dBm
	Input IP3 @ all gain range (ΔG)	-4	-2		dBm
2LO/RF	2LO leakage at RF port @ max. gain		-40		dBm
VD, VDL	DC drain voltage		4.5		V
Id	Drain current (ID + IDL)		360		mA
VGL	LNA DC gate voltage		-0.4		V
GC2, GC3	Gain control DC voltage	-2	-1.5	+0,6	V
VGM	Mixer DC gate voltage		-0.7		V

(1) An external combiner 90° is required on I / Q.
(2) The best noise figure is obtained with VGL tuned for IDL = 110mA

These values are representative of on board measurements as defined on the drawing at paragraph “Evaluation mother baord”.

Note: Id not affected by GC2, GC3.
Note: Electrostatic discharge sensitive device observe handling precautions!

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Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage	5	V
Id	Maximum drain bias current	450	mA
VGL	LNA DC gate voltage	-2.0 to +0.4	V
VGM	Mixer DC gate voltage	-2.0 to +0.4	V
GC1, 2	Gain control voltage	-2.5 to + 0.8	V
P_RF	Maximum peak input power overdrive	10	dBm
P_LO	Maximum LO input power	10	dBm
Tch	Maximum channel temperature (1)	175	℃
Ta	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (convection mode not considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

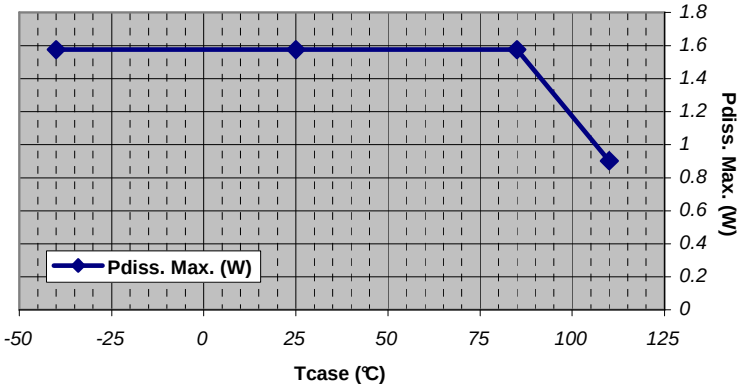
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified in order to guarantee the nominal device life time (MTTF) (see the curve Pdiss. Max below).

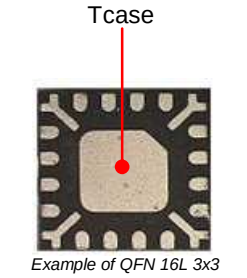
DEVICE THERMAL SPECIFICATION : CHR3664-QEG			
Recommanded max. junction temperature (Tj max)		:	143 °C
Junction temperature absolute maximum rating		:	175 °C
Max. continuous dissipated power @ Tcase=	85 °C	:	1.575 W
=> Pdiss derating above Tcase(1)=	85 °C	:	27 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)		:	<37 °C/W
Min. package back side operating temperature(3)		:	-40 °C
Max. package back side operating temperature(3)		:	85 °C
Min. storage temperature		:	-55 °C
Max. storage temperature		:	125 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hotter junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example of QFN 16L 3x3 back-side view, temperature reference point (Tcase) location.

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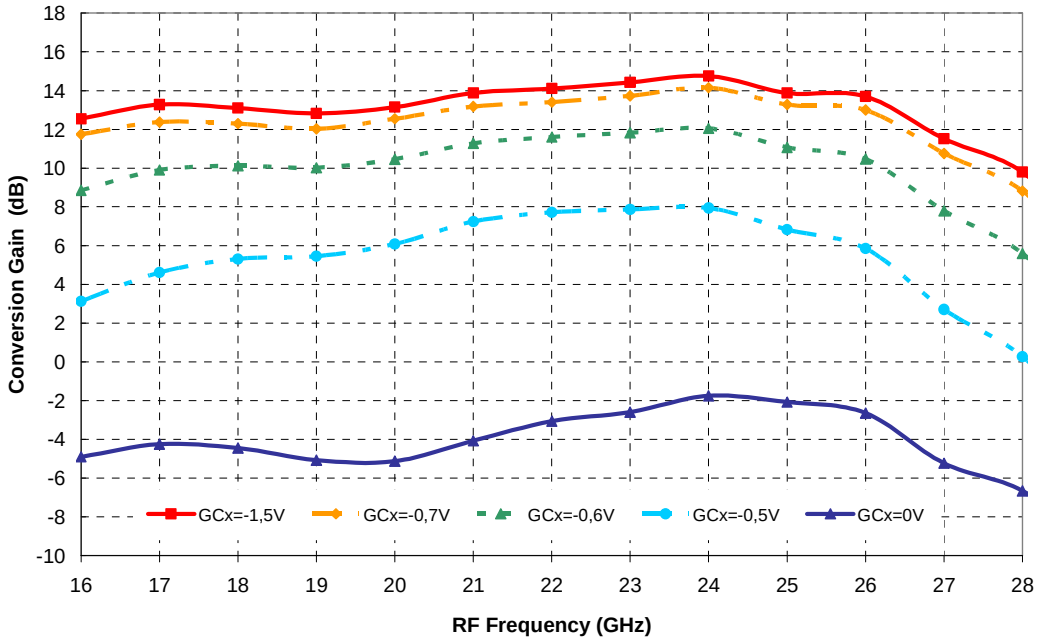
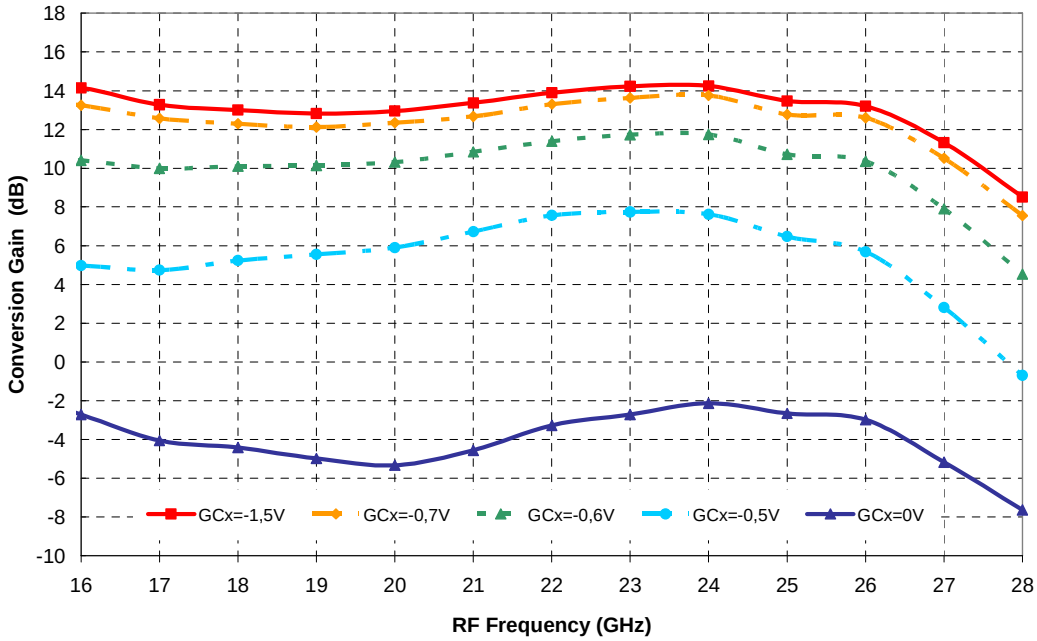
Typical Measured Performances

Tamb = +25°C, VD = VDL = 4.5V, VGL = -0.4V, VGM = - 0.7V, P_LO = 0dBm
If no specific mention, the following values are representative of onboard measurements (on connector access planes) as defined on the drawing at paragrah “Evaluation mother baord”. The board losses are estimated from 1.5 to 2dB in the frequency range.

Conversion Gain in Supradyne Mode versus RF Frequency & GCx
F_RF = 2xF_LO+F_IF, F_IF = 2.0GHz
Board losses deeembedded (result given on package access planes)



Conversion Gain in Infradyne Mode versus RF Frequency & GCx
RF = 2xF_LO-F_IF, F_IF = 2.0GHz
Board losses deeembedded (result given on package access planes)



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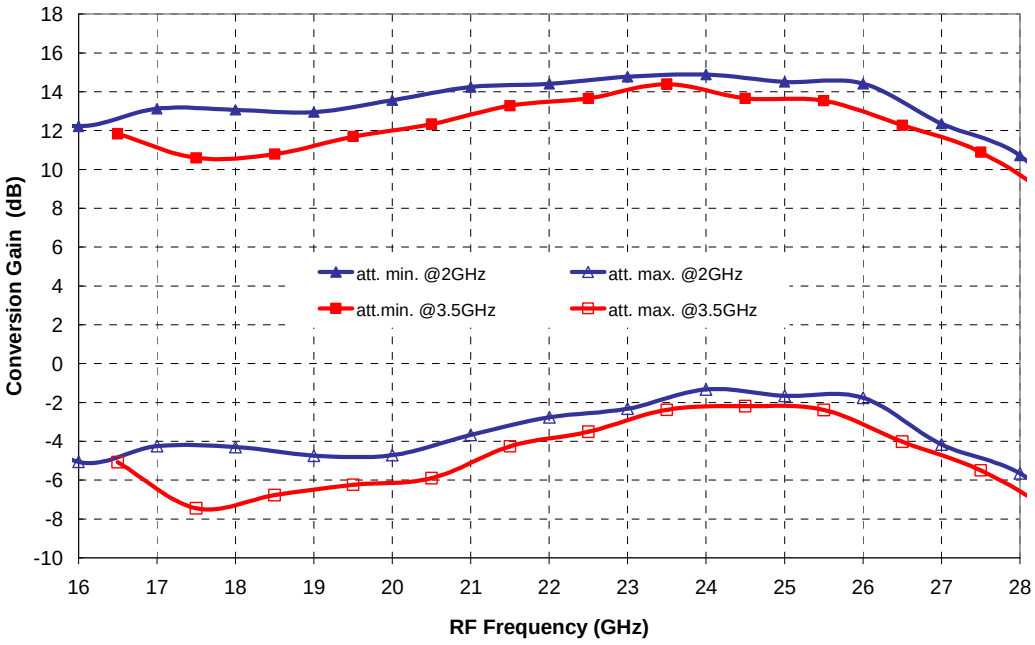
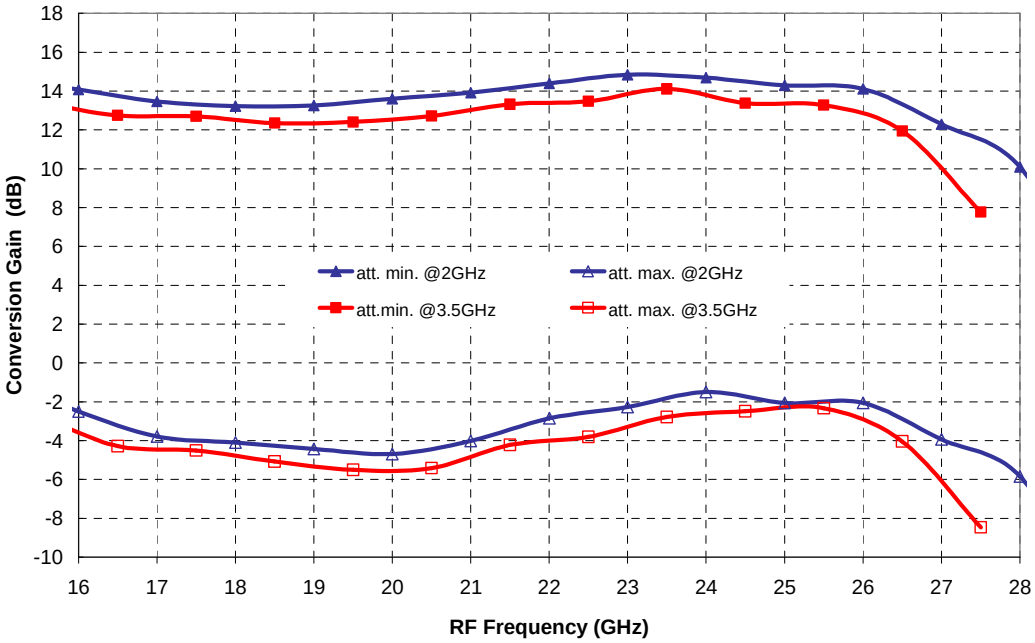
Conversion Gain in Supradyne Mode versus RF Frequency & IF
F_RF = 2xF_LO+F_IF, GCx = -1.5V & 0V
Board losses deeembedded (result given on package access planes)



Conversion Gain in Infradyne Mode versus RF Frequency & IF
RF = 2xF_LO-F_IF, GCx = -1.5 & 0V
Board losses deeembedded (result given on package access planes)



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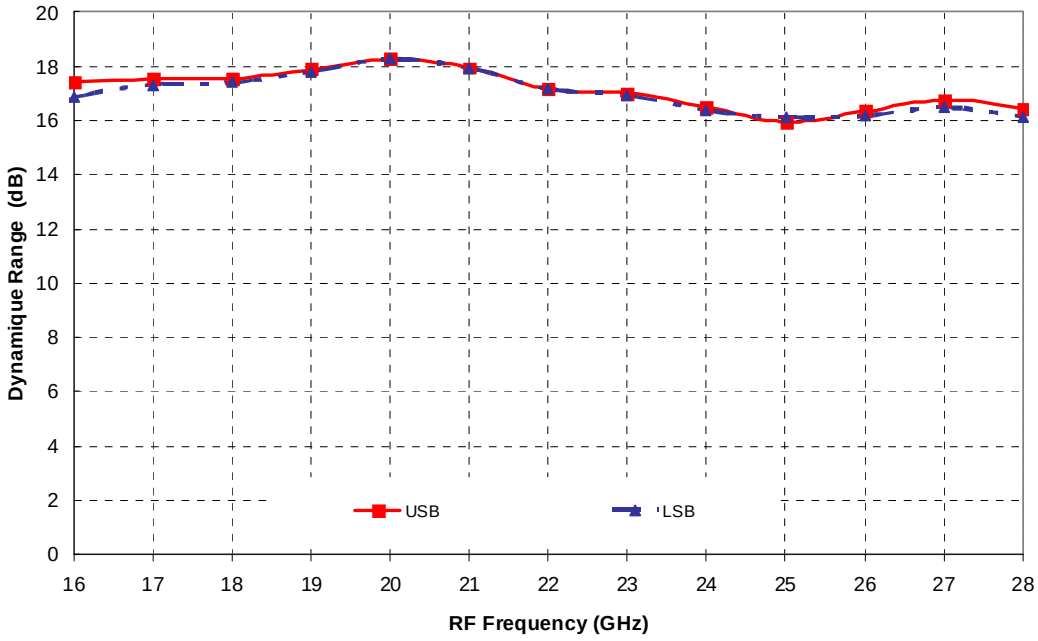
Dynamic Range (Gcmax – Gcmin) versus Frequency
F_RF = 2xF_LO-F_IF & F_RF = 2xF_LO+F_IF, F_IF = 2.0GHz



Noise Figure at min. att. versus Frequency
F_RF = 2xF_LO-F_IF & F_RF = 2xF_LO+F_IF, F_IF = 2.0GHz, GCx = -1.5V
Board losses deeembedded (result given on package access planes)

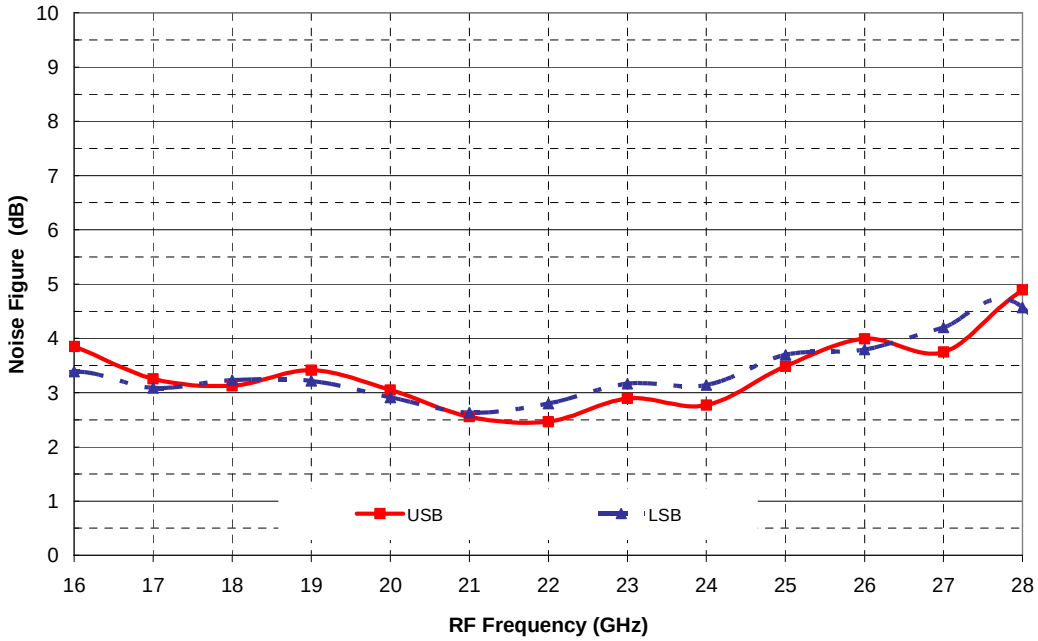


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Image Rejection on Supradyne & Infradyne Mode versus Frequency
F_IF = 2.0GHz, GCx = -1.5V

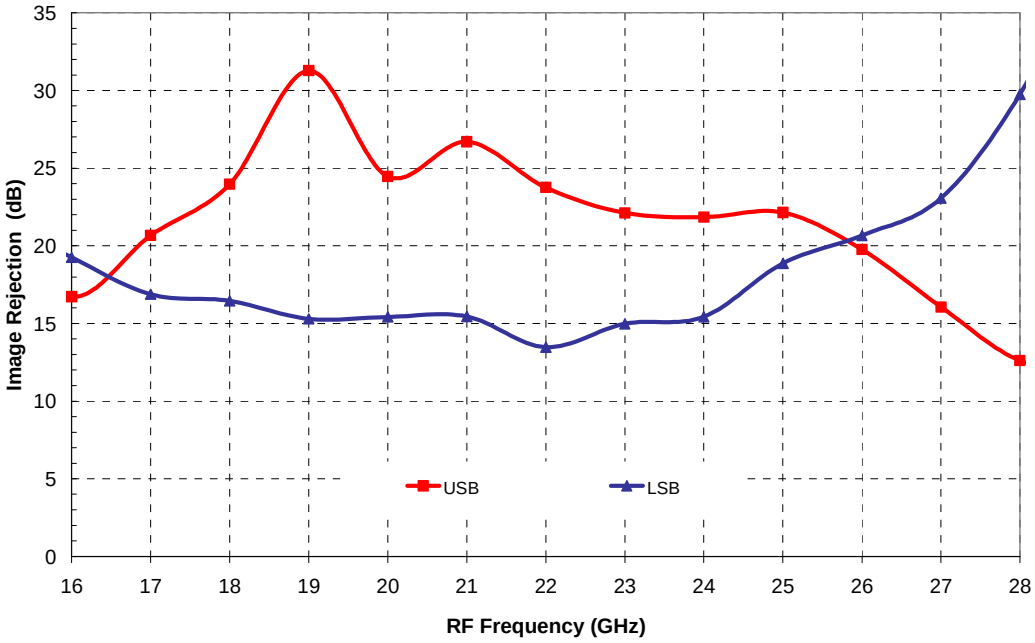
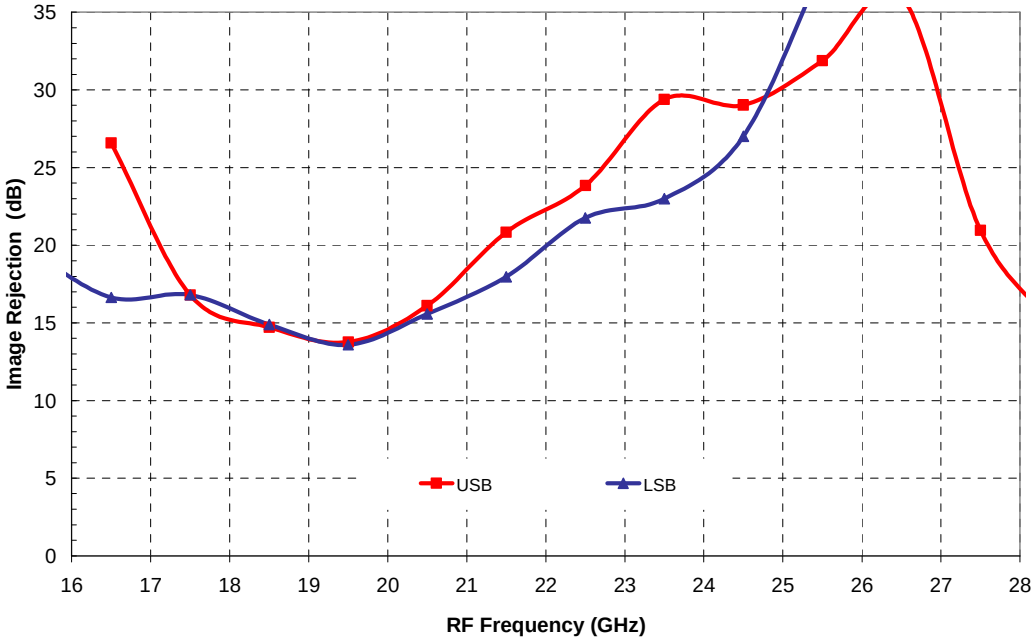


Image Rejection on Supradyne & Infradyne Mode versus Frequency
F_IF = 3.5GHz, GCx = -1.5V



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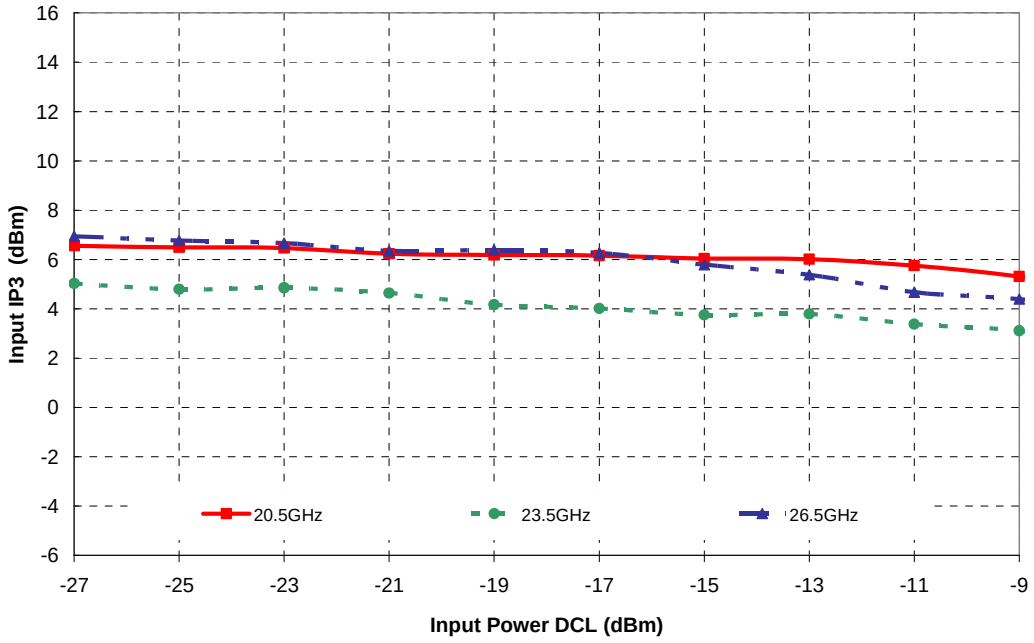
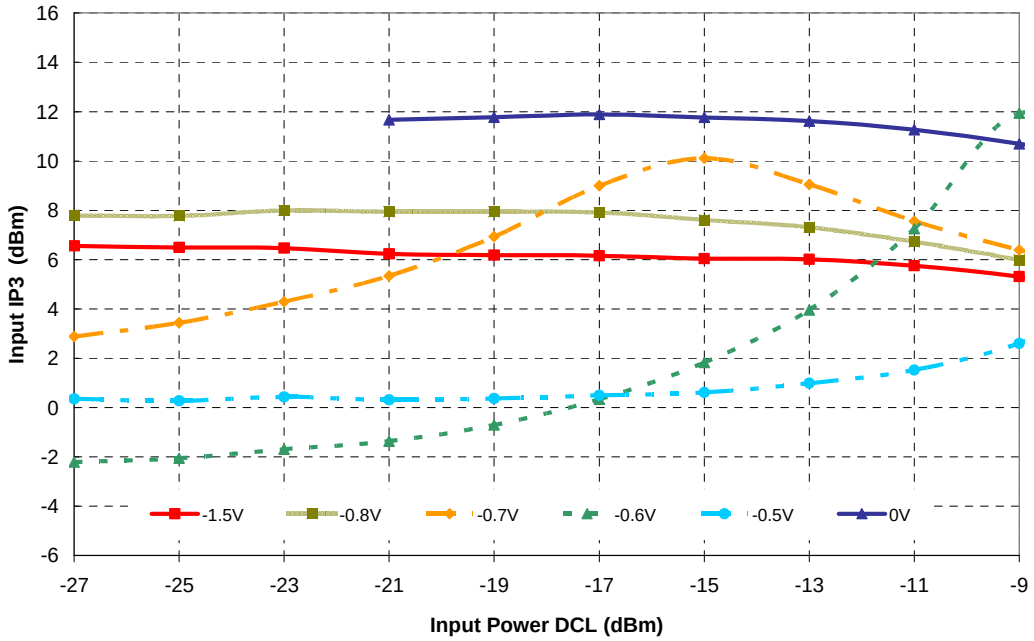
Input IP3 versus Frequency at GCx = -1.5V
F_RF = 2xF_LO+F_IF, F_IF = 3.5GHz



Input IP3 versus GCx
F_RF = 2xF_LO+F_IF, F_RF = 20.5GHz, F_IF = 3.5GHz



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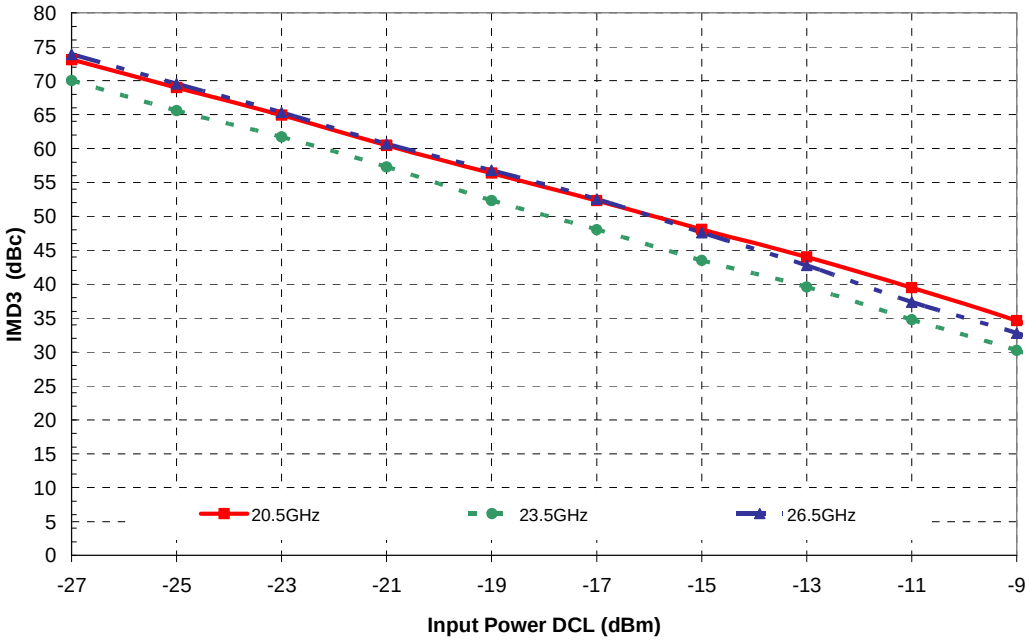
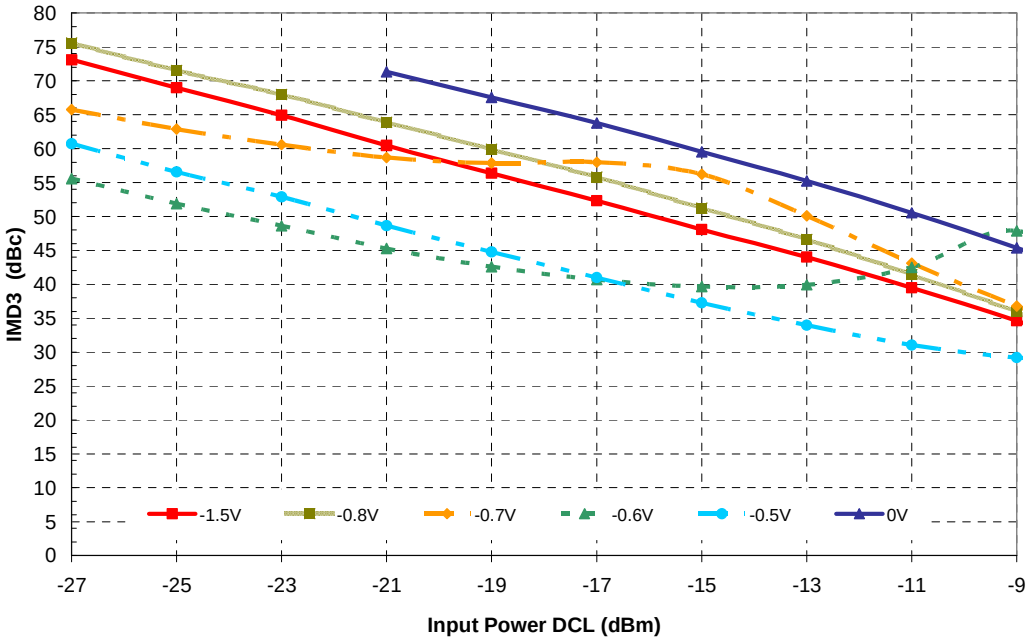
IMD3 versus Frequency at GCx = -1.5V
F_RF = 2xF_LO+F_IF, F_IF = 3.5GHz



IMD3 versus GCx
F_RF = 2xF_LO+F_IF, F_RF = 20.5GHz, F_IF = 3.5GHz



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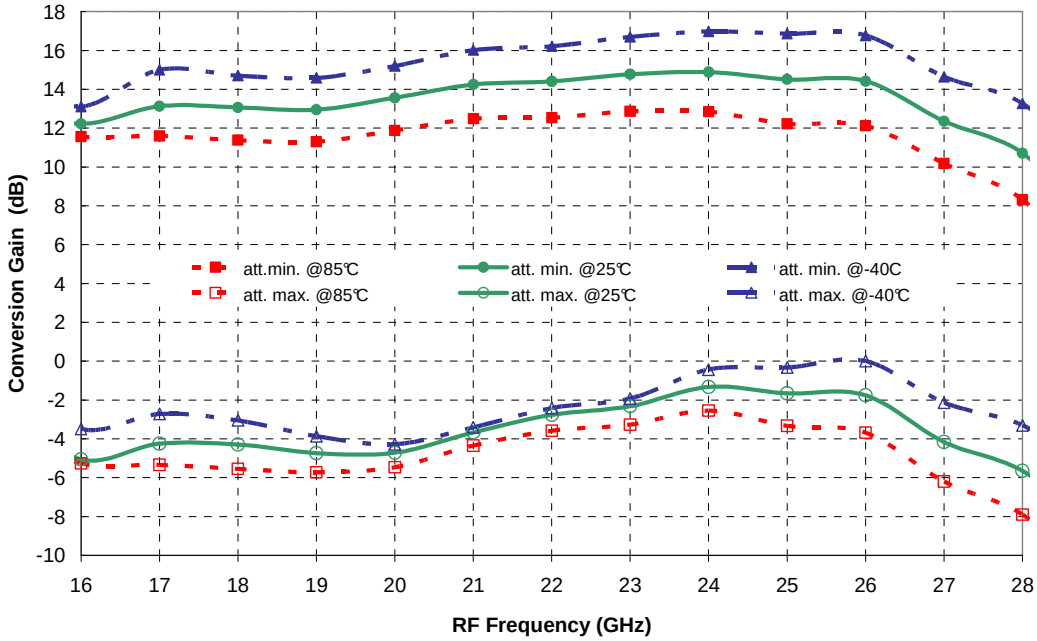
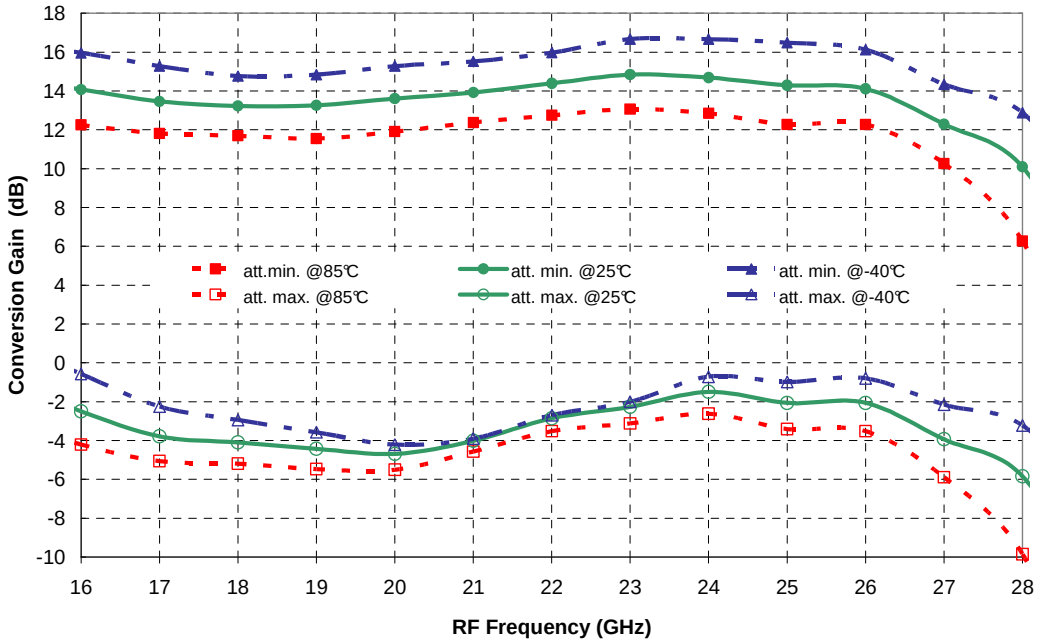
Temperature Measurements

T = [-40, +25, 85] ℃, VD = VDL = 4.5V, VGL = -0.4V , VGM = -0.7V, P_LO = 0 dBm
If no specific mention, the following values are representative of on board measurements (on connector access planes) as defined on the drawing at paragprah “Evaluation mother baord”. The board losses are estimated from 1.5 to 2dB in the frequency range.

Conversion Gain in Supradyne Mode versus Frequency
F_RF = 2xF_LO+F_IF, F_IF = 2.0GHz, GCx = -1.5V & 0V
Board losses deeembedded (result given on package access planes)



Conversion Gain in Infradyne Mode versus Frequency
RF = 2xF_LO-F_IF, F_IF = 2.0GHz, GCx = -1.5V & 0V
Board losses deeembedded (result given on package access planes)



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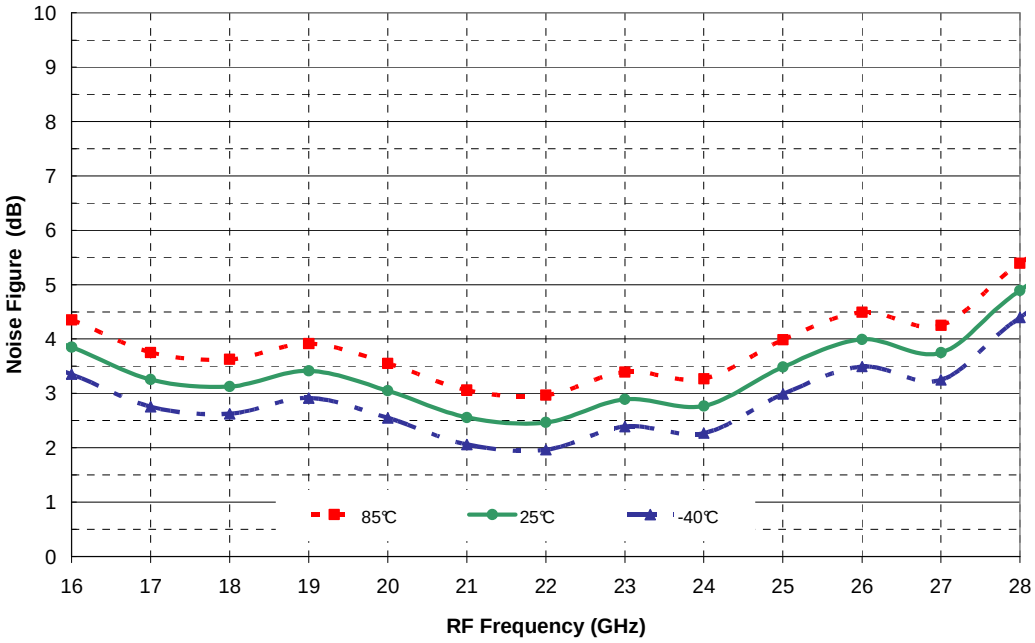
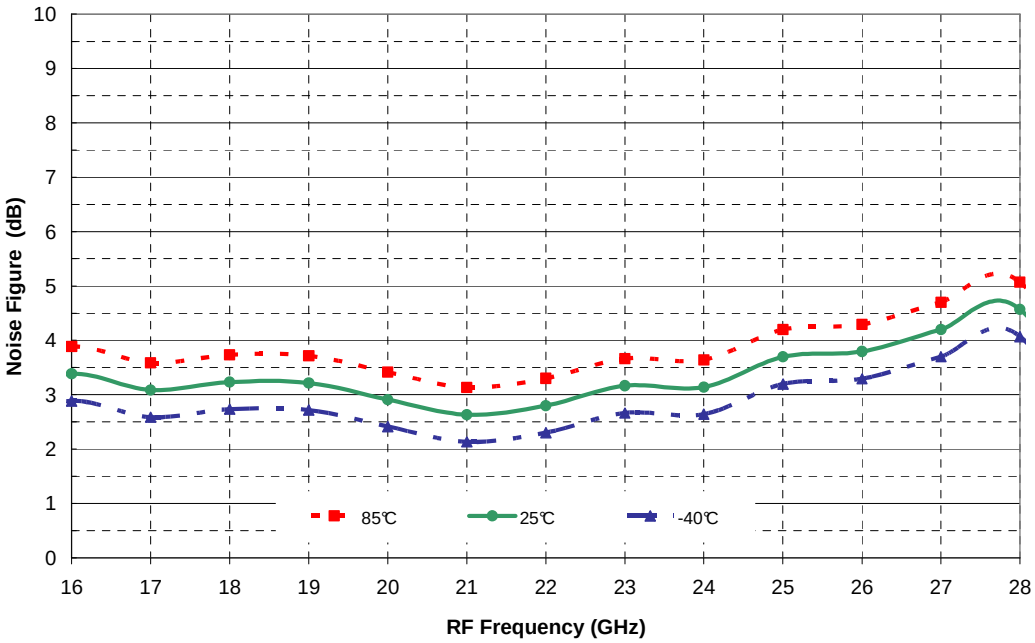
Noise Figure in Supradyne Mode at min. att. versus Frequency
F_RF = 2xF_LO+F_IF, F_IF = 2.0GHz, GCx = -1.5V
Board losses deeembedded (result given on package access planes)



Noise Figure in Infradyne Mode at min. att. versus Frequency
F_RF = 2xF_LO-F_IF, F_IF = 2.0GHz, GCx = -1.5V
Board losses deeembedded (result given on package access planes)



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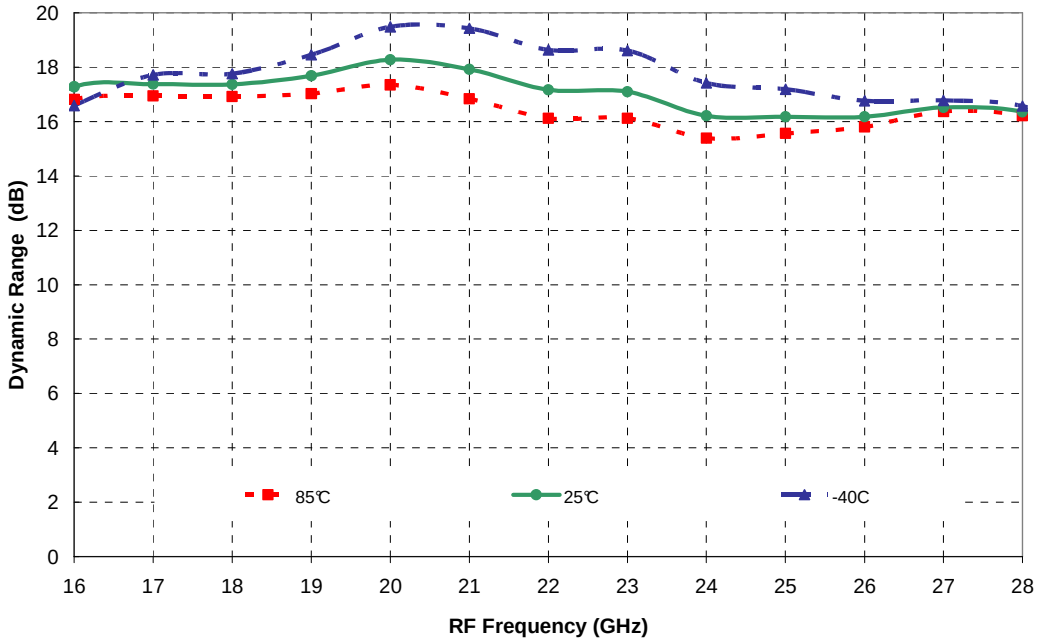
Dynamic Range (Gcmax – Gcmin) in Supradyne Mode versus Frequency
F_RF = 2xF_LO+F_IF, F_IF = 2.0GHz



Dynamic Range (Gcmax – Gcmin) in Infradyne Mode versus Frequency
F_RF = 2xF_LO-F_IF, F_IF = 2.0GHz

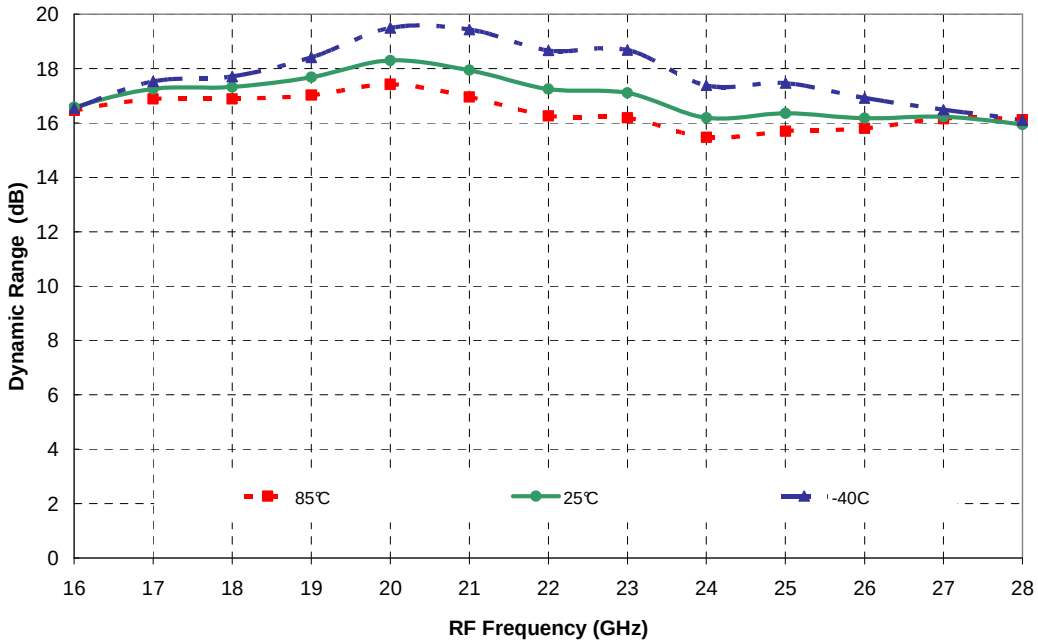


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Image Rejection on Supradyne Mode versus Frequency
F_IF = 2.0GHz, GCx = -1.5V

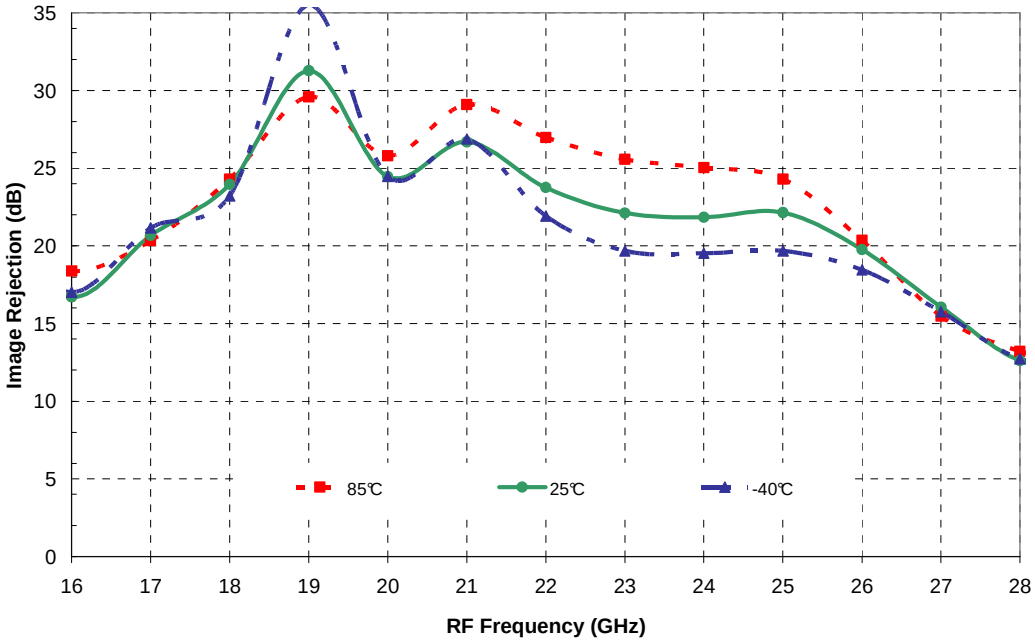
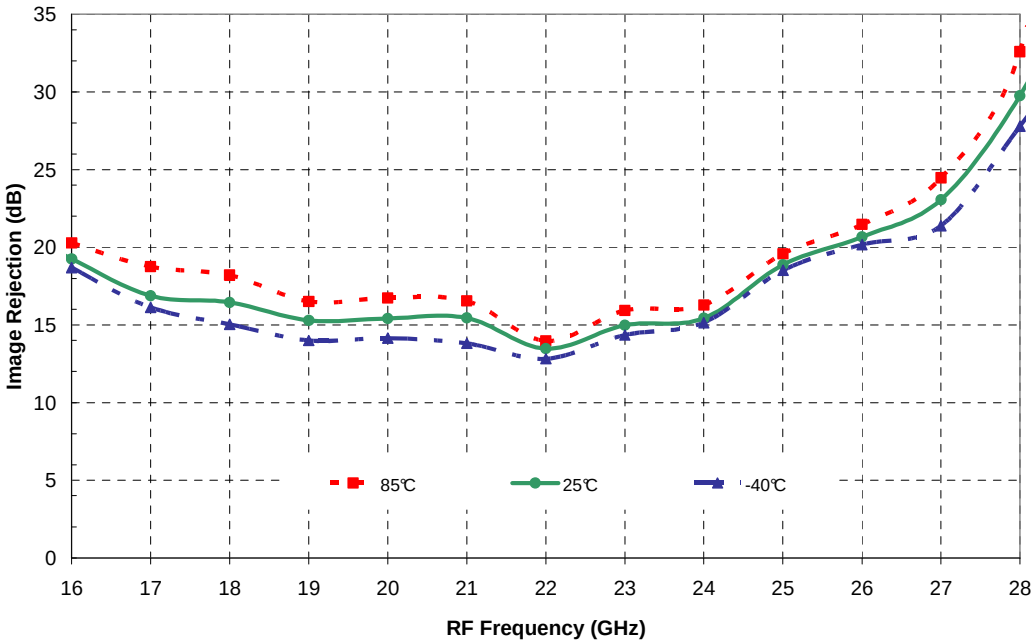


Image Rejection on Infradyne Mode versus Frequency
F_IF = 2.0GHz, GCx = -1.5V



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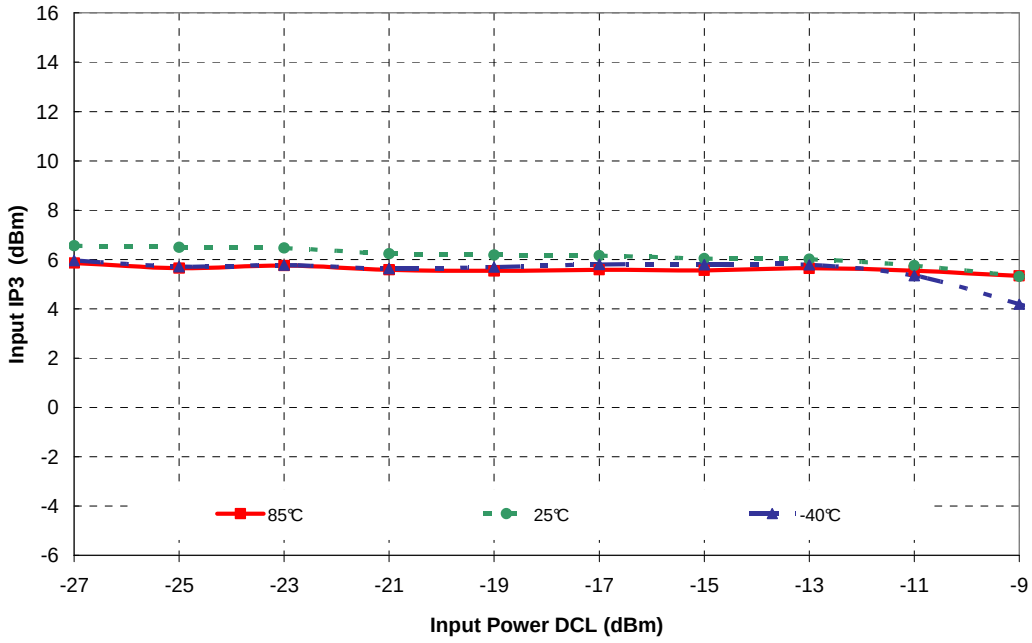
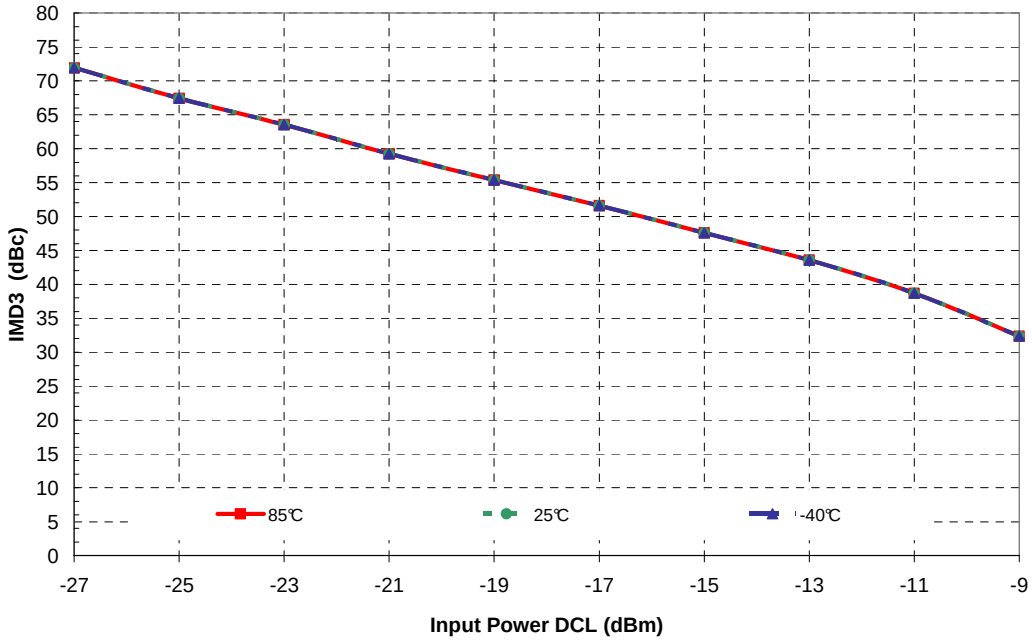
Input IP3 versus Temperature at GCx = -1.5V
F_RF = 2xF_LO+F_IF, F_RF = 20.5GHz, F_IF = 3.5GHz



IMD3 versus Temperature at GCx = -1.5V
F_RF = 2xF_LO+F_IF, F_RF = 20.5GHz, F_IF = 3.5GHz



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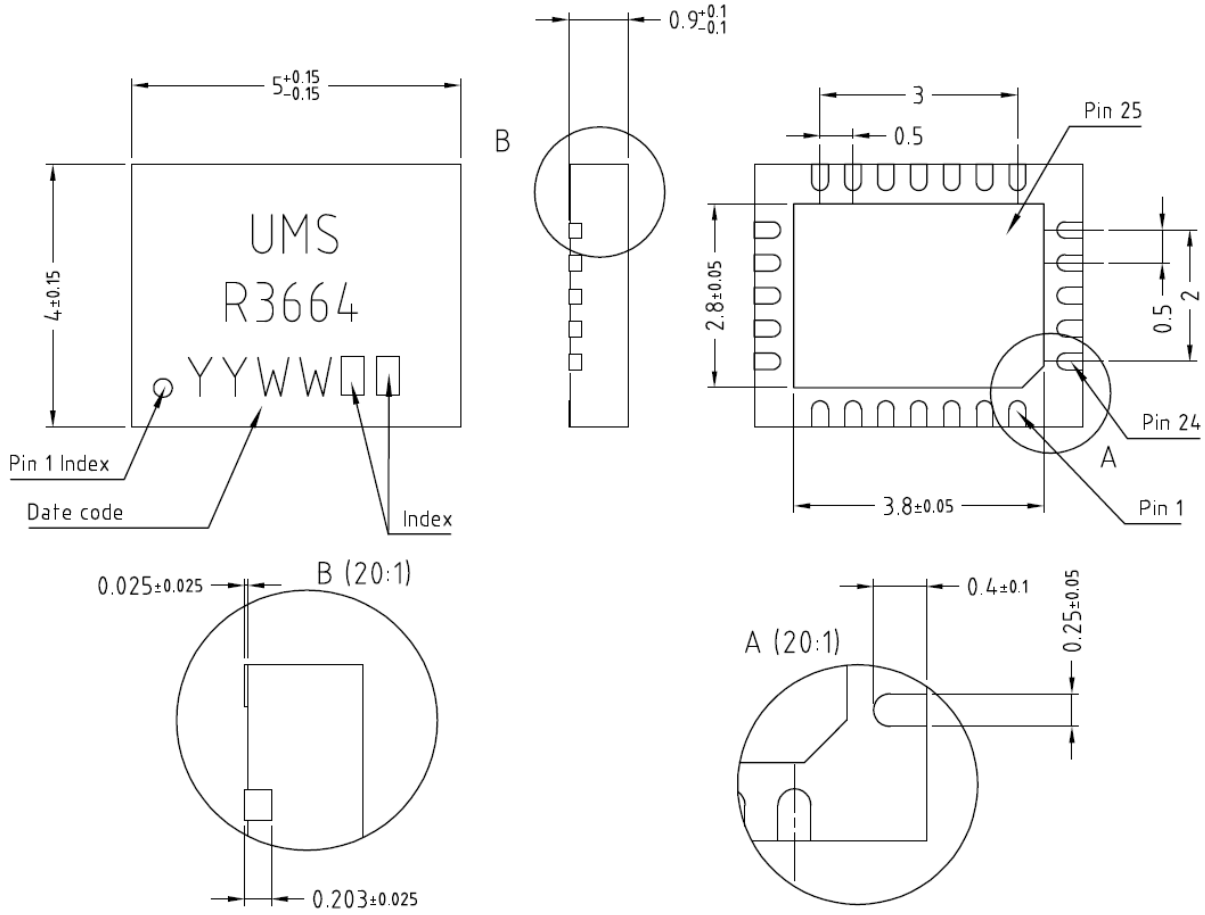
Package outline (1)



Units : mm

From the standard : JEDEC MO-220 [VGHD]

Matt tin, Lead free (Green)

1- Nc	9- VGL	17- Nc	25- GND Exposed pad
2- Nc	10- VDL	18- Nc	
3- Nc	11- VGM	19- Nc	
4- GND(2)	12- VD	20- IF_I out	
5- RF in	13- Nc	21- GND(2)	
6- GND(2)	14- GND(2)	22- IF_Q out	
7- GC3	15- LO in	23- Nc	
8- GC2	16- GND(2)	24- Nc	

(1)The package outline drawing included to this data-sheet is given for indication. Refere to the application note AN0017 available at http://www.ums-gaas.com for exact package dimensions.

(2)It is strongly recommended to ground on the PCB board all the pins referenced as GND.

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

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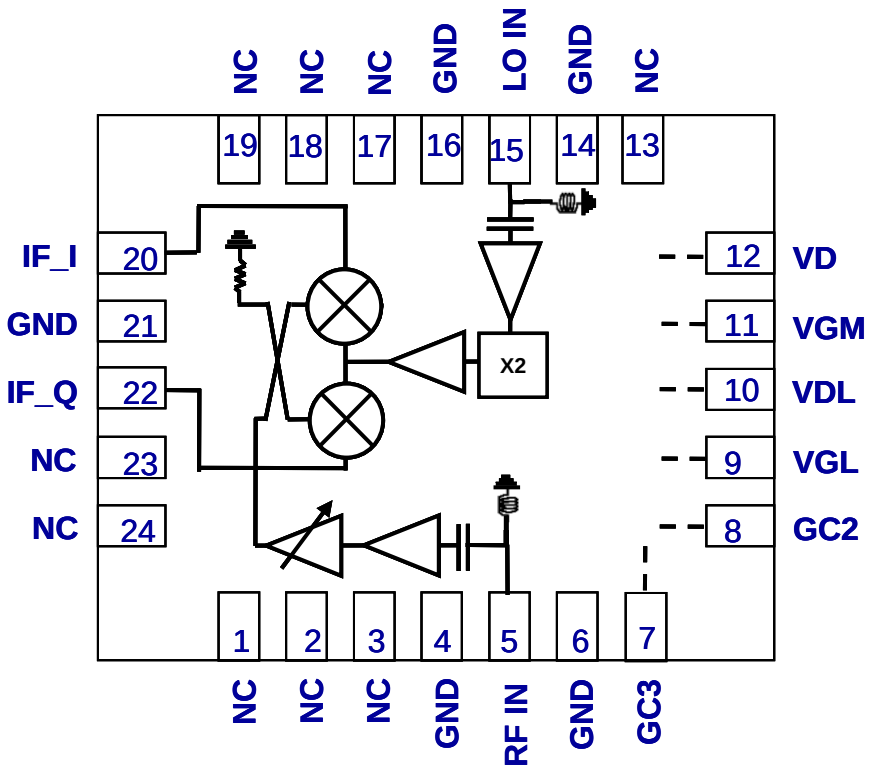
Notes

Due to ESD protection circuits on RF and LO inputs, an external capacitance might be requested to isolate the product from external voltage that could be present on these accesses in the application.



ESD protections are also implemented on gate accesses.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

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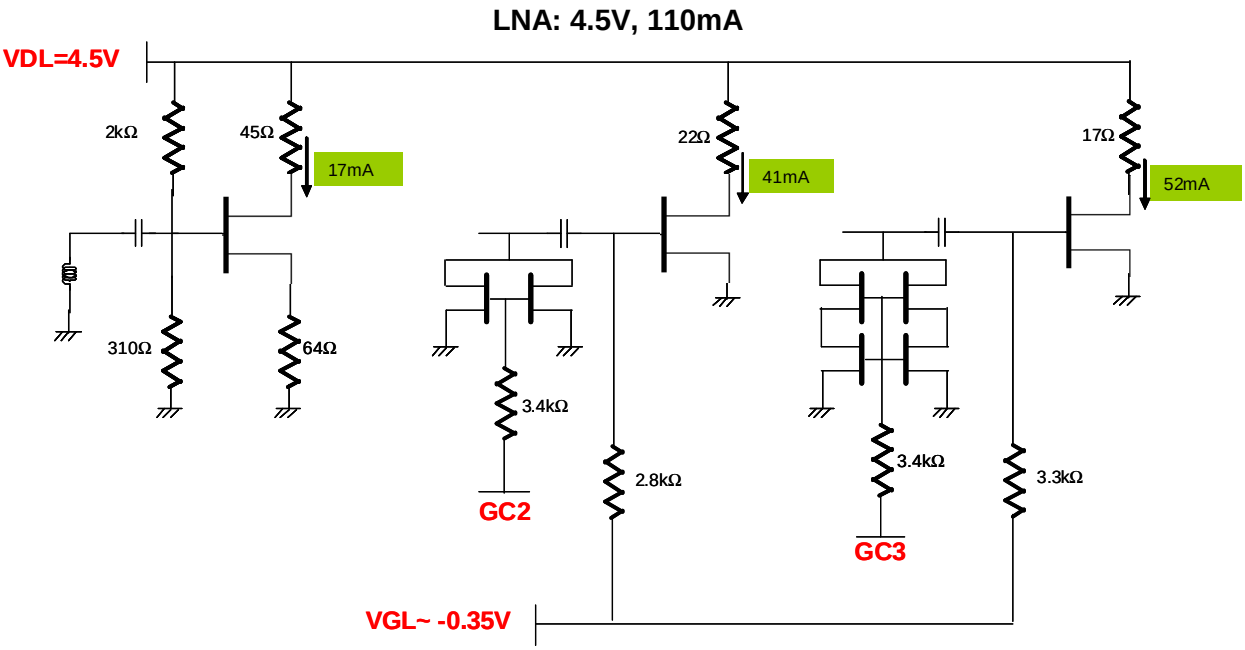
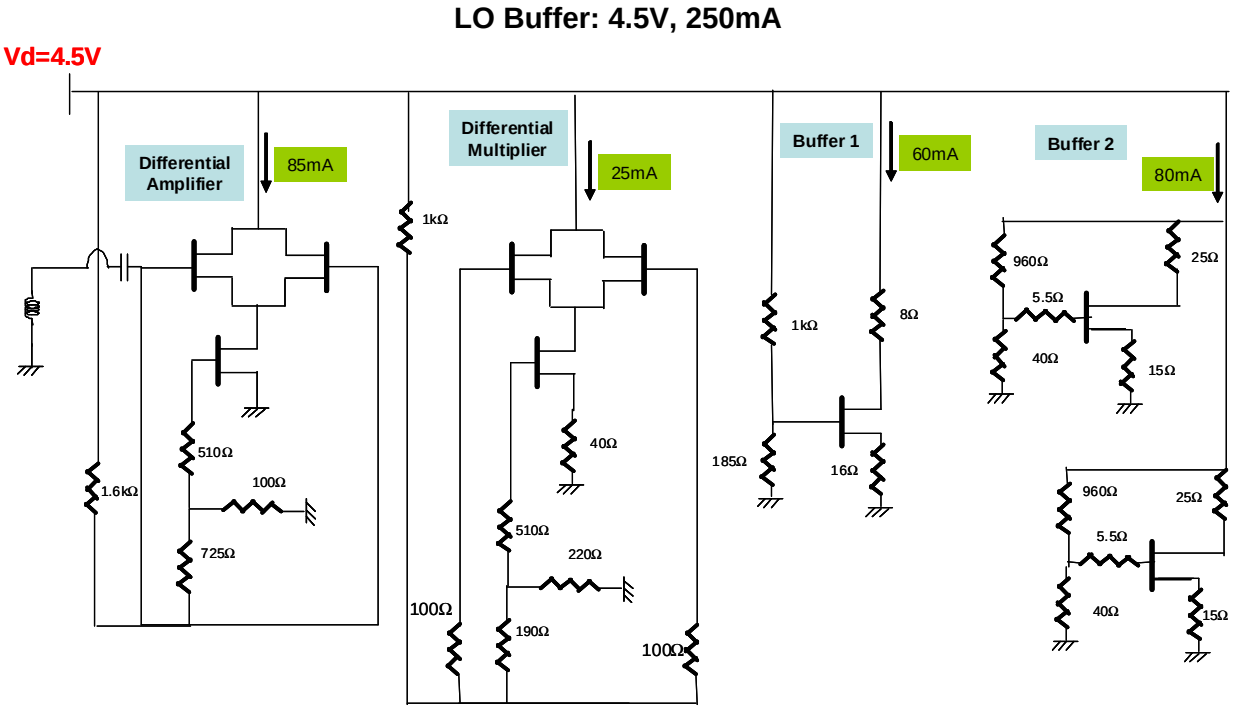
DC Schematic





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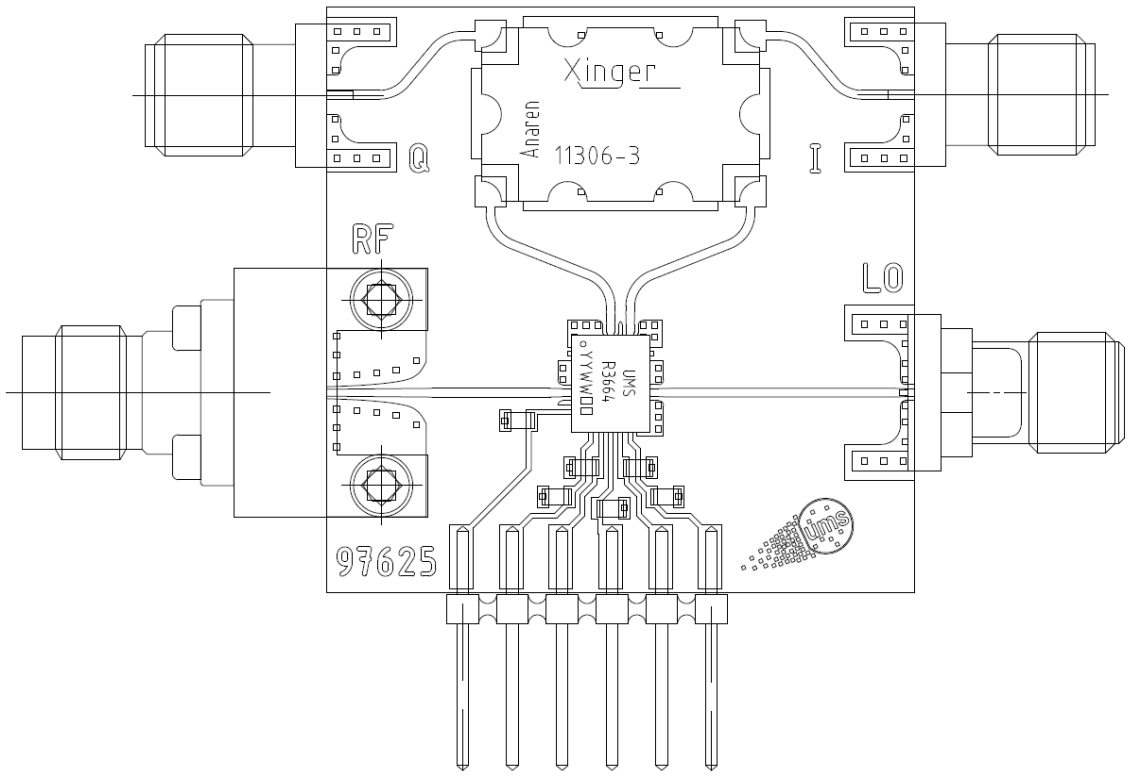
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- (See application note AN0017 for details).



Decoupling Capacitors = 10nF
Hybrid coupler Anaren 90°2-4GHz

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Notes:

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Ordering Information

QFN 4x5 RoHS compliant package: CHR3664-QEG/XY
Stick: XY = 20 Tape & reel: XY = 21

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