21-26.5GHz Integrated Down converter

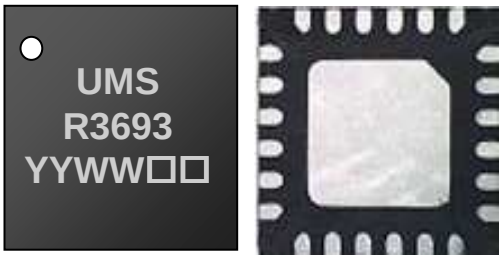
GaAs Monolithic Microwave IC in SMD package

Description

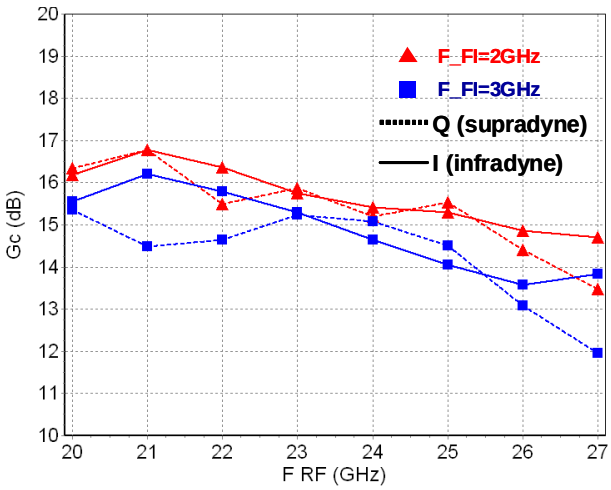
The CHR3693-QDG is a multifunction part, which integrates a balanced cold FET mixer, a time two multiplier, and a RF LNA. It is designed for a wide range of applications, typically commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate and air bridges.

It is supplied in lead-free SMD package.



Conversion gain (Inf. & Sup. Mode)



Main Features

- Broadband performance 21-26.5GHz
- 14dB gain
- -5dBm IIP3
- 18dBc Image rejection
- 24LQFN4x4
- MSL Level : 1

Main Characteristics

Tamb = +25°C, Vd= 4V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	21		26.5	GHz
F_{LO}	LO frequency range	9		14	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G_c	Conversion gain	12	14		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Tamb=25℃, Vdx=Vdl = 4V, Typical Vgx = -0.9V & Vgm= -0.7V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	21		26.5	GHz
F_{LO}	LO frequency range	9		14	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G_c	Conversion gain	12	14		dB
NF	Noise Figure		3	3.5	dB
P_{LO}	LO Input power		2	5	dBm
Img Sup	Image Suppression (1)	15	18		dBc
IIP3	Input IP3		-5		dBm
LO RL	LO return loss		-9.5	-7	dB
RF RL	RF return loss (21 to 24GHz)		-12	-7	dB
	RF return loss (24 to 26.5GHz)		-8	-6	dB
LO/RF	Isolation LO → RF		45		dBc
2LO/RF	Isolation 2LO → RF		35		dBc
Id	Bias current (2) (Idl + Idx)	120	160	200	mA

(1) With external I/Q 90° hybrid coupler
(2) Typically, Idl= 90mA, Idx=70mA

These values are representative of onboard measurements as defined on the drawing at paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage	4.5	V
Id	Maximum drain bias current	230	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
P_{RF}	Maximum RF input power	10	dBm
P_{LO}	Maximum LO input power	10	dBm
Tch	Maximum channel temperature	175	℃
Ta	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

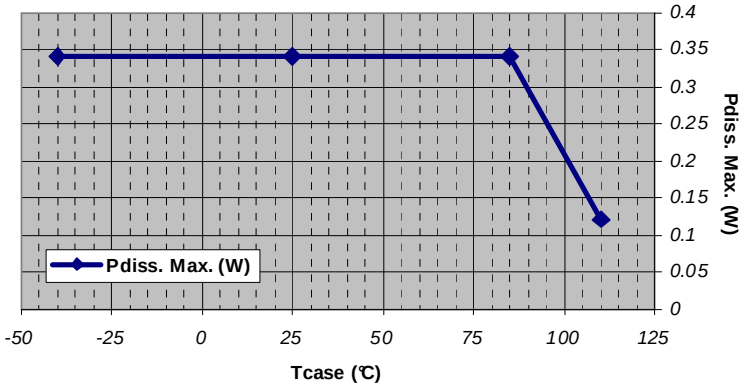
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

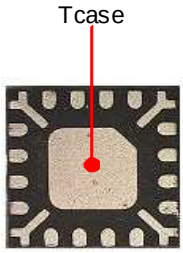
DEVICE THERMAL SPECIFICATION : CHR3693-QDG			
Recommanded max. junction temperature (Tj max)		:	124 °C
Junction temperature absolute maximum rating		:	175 °C
Max. continuous dissipated power @ Tcase=	85 °C	:	0.34 W
=> Pdiss derating above Tcase(1)=	85 °C	:	9 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)		:	<114 °C/W
Min. package back side operating temperature(3)		:	-40 °C
Max. package back side operating temperature(3)		:	85 °C
Min. storage temperature		:	-55 °C
Max. storage temperature		:	125 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hotter junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example of QFN 16L 3x3 back-side view, temperature reference point (Tcase) location.

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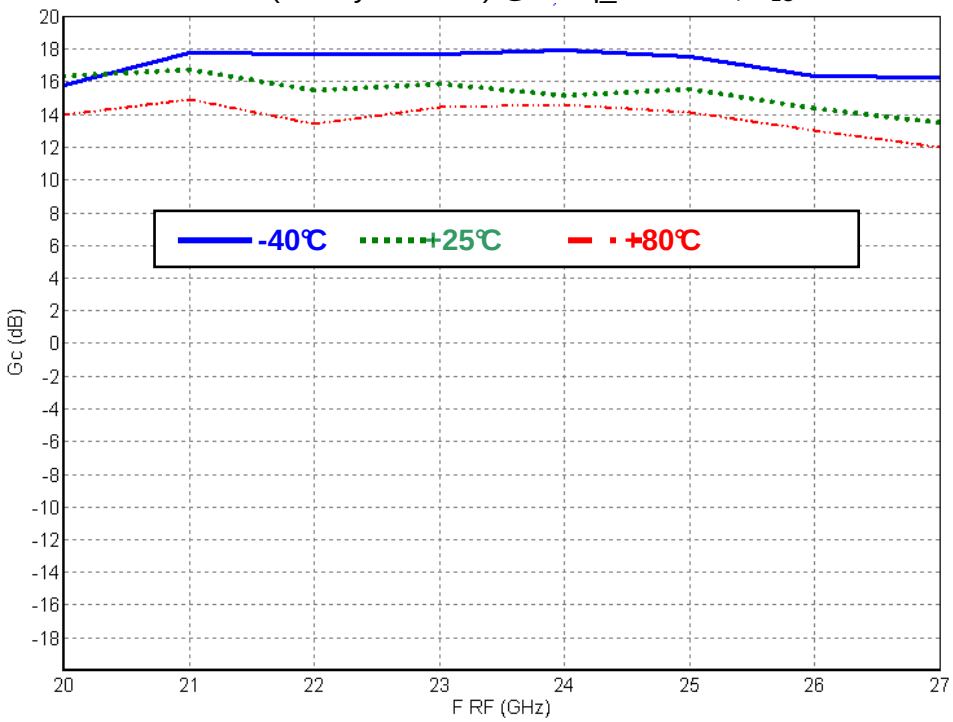
Typical Measured Performances

Tamb. = 25°C, Vdx=Vdl = 4V, Typical Vgx = -0.9V & V gm= -0.7V

These values are representative of onboard measurements, on connectors access planes, as defined on the drawing at paragraph "Evaluation mother board".

Conversion Gain (infradyne mode) @ Freq_IF=2GHz, P_{LO}=2dBm



Conversion Gain (supradyne mode) @ Freq_IF=2GHz, P_{LO}=2dBm

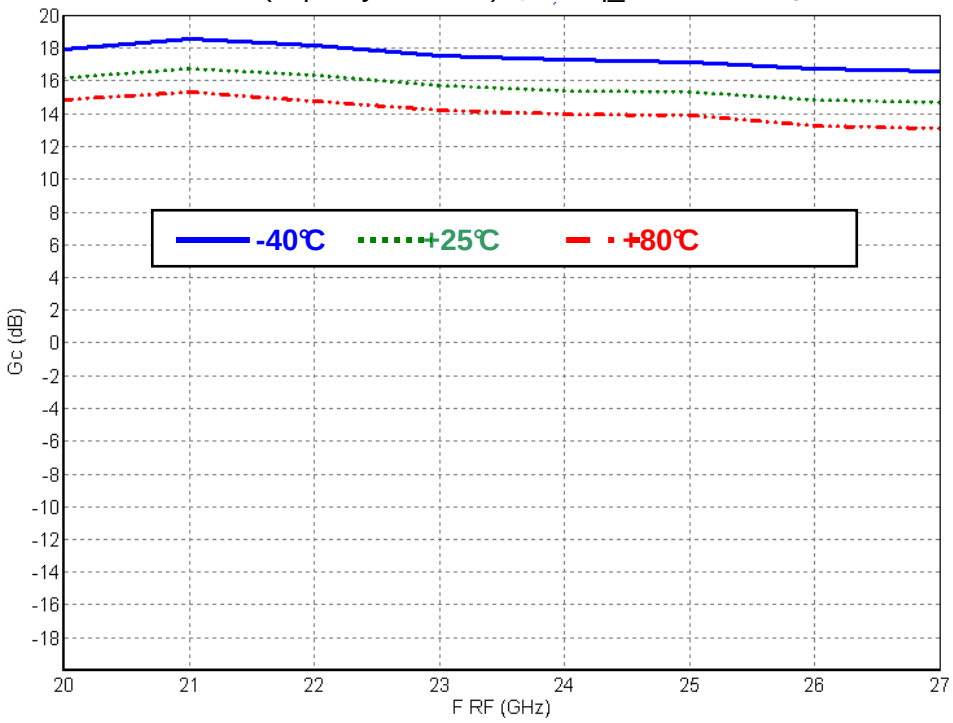


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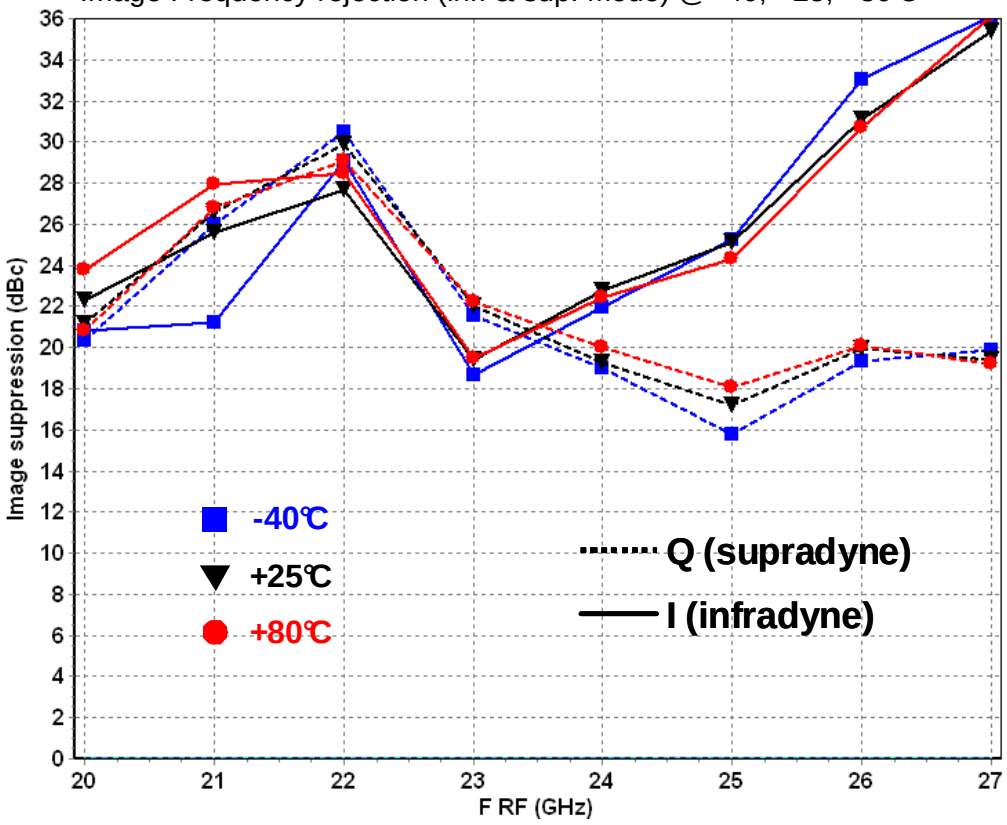
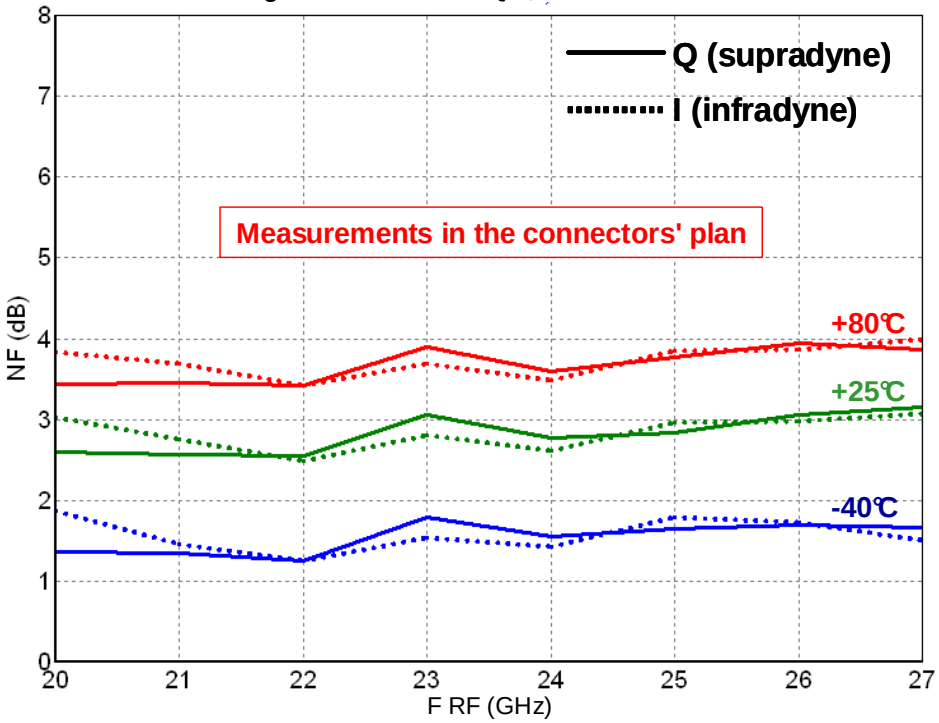
Image Frequency rejection (inf. & sup. Mode) @ -40, +25, +80℃



Noise figure channel I & Q @ -40, +25, +80℃



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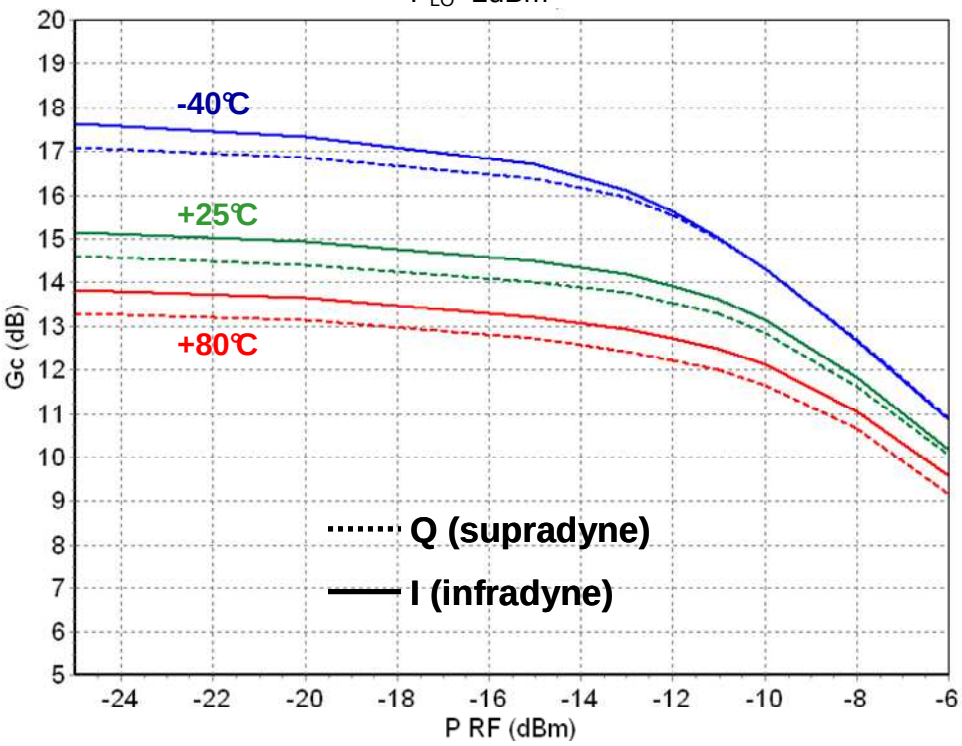
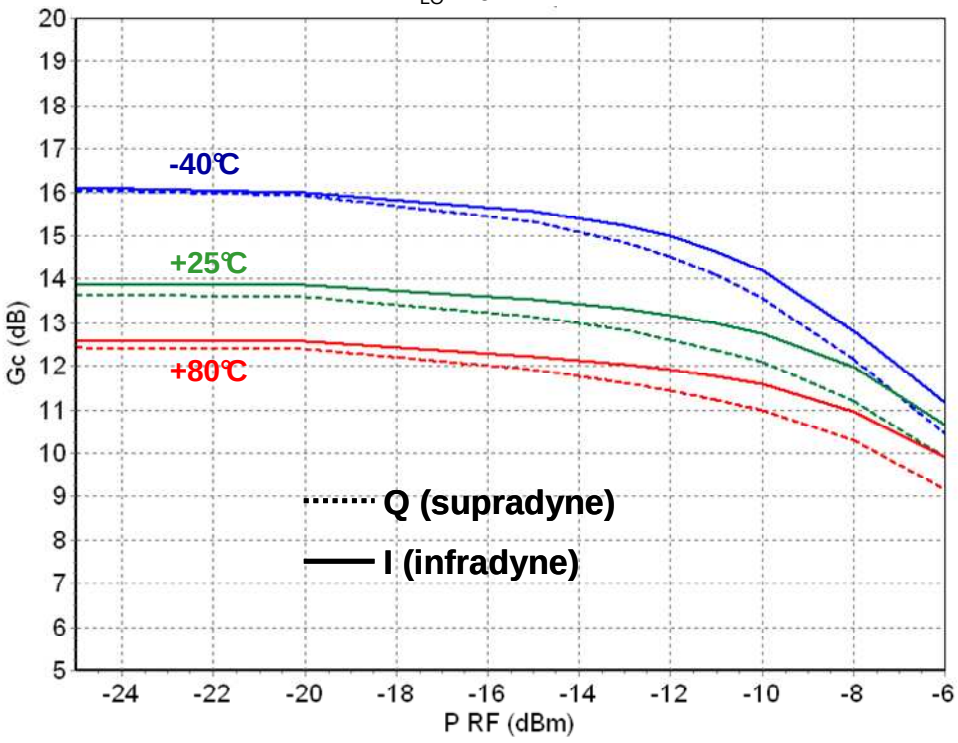
Compression vs P_{RF} (inf. & sup. Mode) @ F_RF=21GHz & F_IF=3GHz
P_{LO}=2dBm



Compression vs P_{RF} (inf. & sup. Mode) @ F_RF=26GHz & F_IF=2GHz
P_{LO}=2dBm



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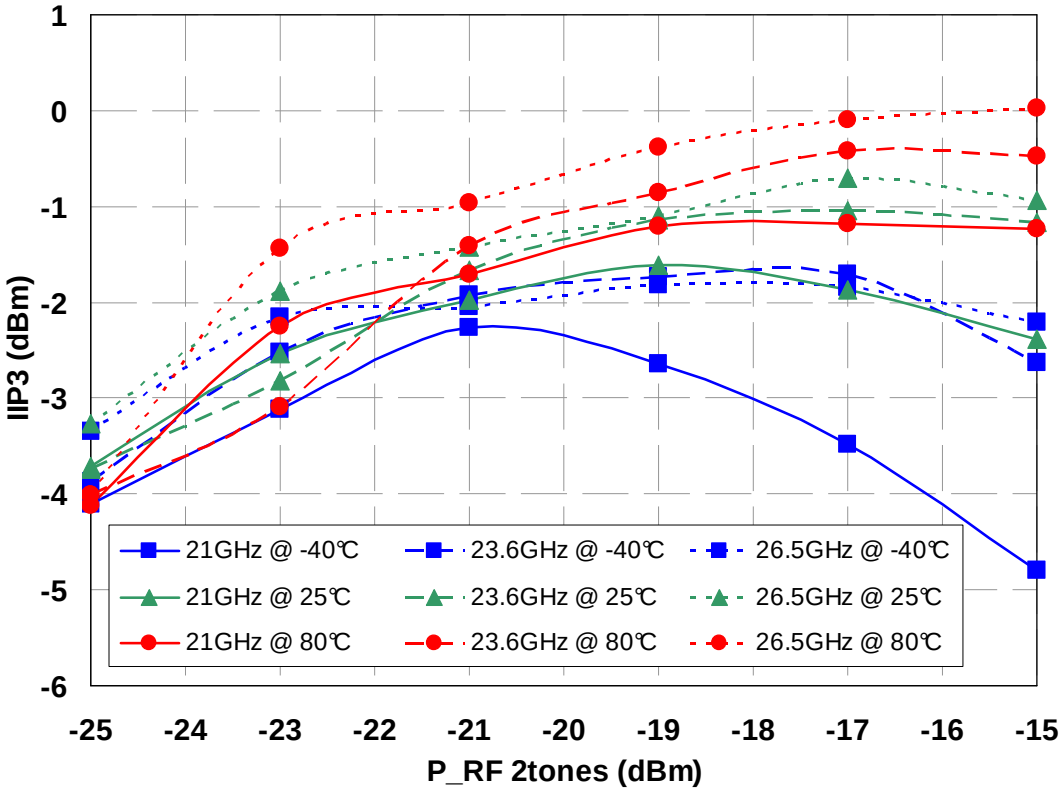
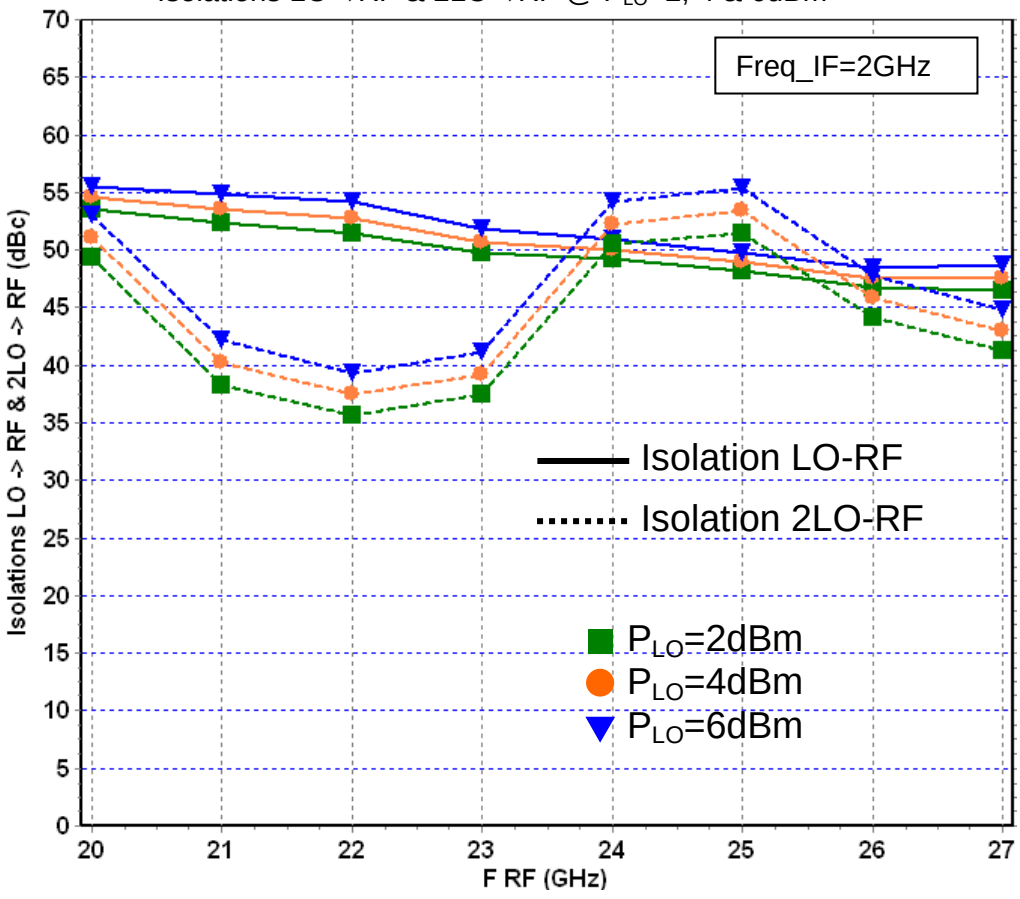
Input IP3 versus RF power



Isolations LO→RF & 2LO→RF @ P_{LO}=2, 4 & 6dBm



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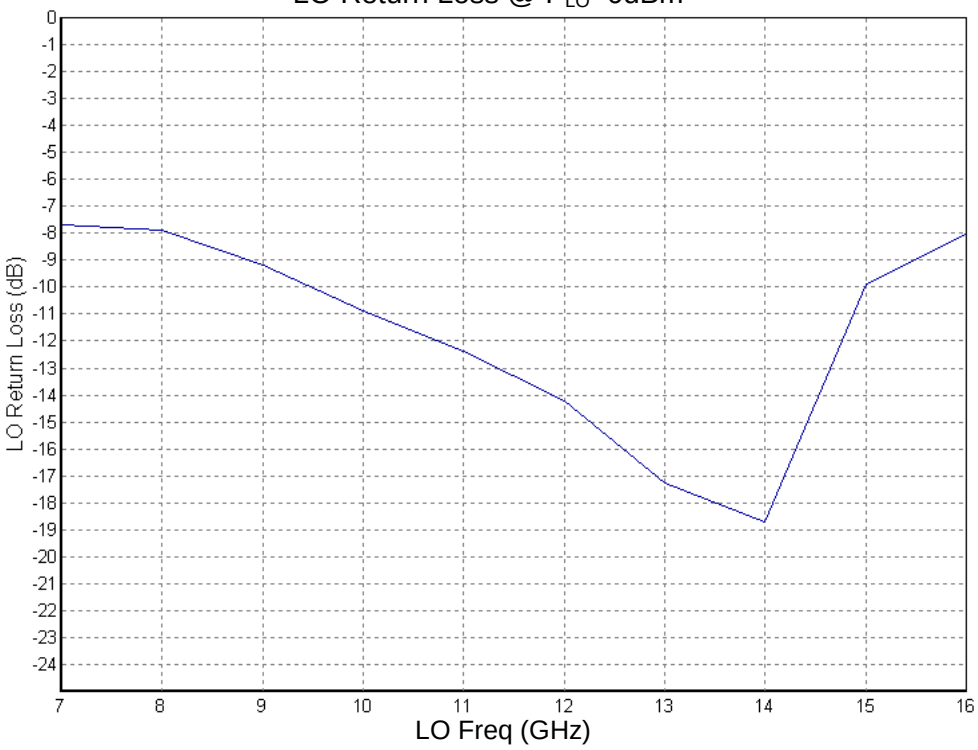
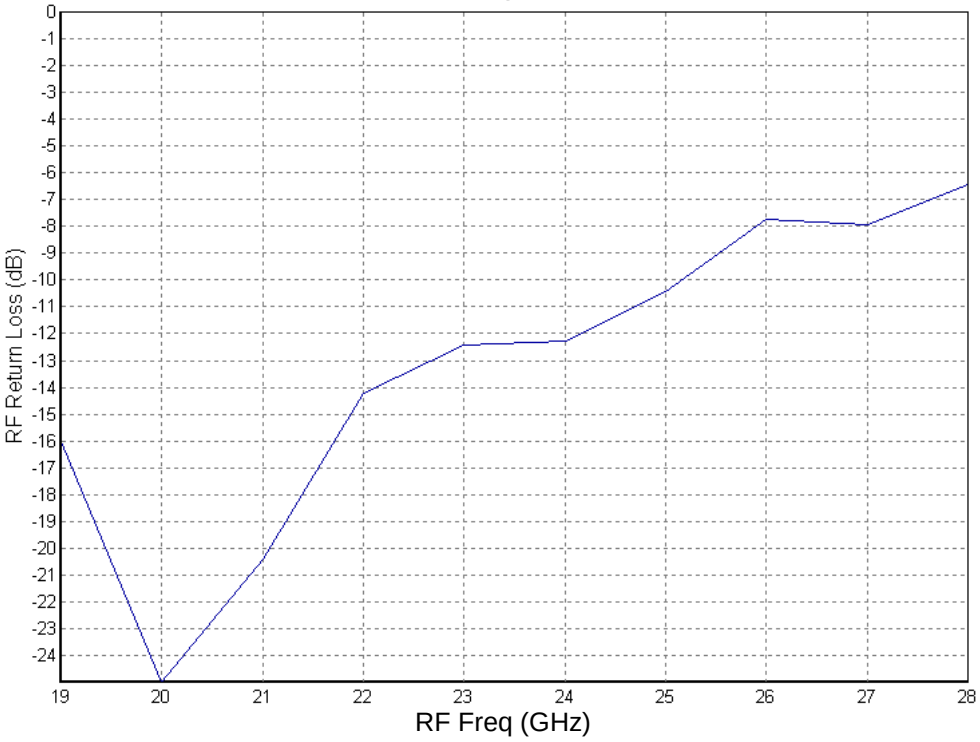
LO Return Loss @ P_{LO}=0dBm



RF Return Loss @ P_{RF}=-30dBm



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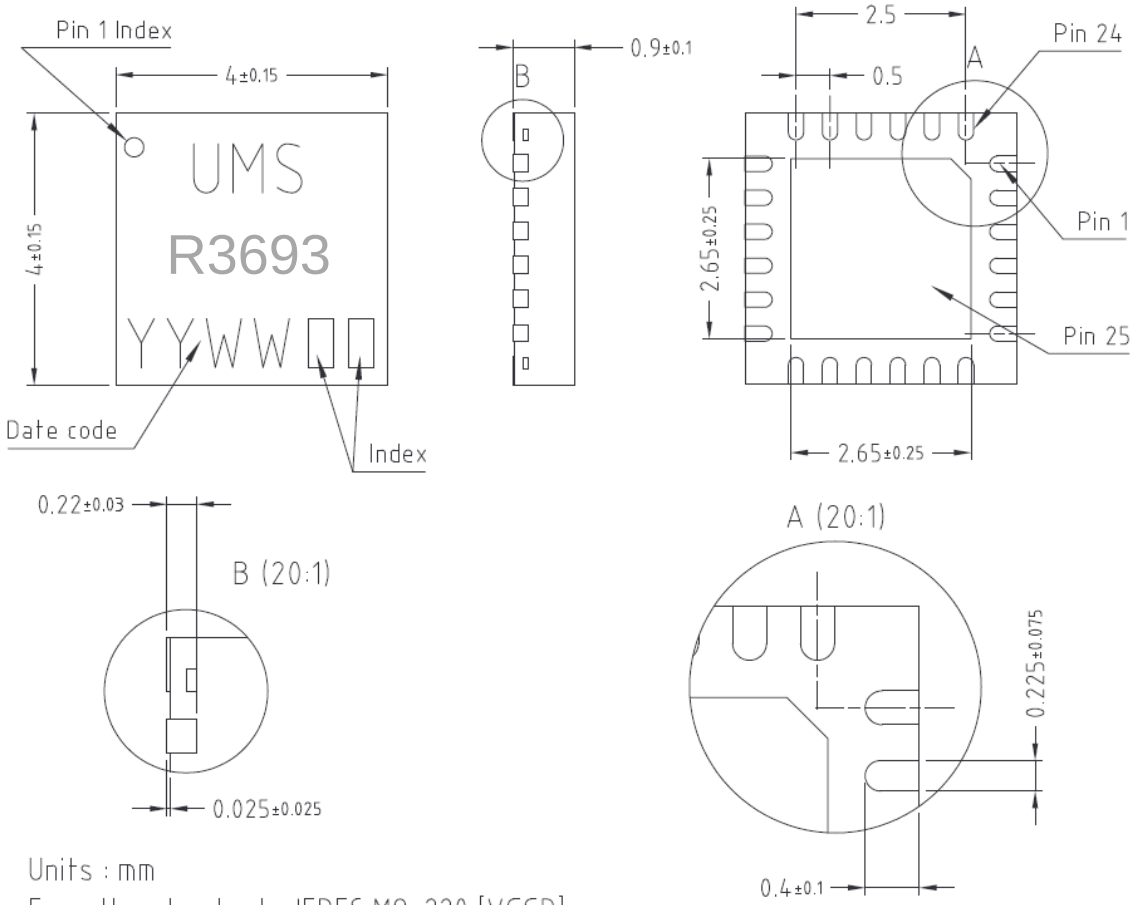
Package outline (1)



Matt tin, Lead Free	(Green)	1-	NC	13-	GND
Units	mm	2-	GND	14-	GND
From the standard	JEDEC MO-220	3-	GND	15-	LO IN
	(VGGD)	4-	RF IN	16-	GND
25- GND		5-	GND	17-	GND
		6-	GND	18-	NC
		7-	Vdl	19-	I-IF OUT
		8-	Vgm	20-	GND
		9-	Vdx	21-	GND
		10-	NC	22-	Q-IF OUT
		11-	NC	23-	NC
		12-	Vgx	24-	NC

(1) The package outline drawing included to this data-sheet is given for indication. Refere to the application note AN0017 available at http://www.ums-gaas.com for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “GND” through the PCB board.

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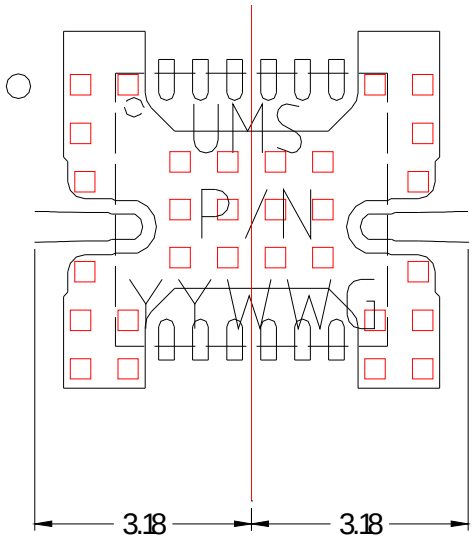
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Recommanded package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommandations.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

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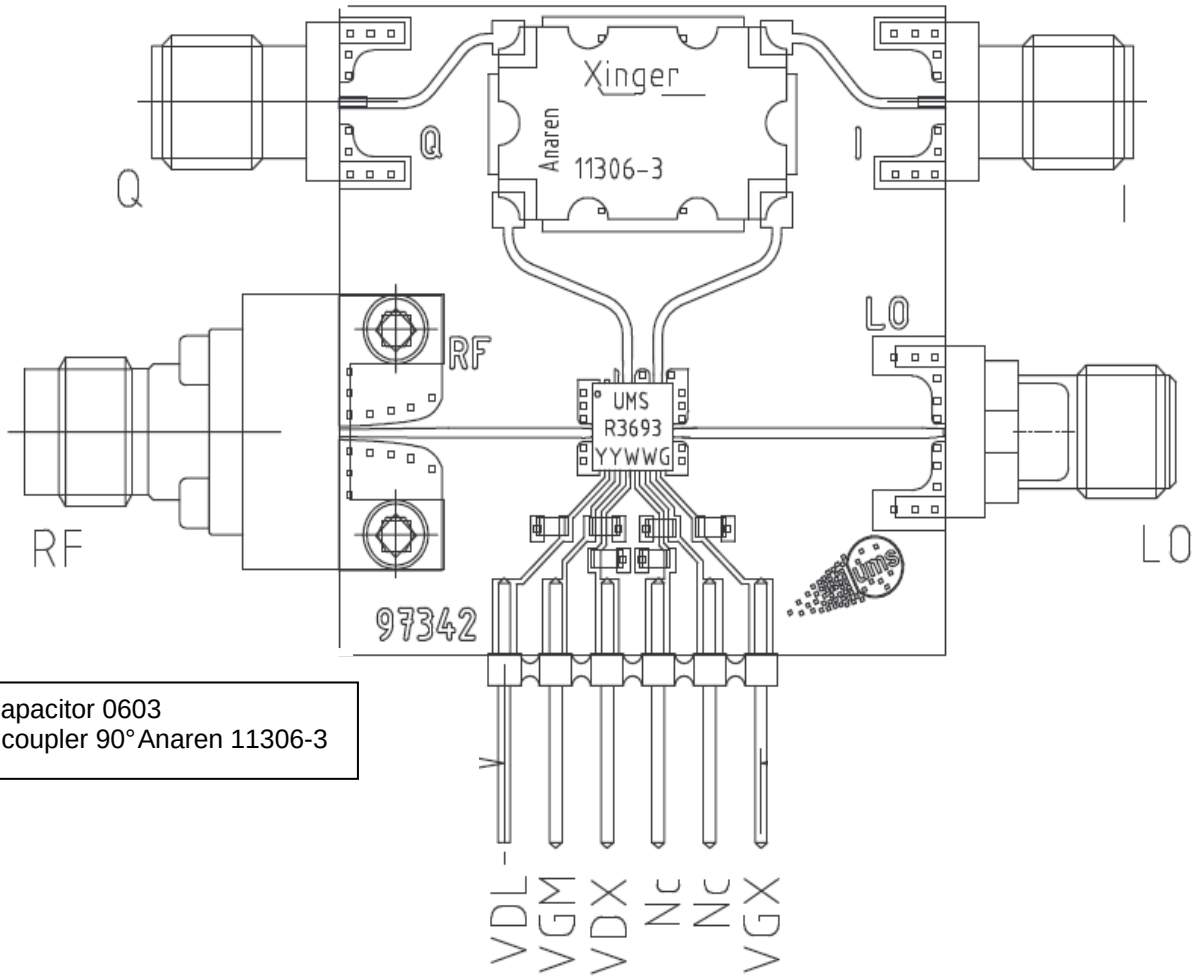
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- (See application note AN0017 for details).



10nF capacitor 0603
Hybric coupler 90° Anaren 11306-3

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

The SMD leadless package has been designed for high volume surface mount PCB assembly process. A typical footprint is proposed for the PCB (motherboard) in the previous drawing. For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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Ordering Information

QFN 4x4 RoHS compliant package: CHR3693-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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