6-9GHz Integrated Down Converter

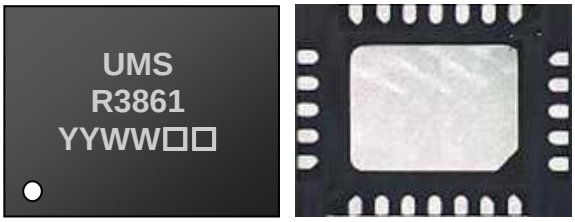
GaAs Monolithic Microwave IC in SMD package

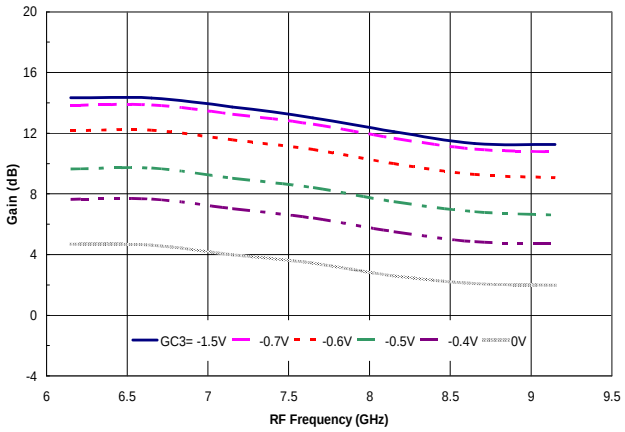
Description

The CHR3861-QEG is a multifunction part, which integrates a balanced cold FET mixer, a LO bufffer, and a RF LNA including gain control. It is designed for a wide range of applications, typically ISM and commercial communication systems.

The circuit is manufactured on a pHEMT process, 0.25µm gate length.

It is supplied in lead-free SMD package.





Main Features

- RF performance 5.9-9.0GHz
- 12dB conversion gain
- 1dBm Input IP3
- 9dB Gain Control
- 15dBc Image Rejection
- 24LQFN4x5
- ESD protected

Main Characteristics

Tamb = +25°C, Vd = 4V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	5.9		9.0	GHz
F_{LO}	LO frequency range	3.0		12.5	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G_c	Conversion gain		12		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Tamb = +25℃, VD = VD1 = 4V

Configuration 1: High linearity with GC4 fixed at 0V

Symbol	Parameter	Min	Typ	Max	Unit
FRF	RF frequency range	5.9		9.0	GHz
FLO	LO frequency range	3.0		12.5	GHz
FIF	IF frequency range	DC		3.5	GHz
Gc	Conversion gain@ min. attenuation (1)		12		dB
∆G	Gain control range with only Gc3		9		dB
NF	Noise Figure@ min. attenuation		2.5		dB
Im_rej	Image rejection (1)		15		dBc
PLO	LO Input power		0		dBm
IIP3	Input IP3@ at Gc max.		1		dBm
VD, VD1	DC drain voltage		4		V
Id	Total drain current at Gc max.		380		mA
VG	LNA DC gate voltage		-0.3		V
B	LO buffer & X2 DC voltage		-4		V
GC3	Gain control DC voltage	-1.5		0	V
GC4	Gain control DC voltage	0		0	V

(1) An external combiner 90°is required on I / Q.
These values are representative of on board measurements as defined on the drawing at paragraph “Evaluation mother board”.

Note: Id not affected by GC3, GC4.

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Configuration 2: High Gain & low Noise with GC3 = GC4

Symbol	Parameter	Min	Typ	Max	Unit
FRF	RF frequency range	5.9		9.0	GHz
FLO	LO frequency range	3.0		12.5	GHz
FIF	IF frequency range	DC		3.5	GHz
Gc	Conversion gain@ min. attenuation (1)		22		dB
∆G	Gain control range with Gc3=GC4		18		dB
NF	Noise Figure@ min. attenuation		2		dB
Im_rej	Image rejection (1)		15		dBc
PLO	LO Input power		0		dBm
IIP3	Input IP3@ at Gc max.		-6		dBm
VD, VD1	DC drain voltage		4		V
Id	Total drain current at Gc max.		380		mA
VG	LNA DC gate voltage		-0.3		V
B	LO buffer & Mixer DC voltage		-4		V
GC3, GC4	Gain control DC voltage	-1.5		0	V

(1) An external combiner 90°is required on I / Q.
These values are representative of on board measurements as defined on the drawing at paragraph “Evaluation mother board”.

Note: Id not affected by GC3, GC4.

Note: Electrostatic discharge sensitive device observe handling precautions!

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Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
VD, VD1	Maximum drain bias voltage	4.5	V
Id	Maximum drain bias current	450	mA
VG	LNA DC gate voltage	-2.0 to 0.4	V
B	Buffer & Mixer DC voltage	-5	V
GCx	Gain control voltage	-2 to 1	V
P_RF	Maximum peak input power overdrive	10	dBm
P_LO	Maximum LO input power	5	dBm
Tch	Maximum channel temperature (1)	175	℃
Ta	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (convection mode not considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

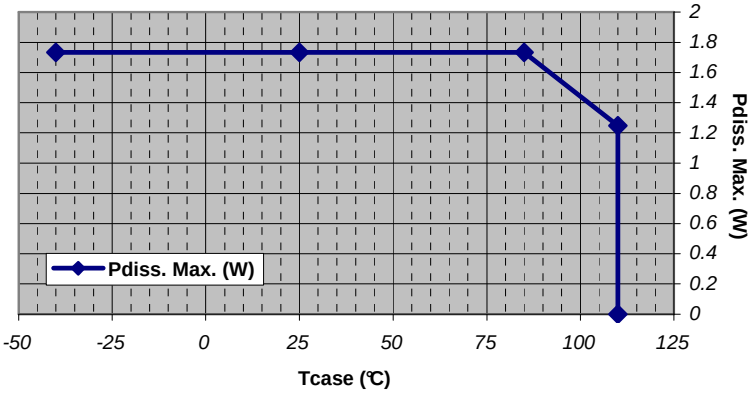
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified in order to guarantee the nominal device life time (MTTF) (see the curve Pdiss. Max below).

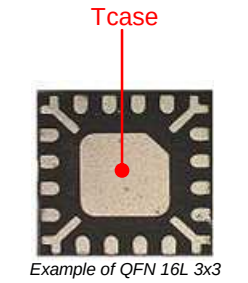
DEVICE THERMAL SPECIFICATION : Product name				
Recommended max. junction temperature (Tj max)			:	174 °C
Junction temperature absolute maximum rating			:	175 °C
Max. continuous dissipated power @ Tcase=	85	°C	:	1.7 W
=> Pdiss derating above Tcase(1)=	85	°C	:	19 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)			:	<51 °C/W
Minimum Tcase operating temperature(3)			:	-40 °C
Maximum Tcase operating temperature(3)			:	85 °C
Absolute maximum rating Tcase temperature(3)			:	110 °C
Minimum storage temperature			:	-55 °C
Maximum storage temperature			:	125 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hottest junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example of QFN 16L 3x3 back-side view, temperature reference point (Tcase) location.

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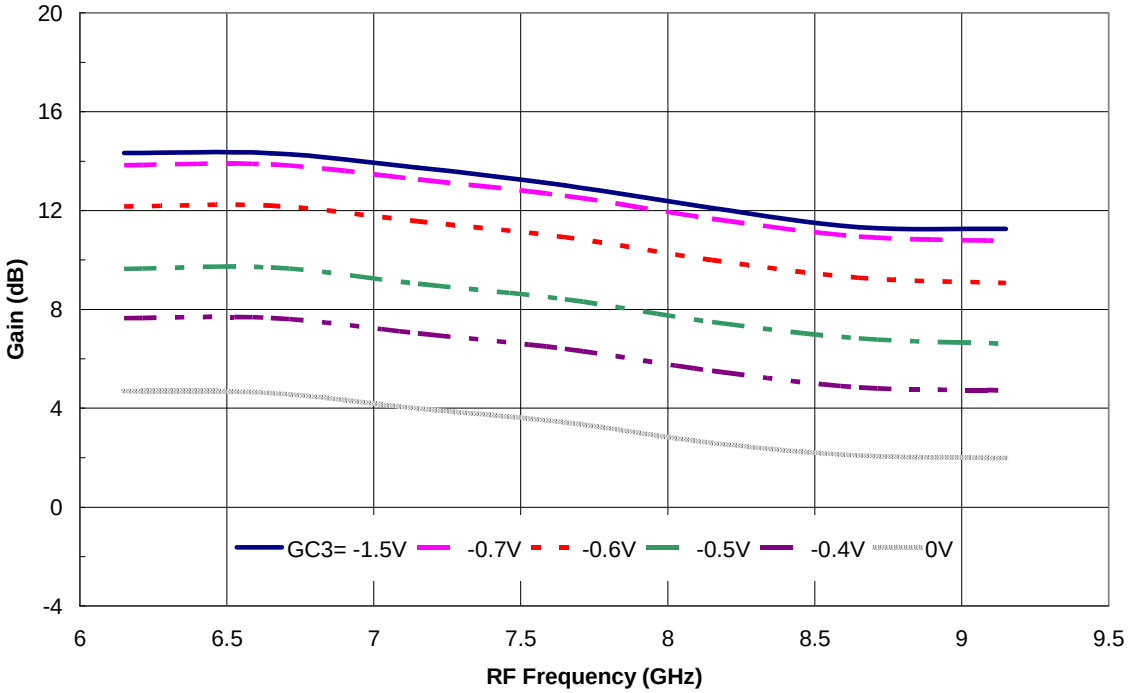
Typical Measured Performances

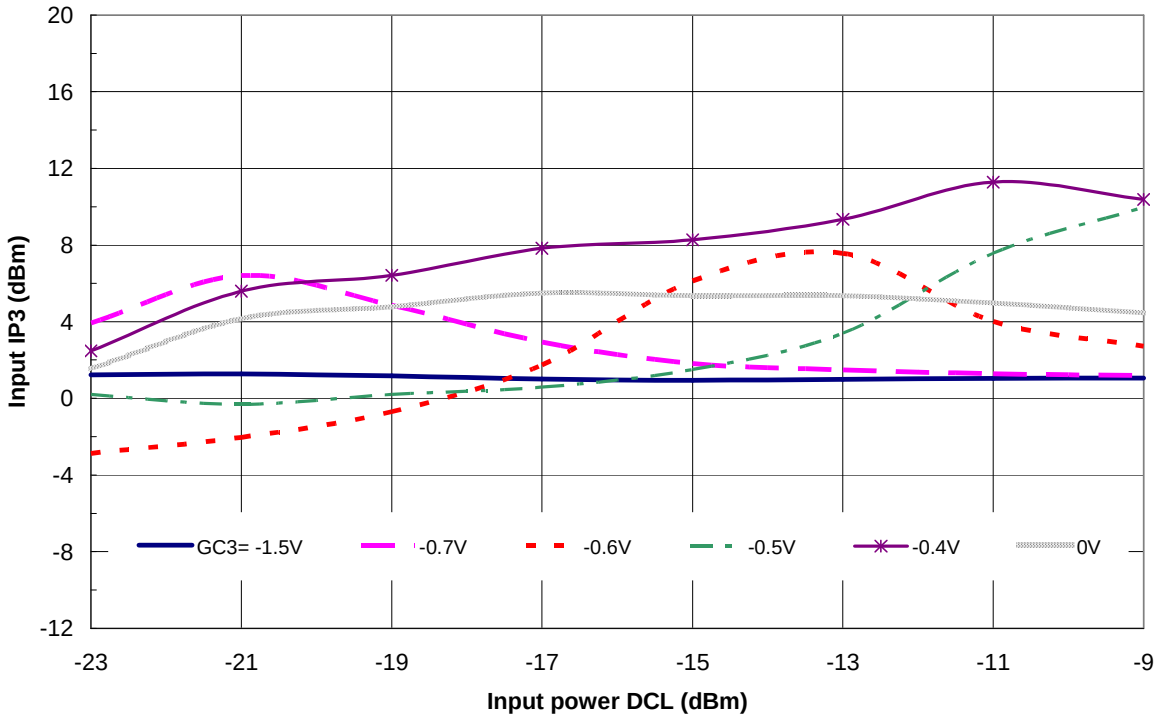
Tamb = +25℃, VD = VD1 = 4V, VG = -0.3V, B = -4V, P _LO = 0dBm
If no specific mention, the following values are representative of onboard measurements (on connector access planes) as defined on the drawing at paragrah “Evaluation mother board”. The board losses are estimated from 0.5 to 0.7dB in the frequency range.

Configuration 1: High linearity

Gain versus GC3 with GC4 = 0V



Input IP3 versus GC3 at RF = 6.2GHz & GC4 = 0V



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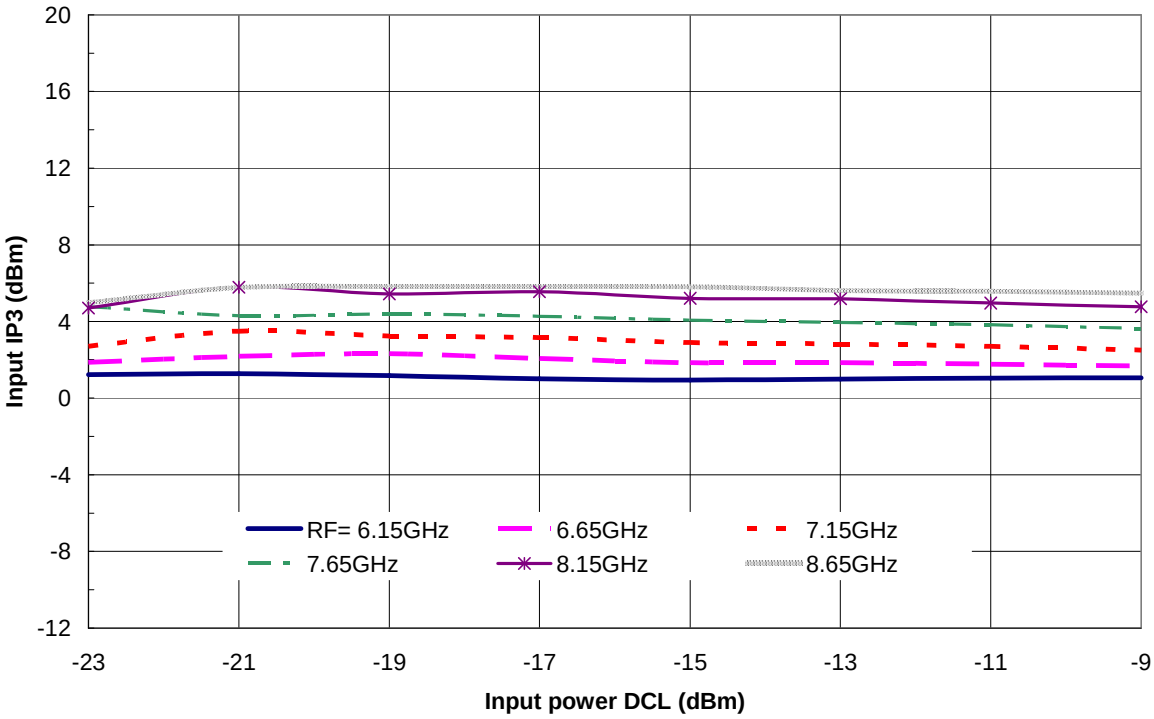
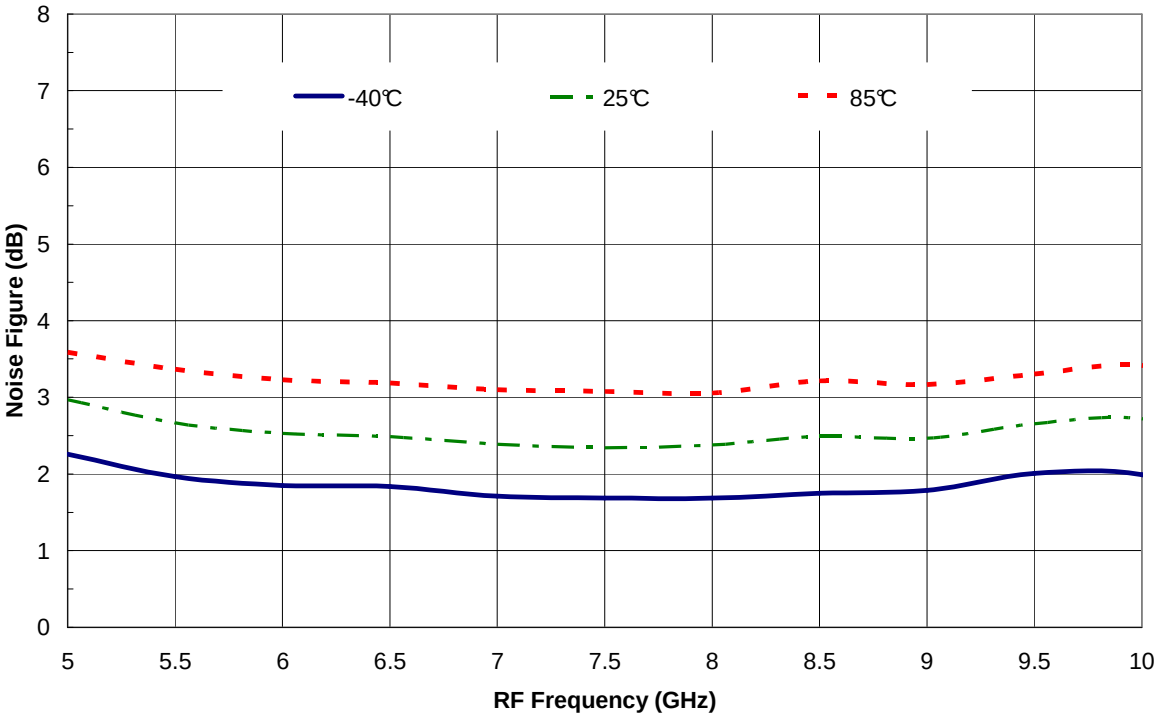
Input IP3 versus RF frequency at GC3 = -1.5V & GC4 = 0V



Noise figure versus temperature with GC3 = -1.5V, GC4 = 0V & IF = 1.4GHz



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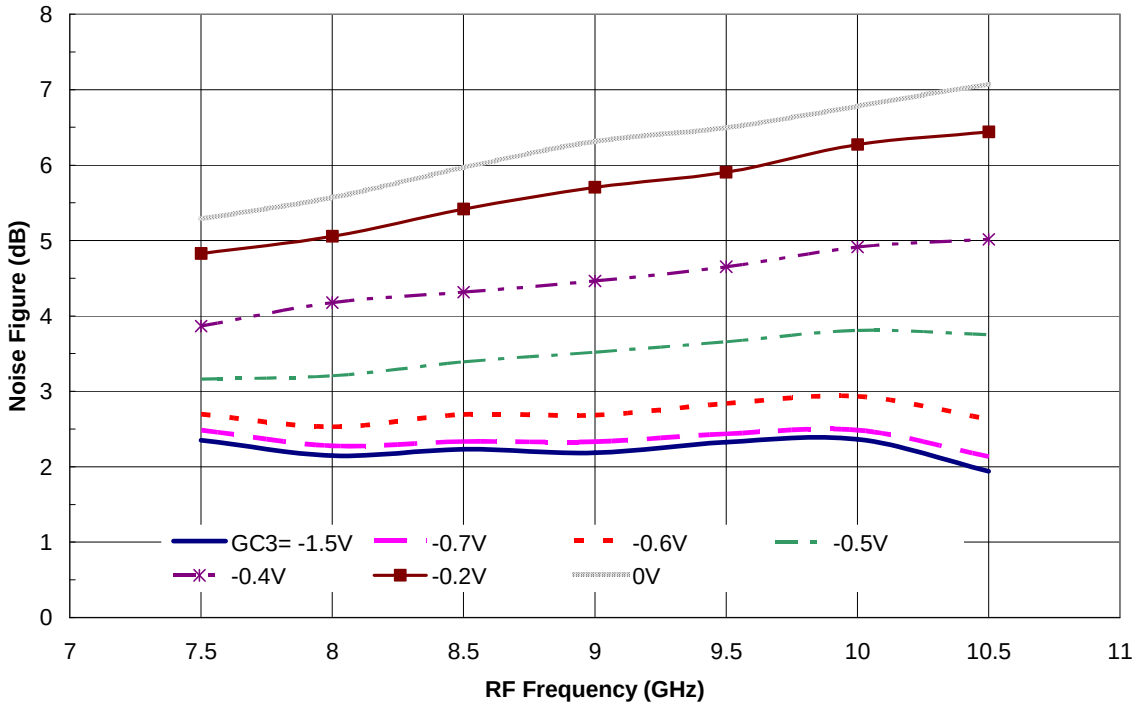
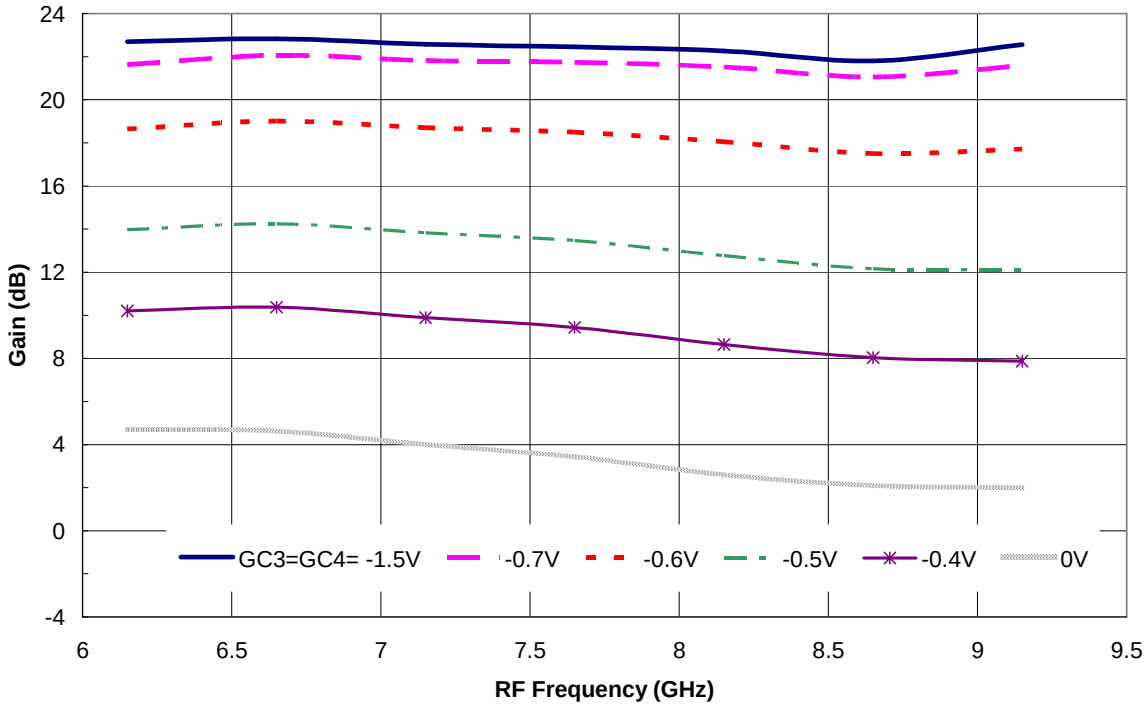
Noise figure versus GC3 with GC4 = 0V at 25℃ & IF = 1.4GHz



Configuration 2: High Gain & High dynamic

Gain versus GC3 = GC4



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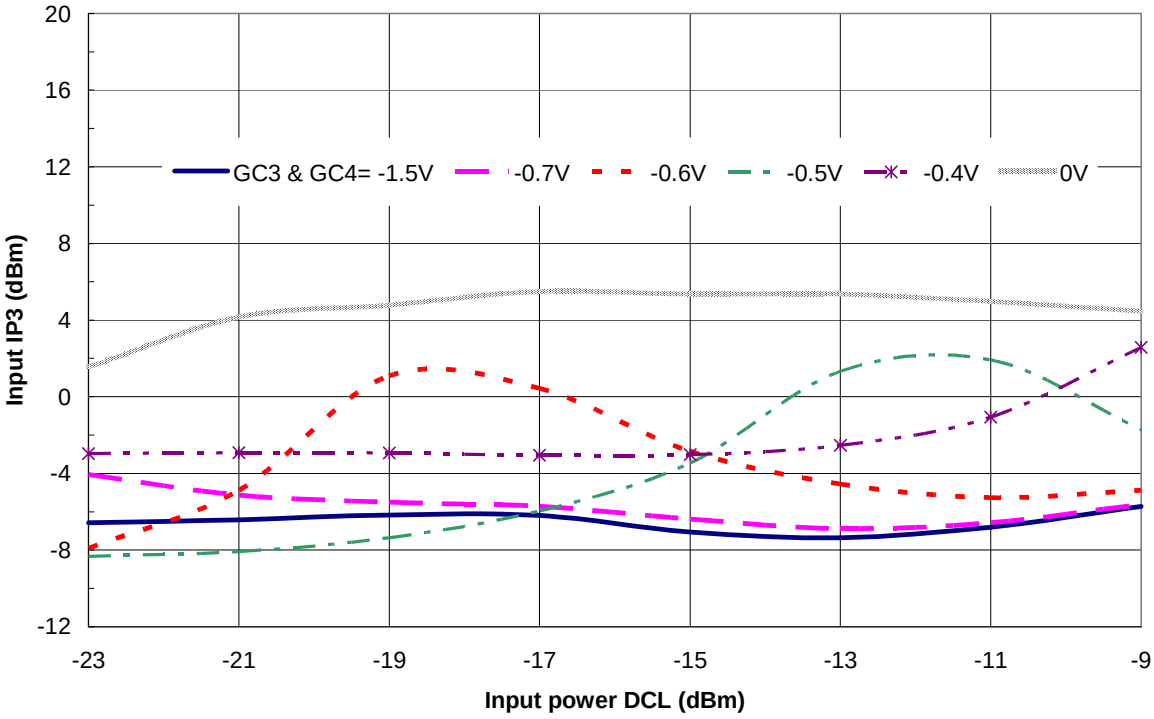
Input IP3 at RF=6.2GHz with GC3 = GC4



Noise figure versus temperature with GC3 = GC4 at max. Gain & IF = 1.4GHz

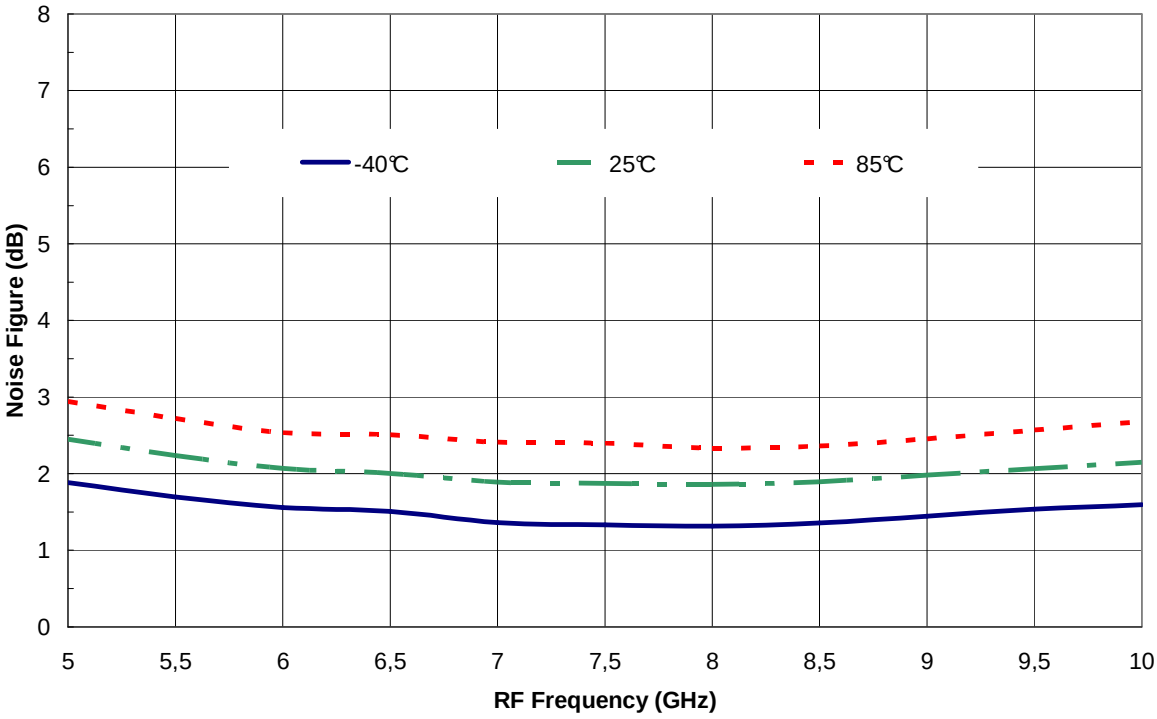


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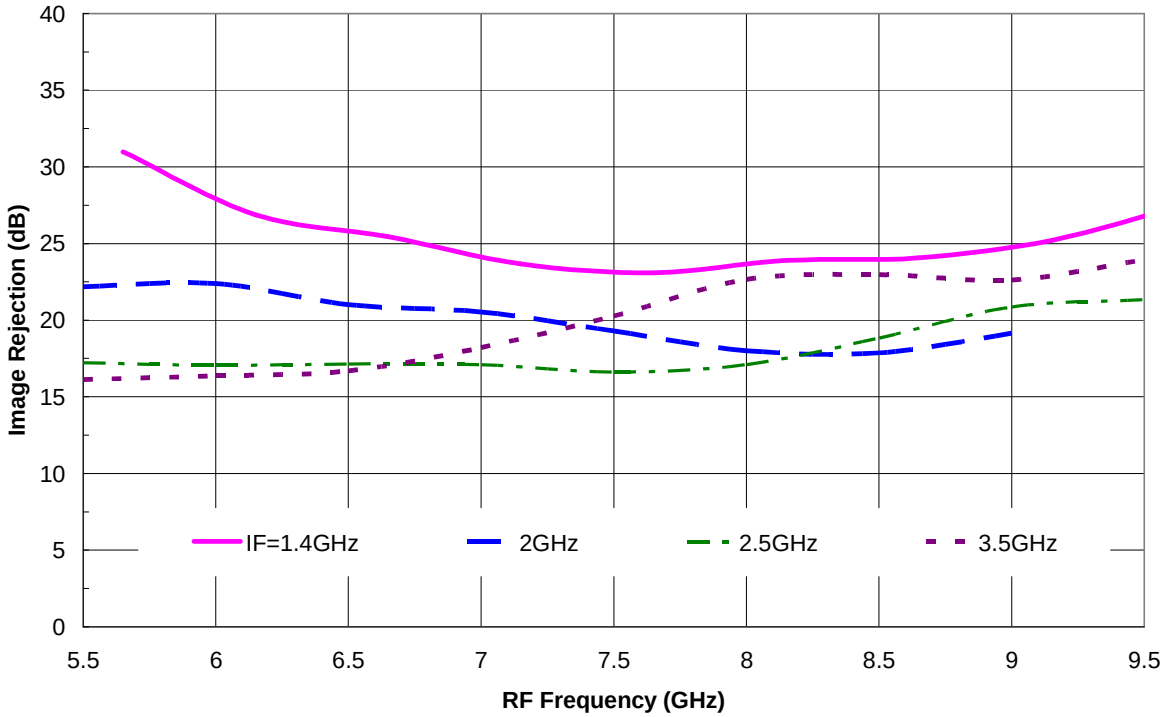
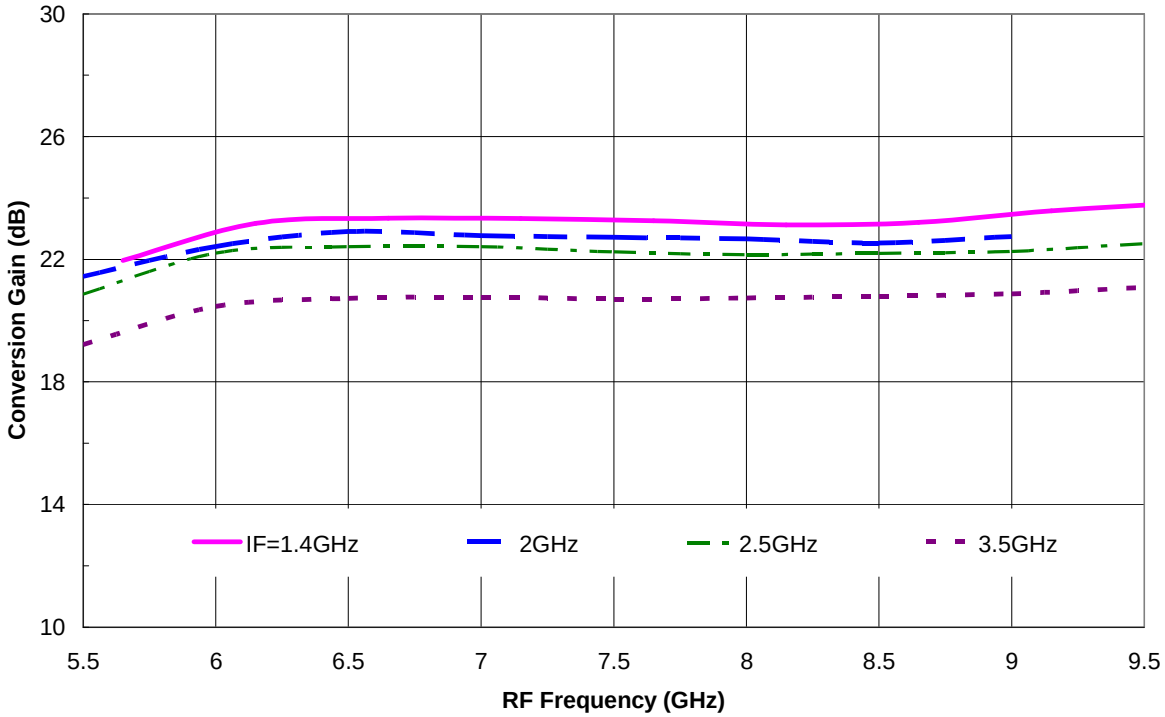
Image rejection versus IF with GC3 = GC4 at max. Gain



Conversion Gain versus IF with GC3 = GC4 at max. Gain

RF = LO - IF



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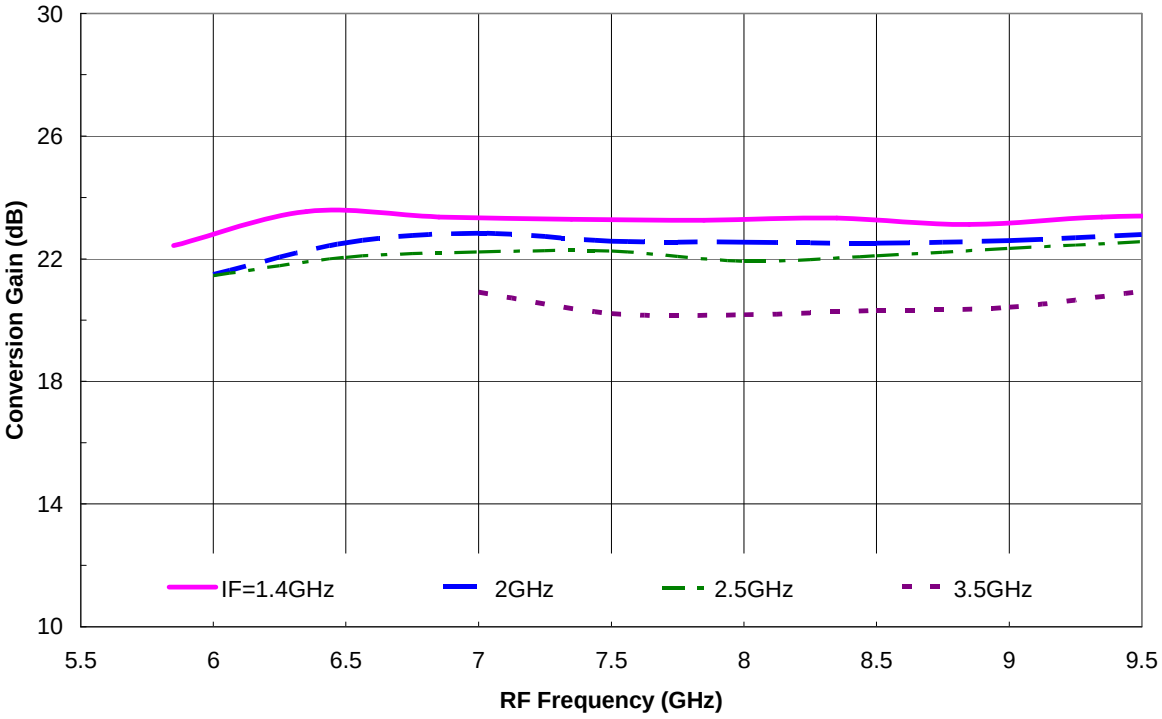
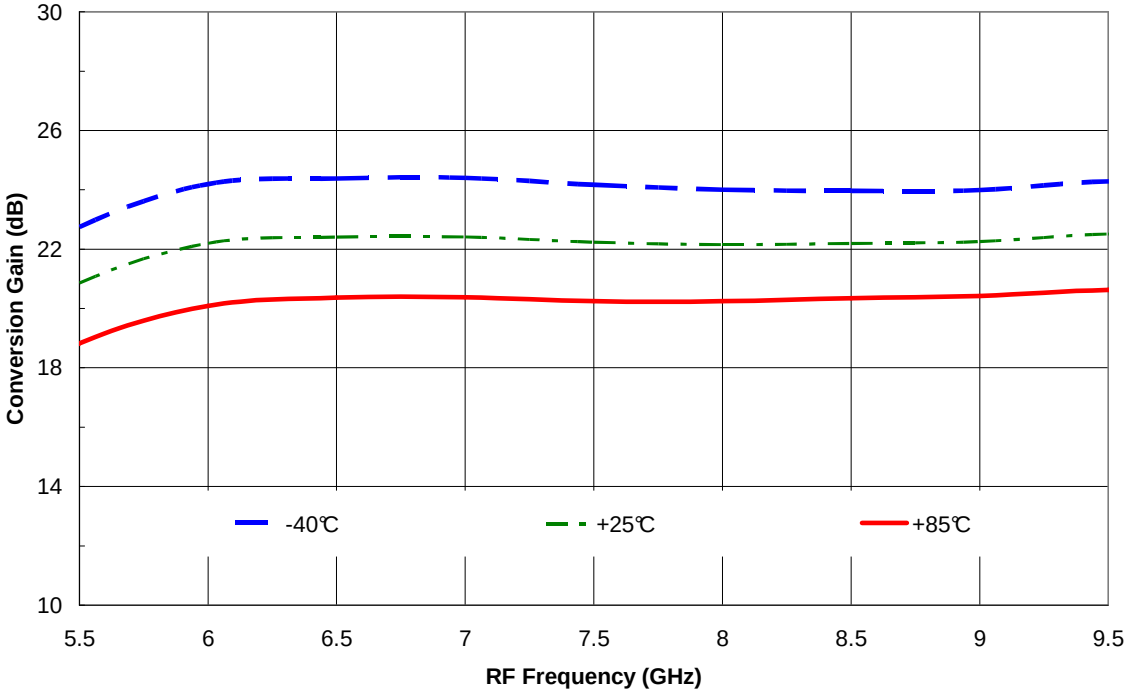
Conversion Gain versus IF with GC3 = GC4 at max. Gain
RF = LO + IF



Conversion Gain versus temperature at max. Gain
RF = LO - IF



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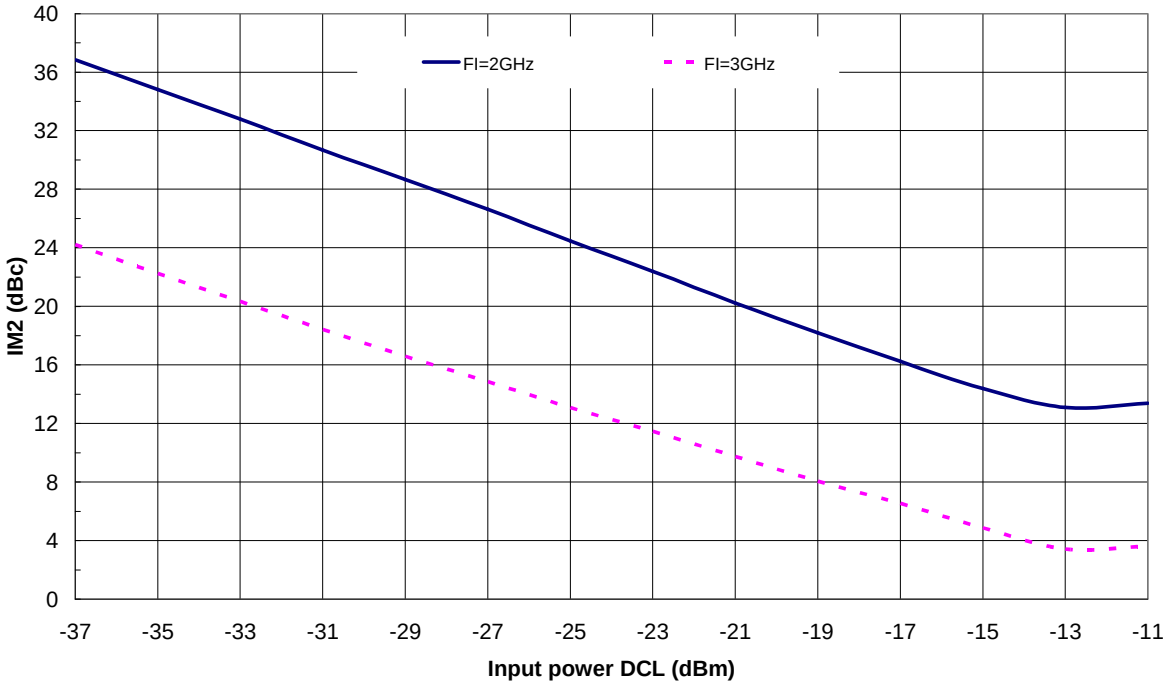
2nd order intermodulation
RF = LO + IF
F_RF = 7.5 GHz



Spurious on IF outputs
RF = LO + IF
P_RF = -30dBm @7GHz / P_LO = 0dBm @6GHz

	nLO				
mRF	0	1	2	3	4
0	xx	6	26	33	30
1	10	0	24	40	48
2	60	56	28	38	75
3	66	80	70	58	58
4	68	56	80	75	38

All values in dBc below IF power level (IF = 1GHz).
Data measured without external hybrid coupler.

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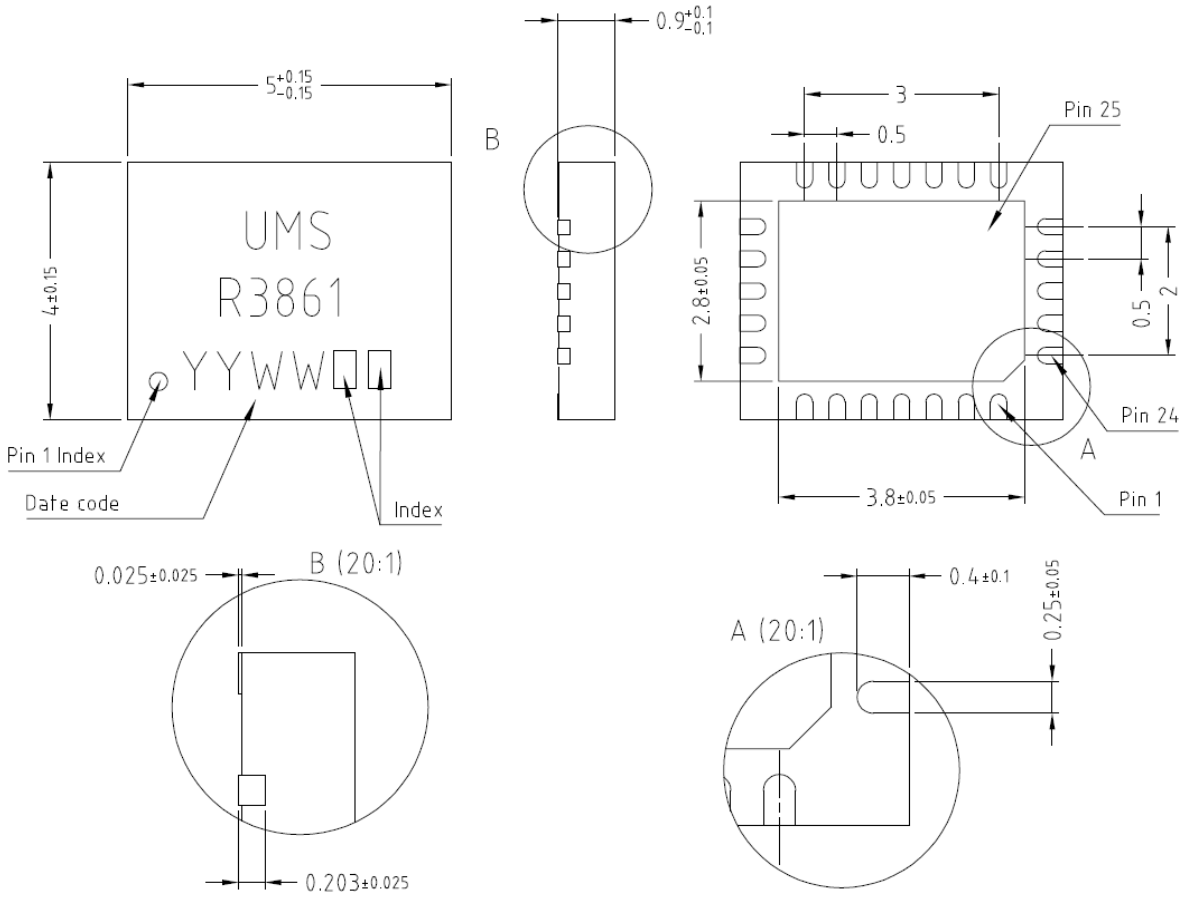
Package outline (1)



Units : mm
From the standard : JEDEC MO-220 [VGHD]
Matt tin, Lead free (Green)

1- Nc	9- VG	17- Nc	25- GND Exposed pad
2- Nc	10- VD1	18- Nc	
3- Nc	11- VD	19- Nc	
4- GND(2)	12- B	20- IF_I out	
5- RF in	13- Nc	21- GND(2)	
6- Nc	14- Nc	22- IF_Q out	
7- GC4	15- LO in	23- Nc	
8- GC3	16- GND(2)	24- Nc	

(1) The package outline drawing included to this data-sheet is given for indication. Refere to the application note AN0017 available at http://www.ums-gaas.com for exact package dimensions.

(2) It is strongly recommended to ground on the PCB board all the pins referenced as GND.

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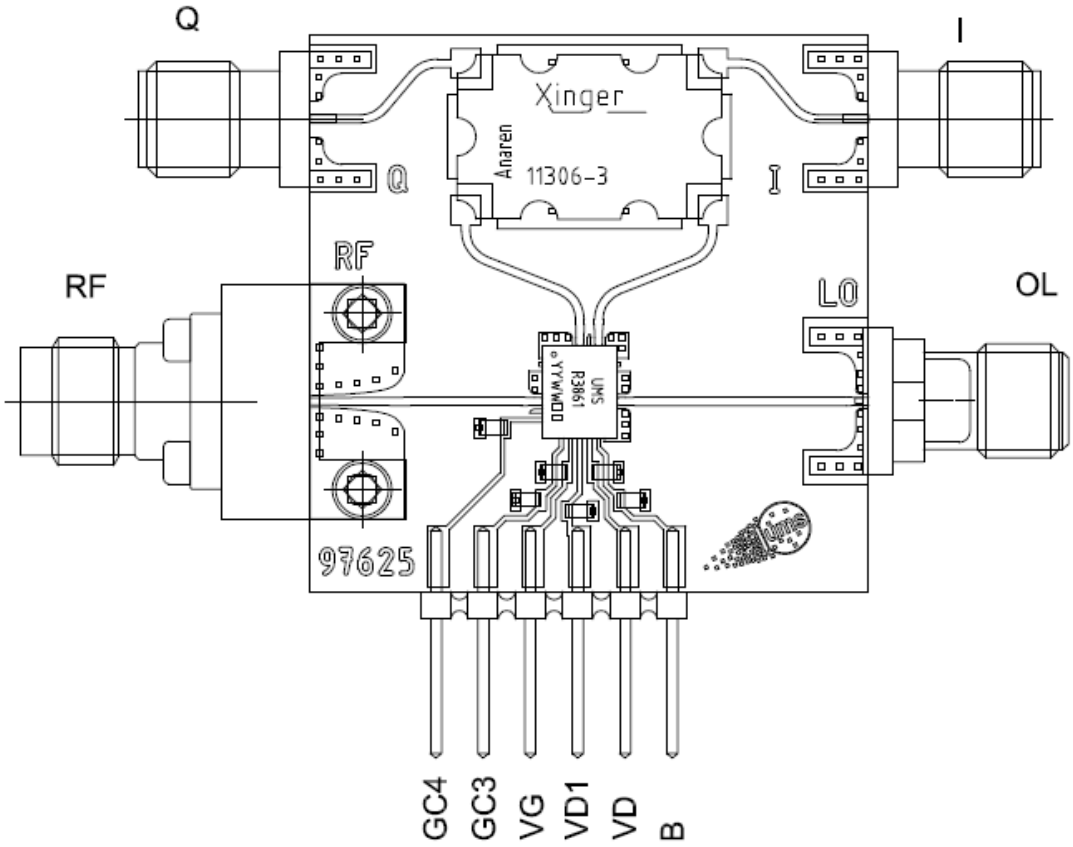
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- (See application note AN0017 for details).



Decoupling Capacitors = 10nF
Hybrid coupler Anaren 90°2-4GHz

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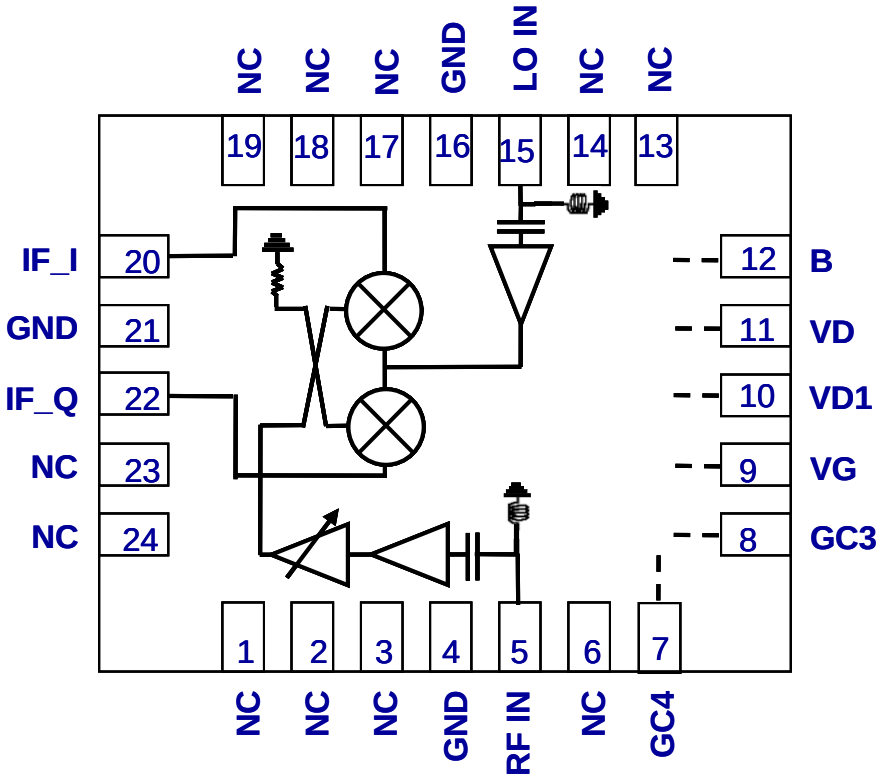
Notes

Due to ESD protection circuits on RF and LO inputs, an external capacitance might be requested to isolate the product from external voltage that could be present on these accesses in the application.



ESD protections are also implemented on gate accesses.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

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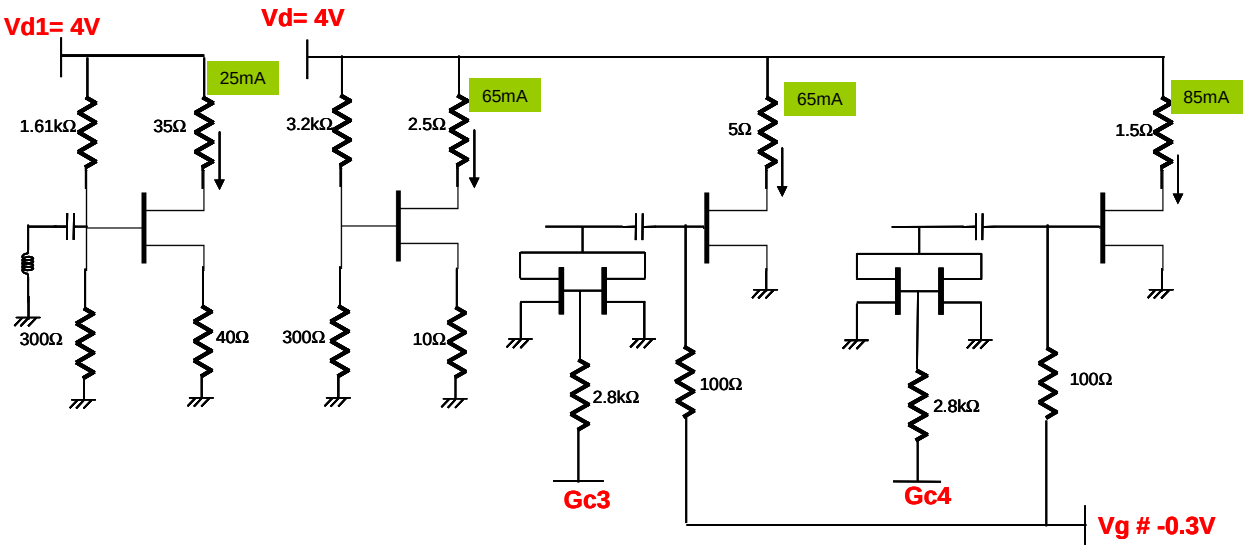
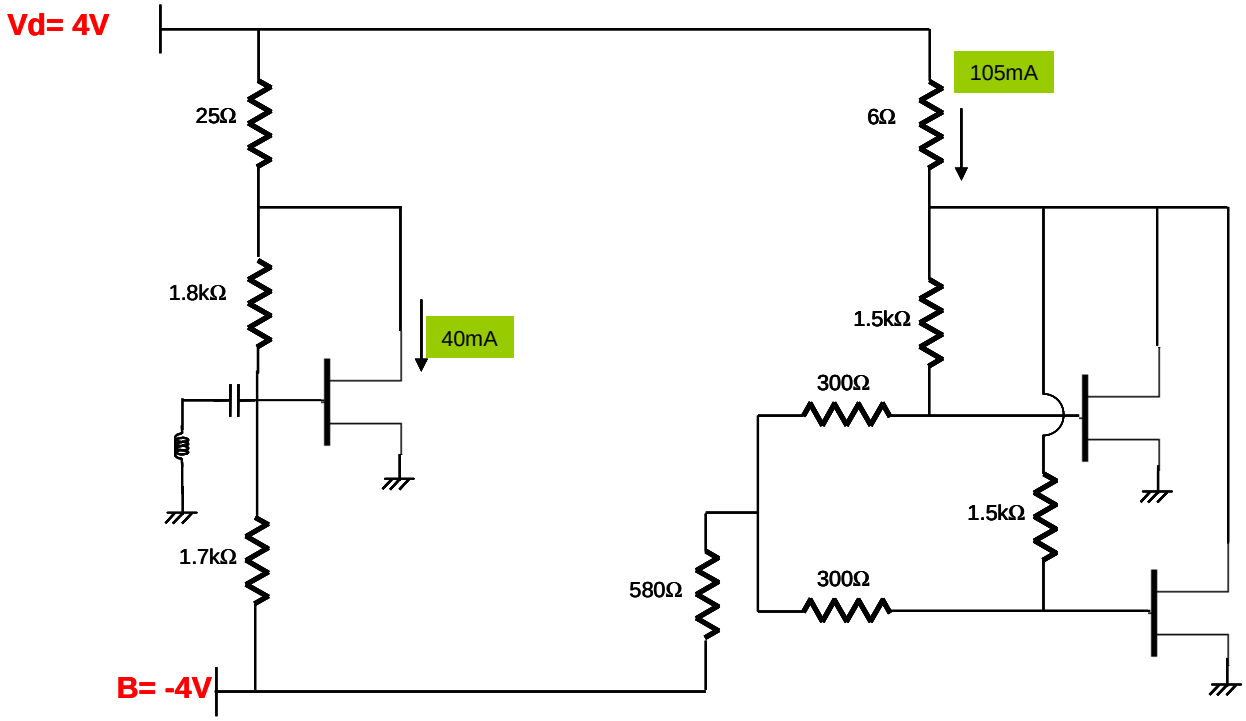
DC Schematic

LNA: 4V, 240mA



LO Buffer: 4V, 140mA



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Notes

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 RoHS compliant package: CHR3861-QEG/XY
Stick: XY = 20 Tape & reel: XY = 21

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