

UltraCMOS® RF Digital Attenuator 2-bit, 18 dB, 35–6000 MHz

Product Description

The PE43205 is a 50Ω, HaRP™ technology-enhanced fast switching 2-bit RF Digital Step Attenuator (DSA) designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

This DSA is a pin-compatible upgraded version of the PE43204 with a wider frequency and power supply range, and extended operating temperature range.

Covering an 18 dB attenuation range in 6 dB and 12 dB steps, it maintains high RF performance and low power consumption from 35 MHz through 6 GHz. PE43205 is offered in a 12-lead 3x3 mm QFN package. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE43205 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- Attenuation: 6 dB / 12 dB steps to 18 dB
- Fast switching time of 29 ns
- Low attenuation error
 - 0.10 dB @ 2 GHz
 - 0.15 dB @ 3 GHz
- High linearity
 - +61 dBm IIP3 @ 1950 MHz
- Wide supply range of 2.3V to 5.5V
- 1.8V control logic compatible
- 105°C operating temperature
- ESD performance
 - 2 kV HBM on all pins
 - 100V MM on all pins
 - 1 kV CDM on all pins
- Parallel control

Figure 1. Functional Diagram

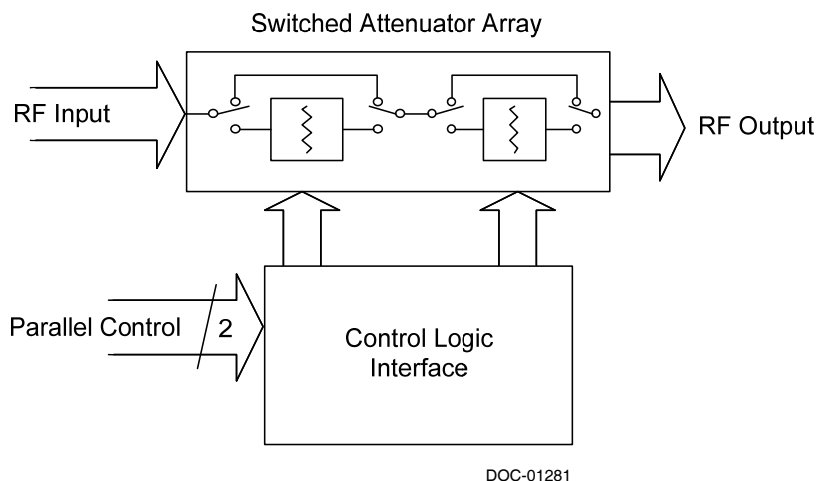


Figure 2. Package Type
12-lead 3x3 mm QFN

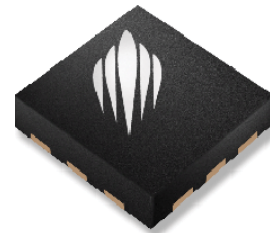


Table 1. Electrical Specifications @ +25°C, V_{DD} = 2.3V to 5.5V

Parameter	Condition	Min	Typ	Max	Unit
Frequency range		35		6000	MHz
Attenuation range	6 dB and 12 dB steps		0–18		dB
Insertion loss	35 MHz–2 GHz		0.50	0.60	dB
	2–3 GHz		0.60	0.70	dB
	3–4 GHz		0.70	0.80	dB
	4–5 GHz		0.85	1.10	dB
	5–6 GHz		1.05	1.30	dB
Attenuation error	0 dB–18 dB attenuation settings				
	35 MHz–2 GHz	–0.25	0.10	0.40	dB
	>2–3 GHz	–0.20	0.15	0.50	dB
	>3–4 GHz	–0.15	0.45	1.05	dB
	>4–5 GHz	–0.15	0.55	1.25	dB
	>5–6 GHz	–0.30	0.75	1.55	dB
Return loss	35 MHz–2 GHz		17		dB
	2–3 GHz		14		dB
	3–4 GHz		11		dB
	4–5 GHz		10		dB
	5–6 GHz		9		dB
Relative phase	All states				
	35 MHz–2 GHz		9		deg
	2–3 GHz		12		deg
	3–4 GHz		17		deg
	4–5 GHz		22		deg
	5–6 GHz		24		deg
Input 0.1dB compression point *	200 MHz–6 GHz		30		dBm
IIP3	1950 MHz		61		dBm
Switching time	50% DC CTRL to 90% or 10% RF		29		ns

Note: * Input 0.1 dB compression point is a linearity figure of merit. Refer to *Table 3* for operating RF input power (50Ω).

Table 1A. Electrical Specifications @ +105°C, $V_{DD} = 2.3V$ to 5.5V

Parameter	Condition	Min	Typ	Max	Unit
Frequency range		35		6000	MHz
Attenuation range	6 dB and 12 dB steps		0–18		dB
Insertion loss	35 MHz–2 GHz		0.60	0.70	dB
	2–3 GHz		0.65	0.80	dB
	3–4 GHz		0.80	0.90	dB
	4–5 GHz		0.95	1.20	dB
	5–6 GHz		1.15	1.45	dB
Attenuation error	0 dB–18 dB attenuation settings				
	35 MHz–2 GHz	–0.35	–0.03	0.25	dB
	>2–3 GHz	–0.45	–0.10	0.30	dB
	>3–4 GHz	–0.45	–0.15	0.65	dB
	>4–5 GHz	–0.35	0.25	0.85	dB
	>5–6 GHz	–0.45	0.40	1.15	dB
Return loss	35 MHz–2 GHz		18		dB
	2–3 GHz		15		dB
	3–4 GHz		11		dB
	4–5 GHz		10		dB
	5–6 GHz		9.5		dB
Relative phase	All states				
	35 MHz–2 GHz		9		deg
	2–3 GHz		13		deg
	3–4 GHz		17		deg
	4–5 GHz		23		deg
	5–6 GHz		25		deg
Input 0.1dB compression point *	200 MHz–6 GHz		30		dBm
IIP3	1950 MHz		63		dBm
Switching time	50% DC CTRL to 90% or 10% RF		31		ns

Note: * Input 0.1 dB compression point is a linearity figure of merit. Refer to *Table 3* for operating RF input power (50Ω).

Figure 3. Pin Configuration (Top View)

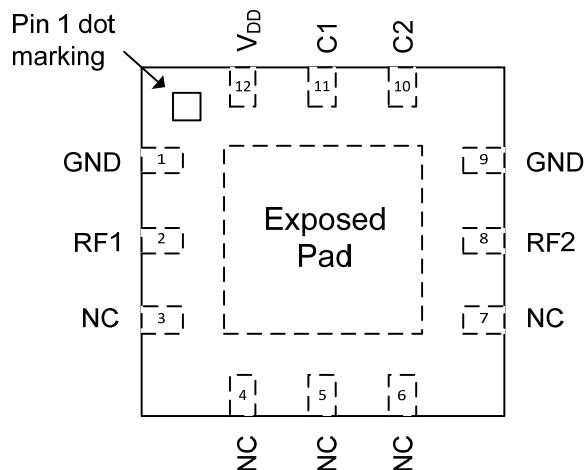


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	GND	Ground
2	RF1 ²	RF1 port
3	NC ¹	No connect
4	NC ¹	No connect
5	NC ¹	No connect
6	NC ¹	No connect
7	NC ¹	No connect
8	RF2 ²	RF2 port
9	GND	Ground
10	C2	Attenuation control bit, 12 dB
11	C1	Attenuation control bit, 6 dB
12	V _{DD}	Supply voltage (nominal 3.3V)

Notes: 1. Pins 3 through 7 may be tied to ground if desired, but they are not connected to ground internal to the package.
2. RF pins 2 and 8 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DD}	2.3		5.5	V
Supply current	I _{DD}		130	200	μA
Digital input high	V _{IH}	1.17		3.6	V
Digital Input Low	V _{IL}	-0.3		0.6	V
Digital input leakage				10	μA
RF input power, CW 35 MHz–4 GHz >4 GHz–6 GHz	P _{MAX,CW}			See Fig. 4 +24	dBm dBm
RF input power, pulsed * 35 MHz–4 GHz >4 GHz–6 GHz	P _{MAX,PULSED}			See Fig. 4 +27	dBm dBm
Operating temperature range	T _{OP}	-40	+25	+105	°C

Note: * Pulsed, 5% duty cycle of 4620 μs period, 50Ω

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V _{DD}	-0.3	5.5	V
Voltage on any digital input	V _I	-0.3	3.6	V
Storage temperature range	T _{ST}	-65	+150	°C
Maximum input power	P _{MAX,ABS}		+27.5	dBm
ESD voltage HBM ¹ , on all pins	V _{ESD,HBM}		2000	V
ESD voltage MM ² , on all pins	V _{ESD,MM}		100	V
ESD voltage CDM ³ , on all pins	V _{ESD,CDM}		1000	V

Notes: 1. Human Body Model (MIL-STD 883 Method 3015.7)
2. Machine Model (JEDEC JESD22-A115)
3. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Switching Frequency

The PE43205 has a maximum 25 kHz switching rate. Switching rate is defined to be the speed at which the DSA can be toggled across attenuation states. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spurious Performance

The typical low-frequency spurious performance of the PE43205 is -135 dBm.

Table 5. Attenuation Word Truth Table

C1	C2	Attenuation Setting RF1–RF2
L	L	Reference I.L.
H	L	6 dB
L	H	12 dB
H	H	18 dB

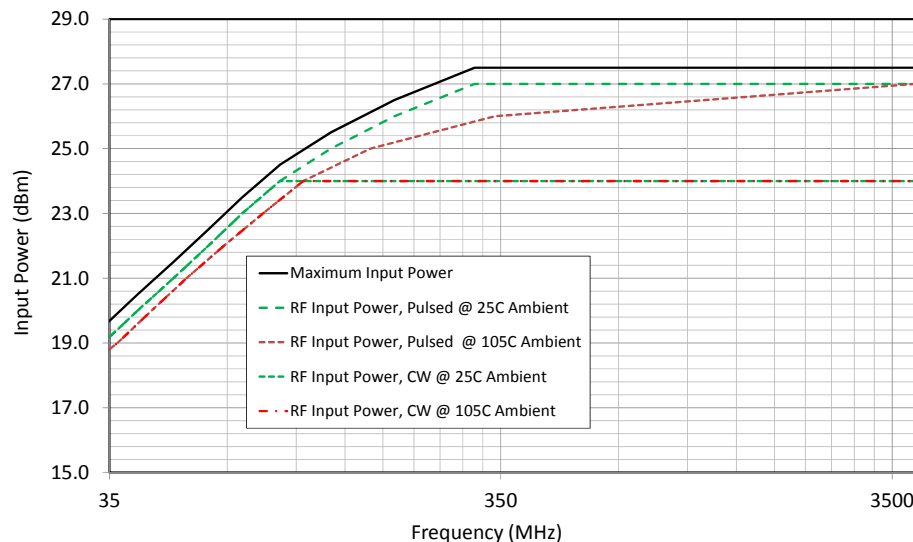
Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE43205 in the 12-lead 3x3 mm QFN package is MSL1.

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Figure 4. Power De-Rating Curve for 35 MHz–4 GHz



Typical Performance Data @ +25°C and $V_{DD} = 3.3V$, unless otherwise specified

Figure 5. Attenuation vs. Attenuation Setting

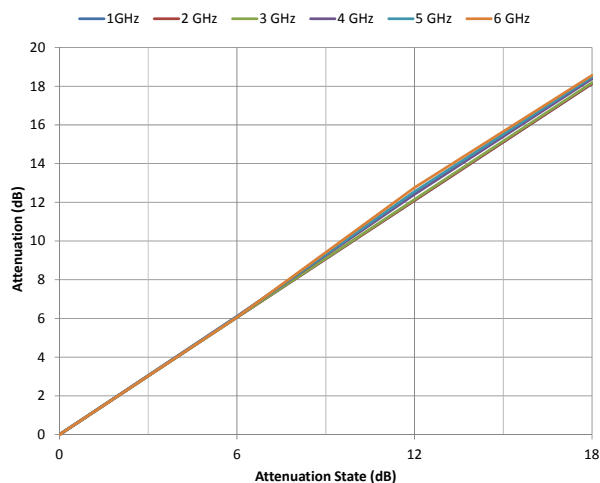


Figure 6. Attenuation Error vs. Frequency

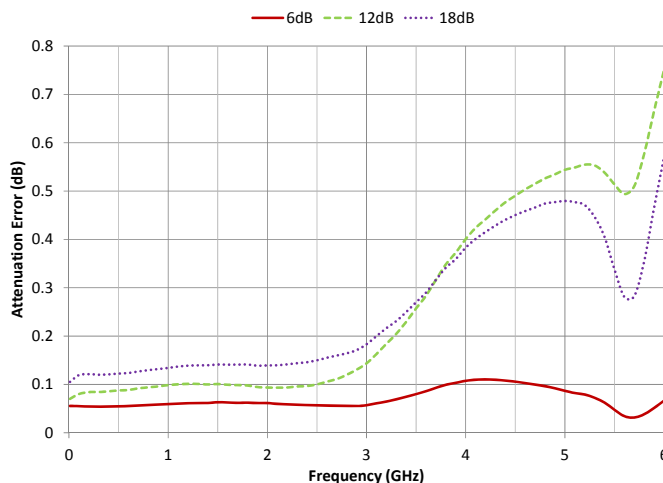


Figure 7. Insertion Loss vs. Temperature

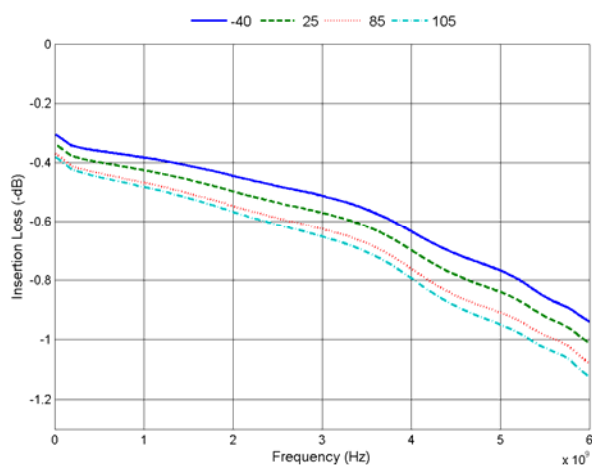


Figure 8. Input Return Loss vs. Attenuation State

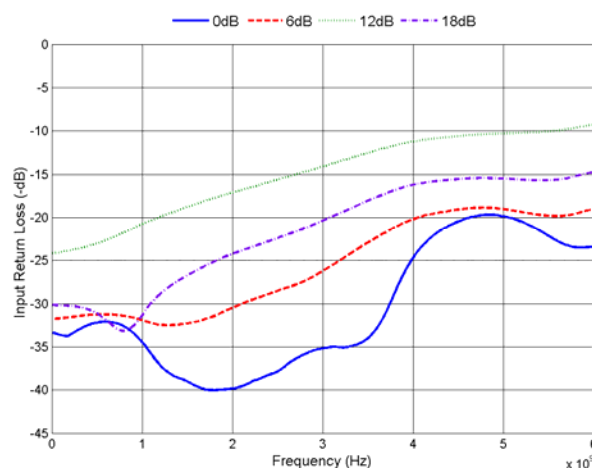


Figure 9. Output Return Loss vs. Attenuation State

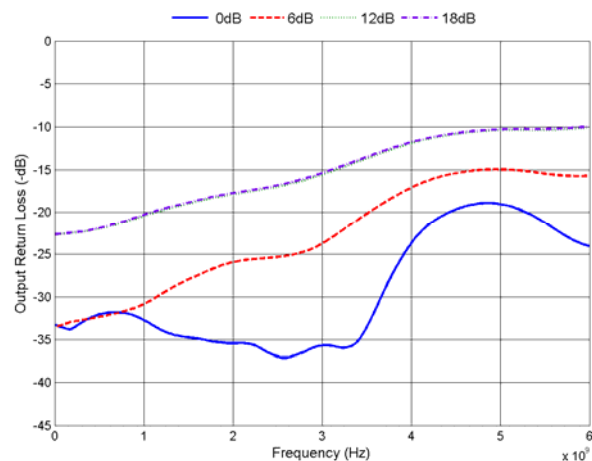
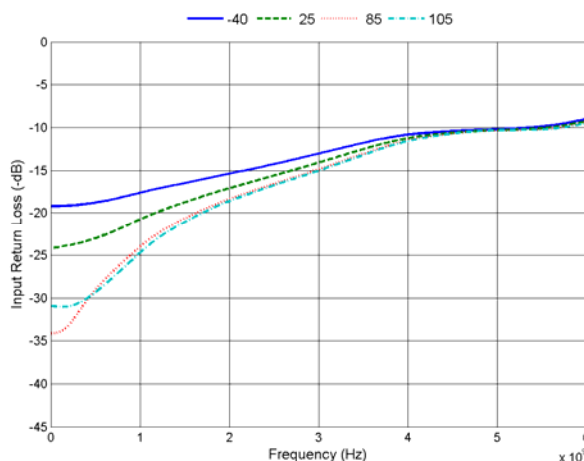


Figure 10. Input Return Loss vs. Temperature @ 12 dB State



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, unless otherwise specified

**Figure 11. Output Return Loss vs. Temperature
@ 12 dB State**

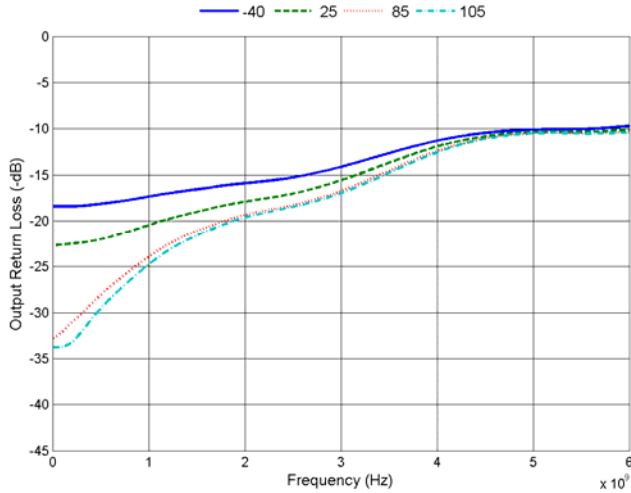
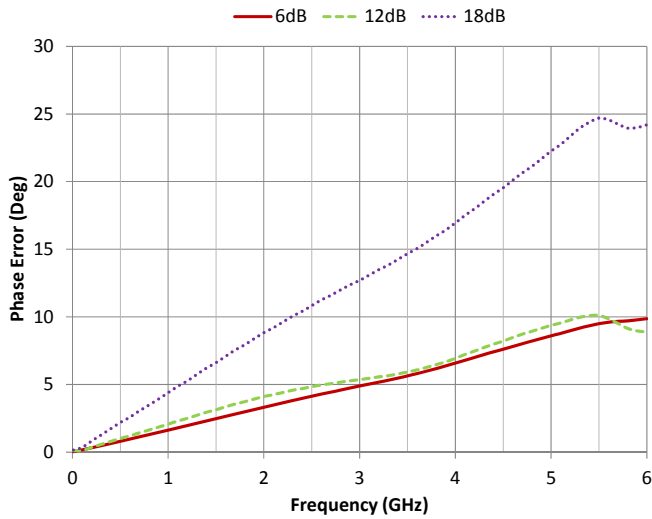


Figure 12. Relative Phase vs. Frequency



Evaluation Kit

The 2-bit DSA evaluation kit board was designed to ease customer evaluation of Peregrine's PE43205.

To evaluate the PE43205, apply 3.3V to the V_{DD} header pin and Ground to the GND header pin. The DUT can be controlled two ways:

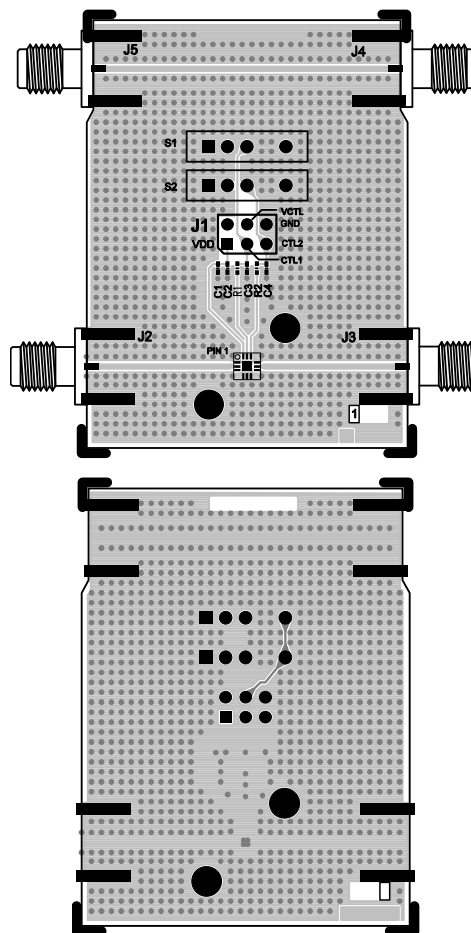
1. *The mechanical switches in conjunction with the VCTL pin can be used.* Apply desired control voltage to VCTL header pin. The top mechanical switch controls the 6 dB stage, the bottom mechanical switch controls the 12 dB stage. For each switch, the left position is the 0V condition, while the right position is the V_{CTRL} condition. The middle position leaves the control pin floating.
2. *The CTL1 and CTL2 pins on the header can be used.* Each pin directly controls the 6 dB and 12 dB stage respectively. The VCTL pin on the header is left open. The mechanical switches may be left uninstalled or must be kept in the middle position.

Note: To accurately measure the fast switching performance of the PE43205, C3 and C4 should be removed.

Power-up Control Settings

The PE43205 will always power up into the state determined by the voltages on the two control pins. The DSA can be preset to any state within the 18 dB range by pre-setting the parallel control pins prior to power-up. There is a 10 μ s delay between the time the DSA is powered-up to the time the desired state is set. If the control pins are left floating during power-up, the device will default to the minimum attenuation setting (insertion loss state).

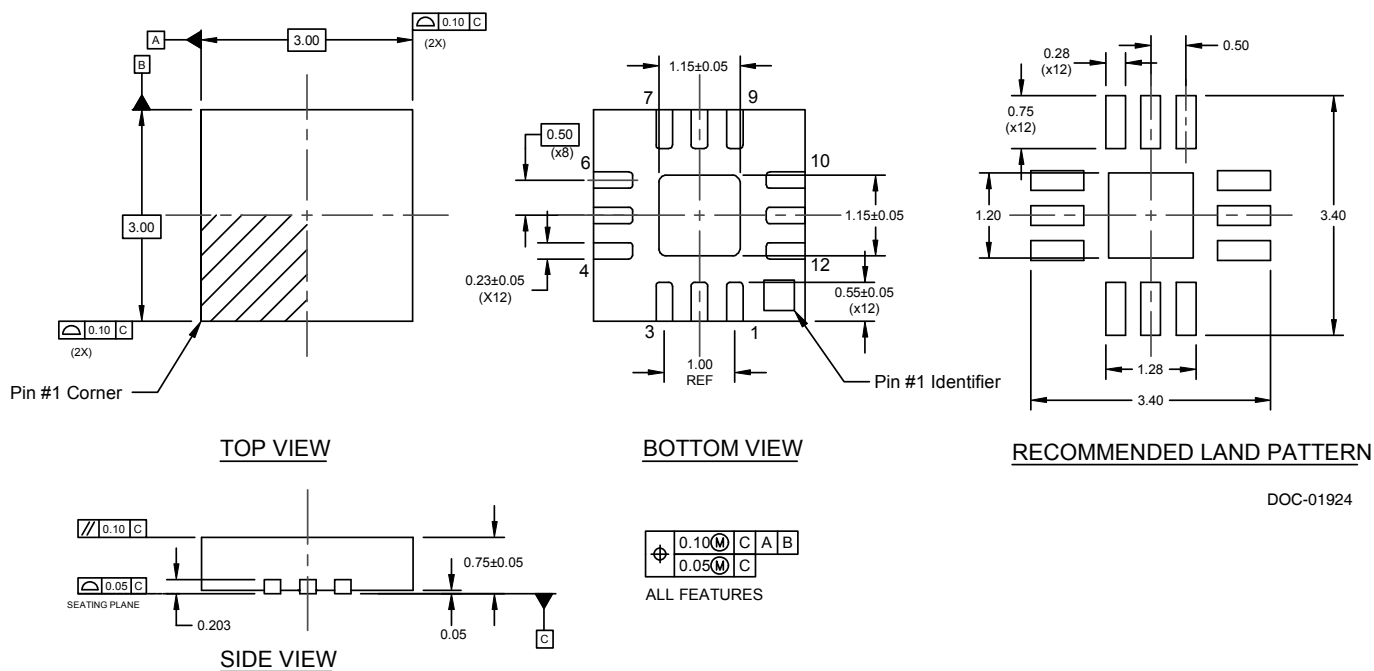
Figure 13. Evaluation Board Layout



PRT-53374

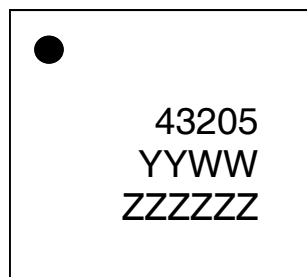
DOC-30927

Figure 15. Package Drawing
12-lead 3x3 mm QFN



Note: Pin 1 identification tab is electrically connected to the exposed ground paddle.

Figure 16. Top Marking Specifications



DOC-51207

- = Pin 1 designator
- 43205 = Five digit part number
- YYWW = Date Code, last two digits of the year and work week
- ZZZZZZ = Maximum six characters of the assembly lot code

0.30 $\pm$ 0.05

R 0.3 MAX

2.00 $\pm$ 0.05 SEE NOTE 3

4.00 SEE NOTE 1

Pin 1

ϕ 1.5 $\pm$ 0.1/-0.0

0.00

ϕ 1.50 MIN

1.75 $\pm$ 0.10

5.50 $\pm$ 0.05 SEE NOTE 3

12.0 $\pm$ 0.3

0.25

R.25

SECTION A - A

NOTES:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE $\pm$ 0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

A_0 = 3.30

B_0 = 3.30

K_0 = 1.10

-----> Tape Feed Direction ----->

Pin 1

Top of Device

Device Orientation in Tape

Ordering Code	Description	Package	Shipping Method
PE43205MLAA-Z	PE43205 Digital step attenuator	Green 12-lead 3x3 mm QFN	3000 units/T&R
EK43205-01	PE43205 Evaluation kit	Evaluation kit	1/Box

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