W-band Multifunction : Multiplier / MPA

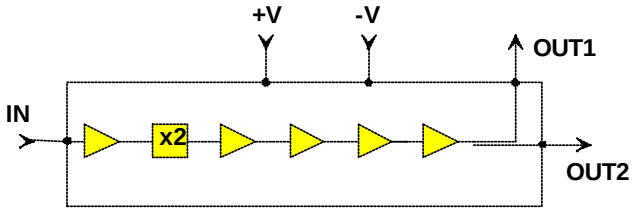
GaAs Monolithic Microwave IC

Description

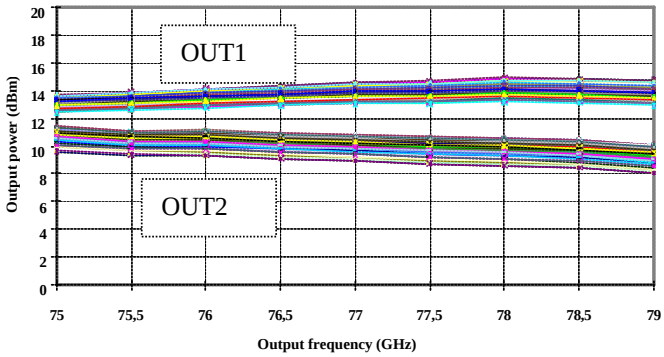
The CHU2277 is a W-band monolithic multifunction which integrates a frequency multiplier, a four-stage amplifier and a power divider. The frequency multiplier is based on an active transistor and allows to operate at low input level with a reduced power consumption. This chip provides two outputs at 77GHz, the main one is for the transmission path and the auxiliary one for the receiving mixer (s) LO signal. All the active devices are internally self biased. This chip is compatible with automatic equipment for assembly.

The circuit is manufactured with the P-HEMT process : 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



W-band multifunction block-diagram



Typical output power characteristic
Pin = 7dBm
(on wafer measurement)

Main Features

- Wide operating frequency range
- Low input power : 5dBm typical
- High output power (OUT1)
- Auxiliary output power (OUT2)
- Low AM noise
- High temperature range
- On-chip self biasing
- Automatic assembly oriented
- Low DC power consumption
- Chip size : 4.65 x 1.6 x 0.1mm

Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_in	Input frequency	38		38.5	GHz
F_out	Output frequency	76		77	GHz
P_out1	Main output power		13		dBm
P_out2	Auxiliary output power		10		dBm

ESD Protections : Electrostatic discharge sensitive device observe handling precautions !

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Electrical Characteristics

Full operating temperature range, used according to section "Typical assembly and bias configuration"

Symbol	Parameter	Min	Typ	Max	Unit
F_in	Input frequency	38		38.5	GHz
F_out	Output frequency	76		77	GHz
P_in	Input power	0	5	12	dBm
P_out1	Output power (OUT1) (1)	11	13	16	dBm
P_out2	Output power (OUT2) (1)	8	10	13	dBm
Fin_rej	fundamental rejection (dBc/Pout1(2Fin))	45	55		dBc
S_rej	Spurious rejection (dBc/Pin)				
	12.75 GHz	40	50		dBc
	25.5 GHz	40	50		
	38.25 GHz	35	45		
	51 GHz	50	60		
	63.75 GHz	40	50		
	76.5 GHz	15	20		
	89.25 GHz	40	50		
	102 GHz	50	60		
An	Amplitude noise @ 1kHz (SSB)		-137	-132	dBc/Hz
	Amplitude noise @ 10kHz (SSB)		-145	-140	
	Amplitude noise @ 100kHz (SSB)		-151	-146	
	Amplitude noise @ 200kHz (SSB)		-153	-148	
	Amplitude noise @ 1MHz (SSB)		-157	-152	
VSWR_in	VSWR at input port (50Ω)		2:1	2.5:1	
+V	Positive supply voltage (2)	4.4	4.5	4.6	V
+I	Positive supply current		180	240	mA
-V	Negative supply voltage (2)	-4.6	-4.5	-4.4	V
-I	Negative supply current		14	20	mA
Top	Operating temperature range	-40		100	°C

(1) Defined on load VSWR £1.5:1.

(2) Negative supply voltage must be applied at least 1us before positive supply voltage.

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Absolute Maximum Ratings (1)

Symbol	Parameter	Values	Unit
P_in	Input power (2)	13	dBm
+V	Positive supply voltage	5	V
-V	Negative supply voltage	-5	V
+I	Positive supply current	250	mA
-I	Negative supply current	20	mA
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s

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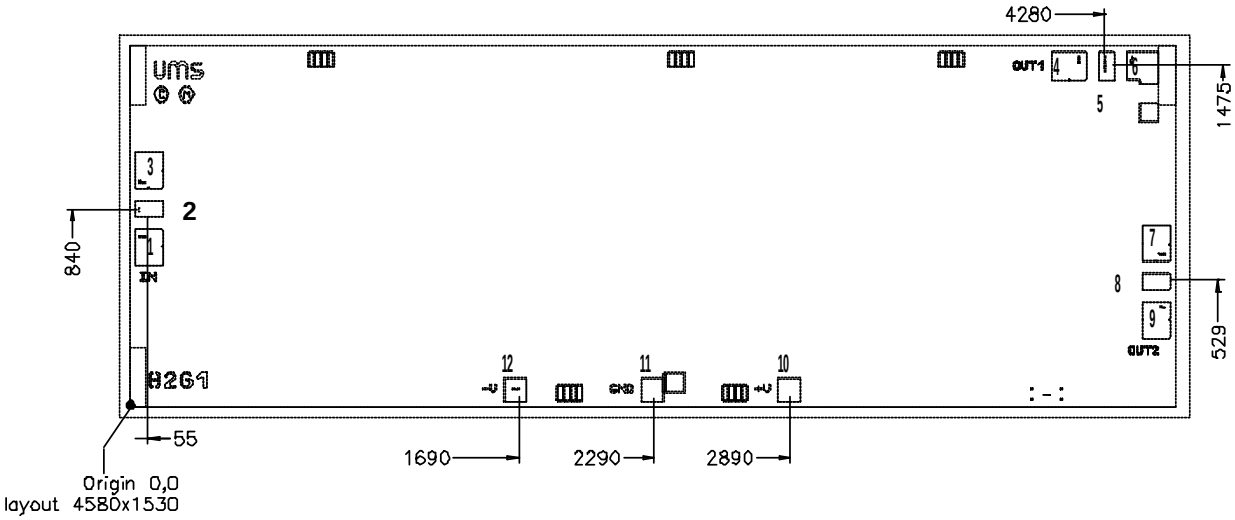
Chip Mechanical Data and Pin References



Unit = µm
External chip size (layout size + dicing streets) = 4650 x 1600 ± 35
Chip thickness = 100 +/- 10
HF Pads (2, 5,8) = 68 x 118
DC/IF Pads = 100 x 100

Pin number	Pin name	Description
1,3,4,6,7,9		Ground : should not be bonded. If required, please ask for more information.
11		Ground (optional)
2	**IN**	Input port
5	**OUT1**	Main output
8	**OUT2**	Auxiliary output
10	**+V**	Positive supply voltage
12	**-V**	Negative supply voltage

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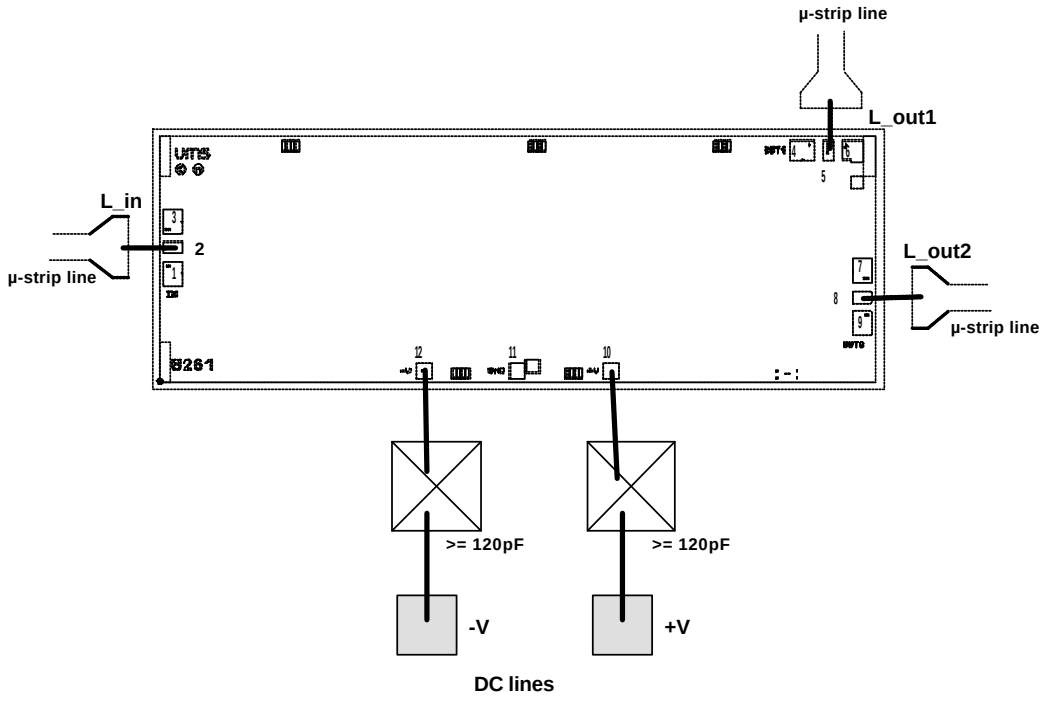
Typical Assembly and Bias Configuration



This drawing shows an example of assembly and bias configuration. All the transistors are internally self biased. An external capacitor is recommended for the positive and negative supply voltages.
For the RF pads the equivalent wire bonding inductance (diameter=25µm) have to be according to the following recommendation.

Port	Equivalent inductance (nH)	Wire length (mm) (1)
IN (2)	L_in = 0.32	0.4
OUT1 (5)	L_out1 = 0.32	0.4
OUT2 (8)	L_out2 = 0.32	0.4

(1) This value is the total length including the necessary loop from pad to pad.

For a micro-strip configuration a hole in the substrate is necessary for chip assembly.

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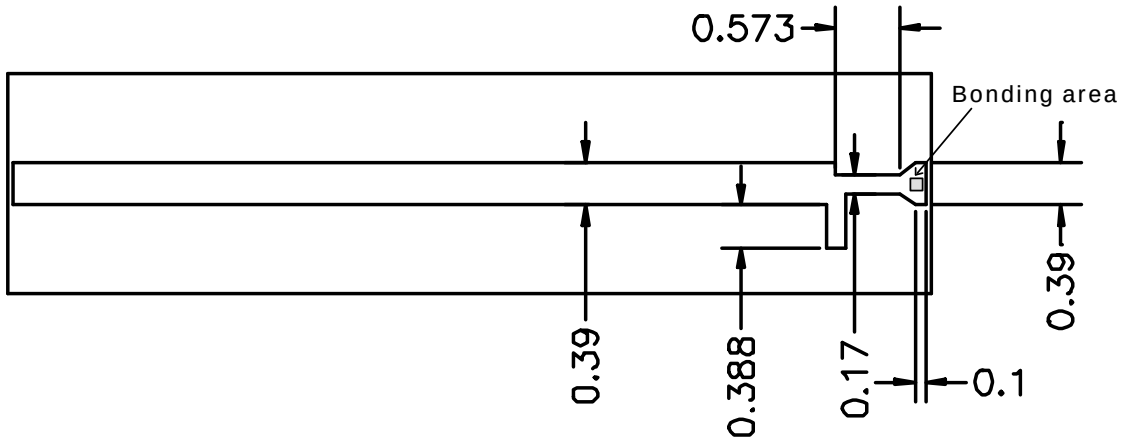
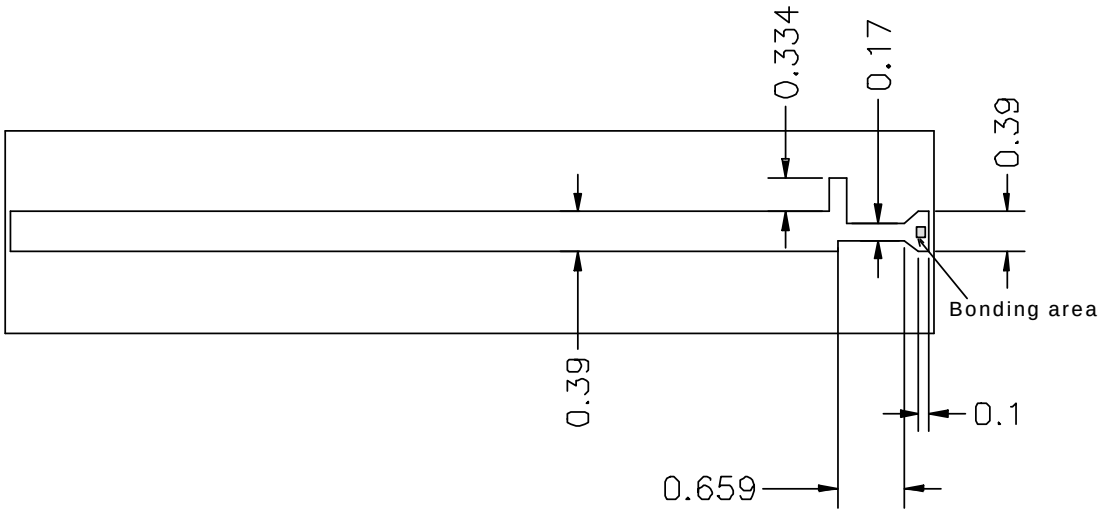
As the connections at 77GHz (between MMIC and MMIC or between MMIC and external substrate) are critical, the transition matching network is split into two parts: one on MMIC and one on the external substrate. This choice allows to do, for OUT2 port, a direct connection between MMICs. For a connection to an external substrate a network is proposed on soft substrate for OUT1 and OUT2 ports. The following drawings gives the dimensions for a DUROID substrate (thickness=0.127mm, εr=2.2).



Proposed matching network for a 50Ω transition between OUT1 and a µ-strip line on DUROID substrate



Proposed matching network for a 50Ω transition between OUT2 and a µ-strip line on DUROID substrate.

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Ordering Information

Chip form : CHU2277-99F/00

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