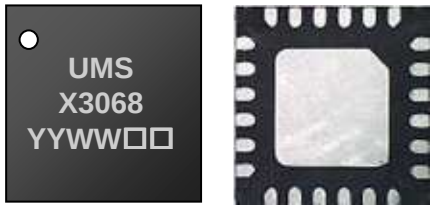
15-30GHz Frequency Multiplier

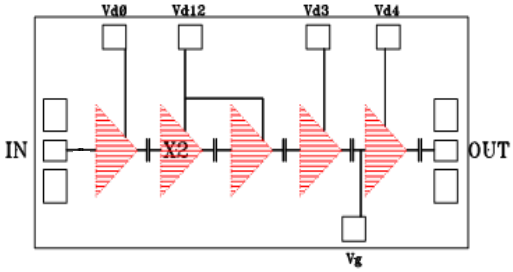
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHX3068-QDG is a Ka-band frequency multiplier monolithic integrated circuit. Typical applications are for telecommunication such as DVB-RCS.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in lead-free SMD package





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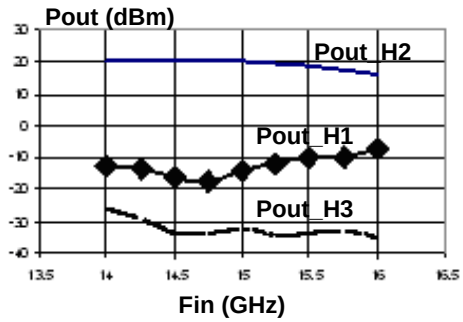
Main Features

- 14 to 15 GHz input frequency
- Input and output integrated buffers
- 20dBm output power
- Low input power: 0 to 5dBm
- DC bias 270mA @ 4V
- 24L-QFN4X4 SMD package



Main Characteristics

Tamb. = 25℃, Vd = 4.V typical consumption ≈270mA

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	14		15	GHz
Fout	Output frequency range	28		30	GHz
Pin	Input power	0		5	dBm
Pout	Output power		20		dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Tamb = +25℃, Vd0=Vd1,2=Vd3=Vd4= 4.V Consumption(Id0+Id1,2+Id3+Id4) ≈ 270mA (1)

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	14		15	GHz
Fout	Output frequency range	28		30	GHz
Pin	Input power	0		5	dBm
Pout_H2	Output power for +2 dBm input power		20		dBm
Rej_H1	Fundamental rejection for +2dBm input power		30		dBc
Rej_H3	Third harmonic rejection for +2dBm input power		50		dBc
VSWRin	Input VSWR		2.0:1		
VSWRout	Output VSWR		2.0:1		
Vd	Drain voltage supply		4		V
Vg	Gate voltage supply (1)		-1.8		V
Id	Bias current (with RF)		270		mA

(1) Adjust Vg to achieve Id4=115 mA

(These values are representative of onboard measurements as defined on the drawing at page 8)

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Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Id	Drain bias current	330	mA
Pin	Maximum input power	+8	dBm
Tjmax	Maximum Junction Temperature	175	℃
Ta	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

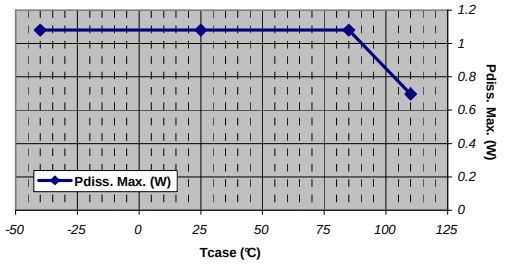
Device thermal performances:

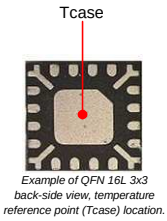
All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the case temperature (Tcase) can not be maintained below the maximum temperature specified in order to guarantee the nominal device life time (MTTF) (see the curve Pdiss. Max).

DEVICE THERMAL SPECIFICATION : CHX3068-QDG			
Max. junction temperature (Tj max)		:	155 ℃
Max. continuous dissipated power @ Tcase=	85 ℃	:	1.08 W
=> Pdiss derating above Tcase(1)=	85 ℃	:	15 mW/℃
Junction-Case thermal resistance (Rth J-C)(2)		:	<65 ℃/W
Min. package back side operating temperature(3)		:	-40 ℃
Max. package back side operating temperature(3)		:	85 ℃
Min. storage temperature		:	-55 ℃
Max. storage temperature		:	125 ℃

(1) Derating at junction temperature constant = Tj max.
*(2) Rth J-C is calculated for a worst case where the **hotter junction** of the MMIC is considered.*
(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example of QFN 16L 3x3 back-side view, temperature reference point (Tcase) location.

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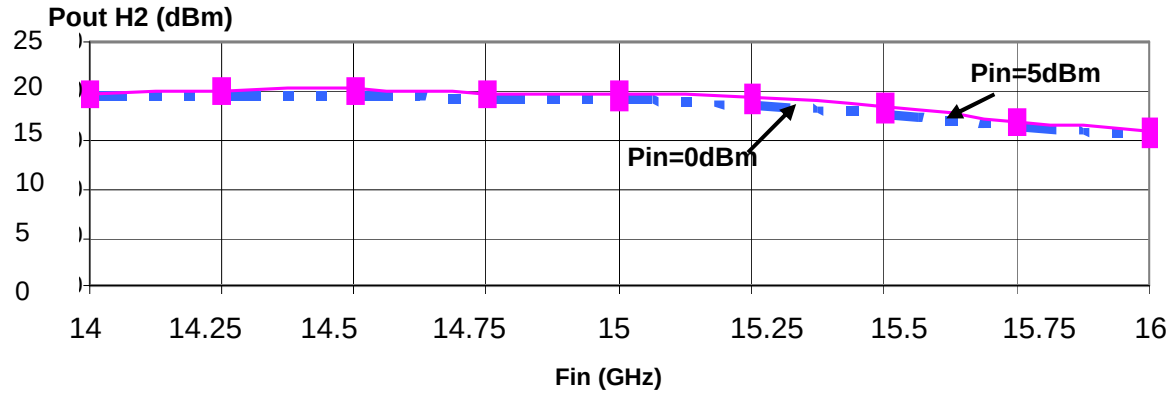
Typical PCB Measured Performances

Tamb=+25℃, Vd0=Vd1,2=Vd3=Vd4=4V Vg for Id4=115mA (≈-1.8V)

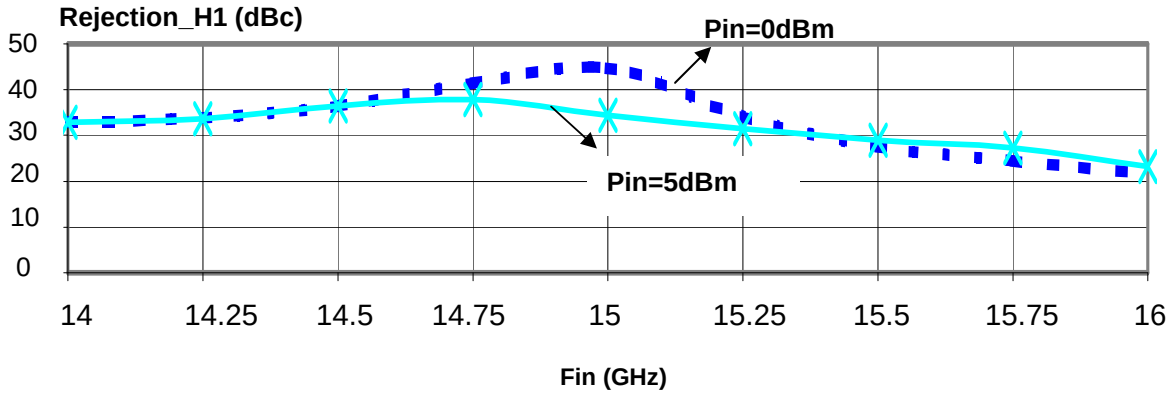
Second harmonic output power versus input frequency (Fin)

@ Pin=0 & 5dBm



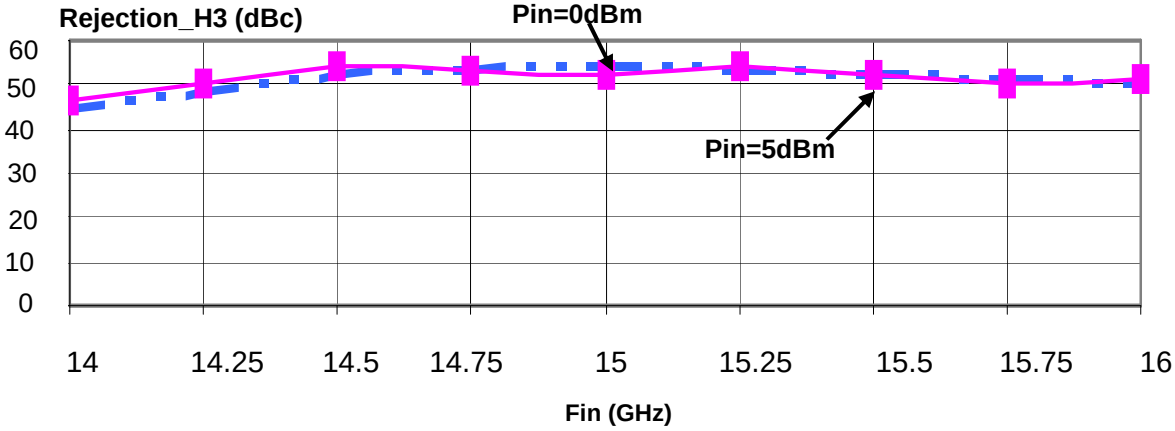
Fundamental rejection versus Fin

@ Pin=0 & 5dBm



3rd harmonic rejection versus Fin

@Pin=0 & 5dBm



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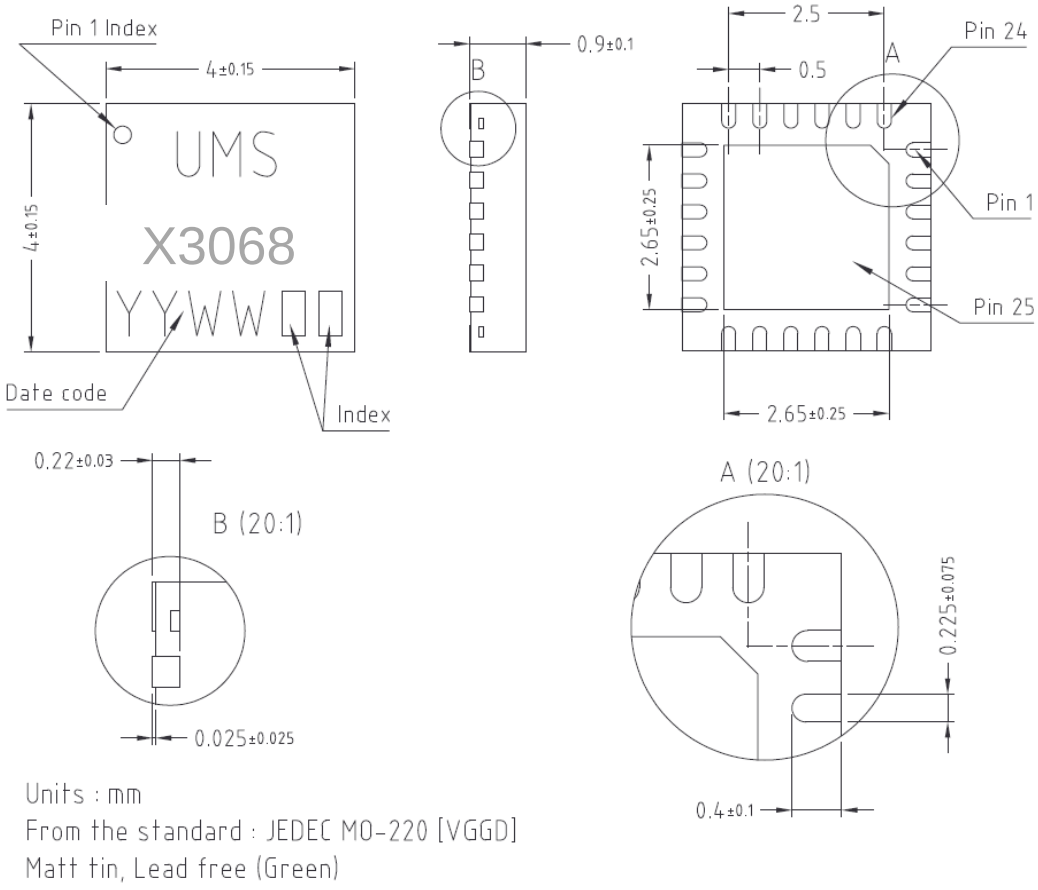
Package outline [(1)]:



Matt tin, Lead Free	(Green)	1-	NC	13-	NC
Units	mm	2-	NC	14-	GND
From the standard	JEDEC MO-220	3-	GND	15-	RF OUT
	(VGGD)	4-	RF IN	16-	GND
25	GND	5-	GND	17-	NC
		6-	NC	18-	NC
		7-	NC	19-	Vd4
		8-	NC	20-	NC
		9-	NC	21-	Vd3
		10-	Vg	22-	Vd1, 2
		11-	NC	23-	Vd0
		12-	NC	24-	NC

[(1)]The package outline drawing included to this data-sheet is given for indication. Refere to the application note AN0017 available at http://www.ums-gaas.com for exact package dimensions.

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Recommanded package footprint

Refere to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommandations.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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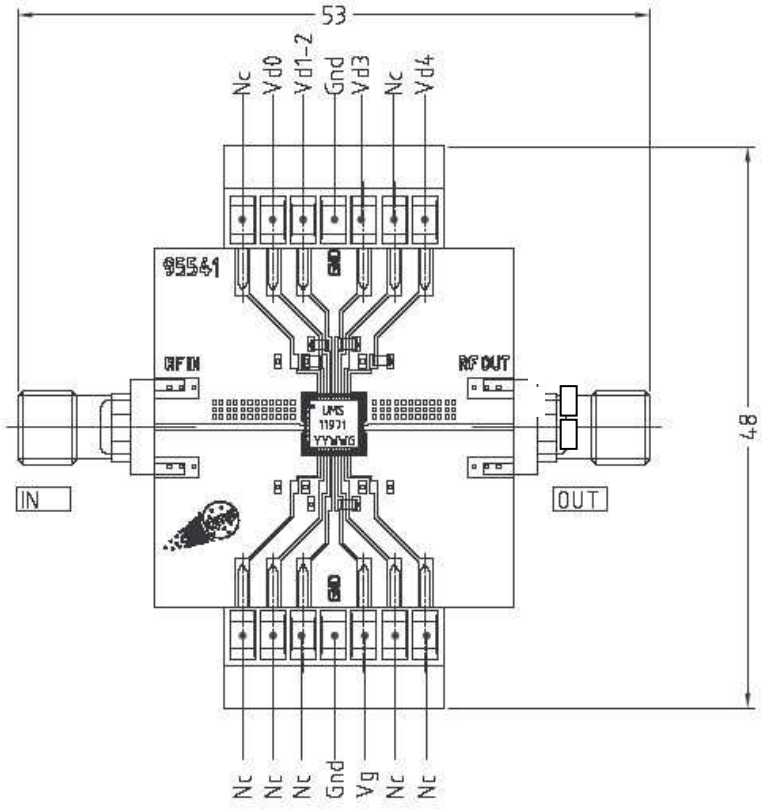
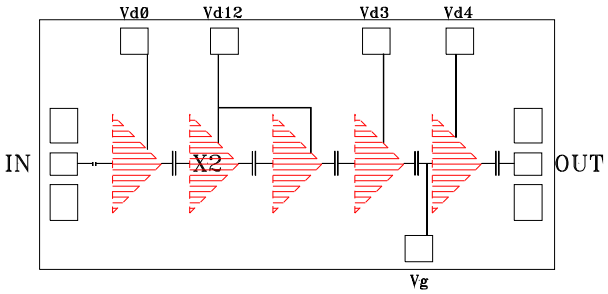
Proposed Assembly board for the 24L-QFN4x4 products characterization.

- Compatible with the proposed foot print.
- Based on typically RO4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



Capacitor 10nF ± 10%



Biasing :

-Vd0=Vd1,2=Vd3=Vd4=4V
-Adjust Vg to achieve Id4=115mA typically Vg=-1.8V)

Id0+Id1,2+Id3+Id4 ≈270mA

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Evaluation mother board:

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- (See application note AN0017 for details).

Ordering Information

QFN 4x4 RoHS compliant package : CHX3068-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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