United Monolithic Semiconductors

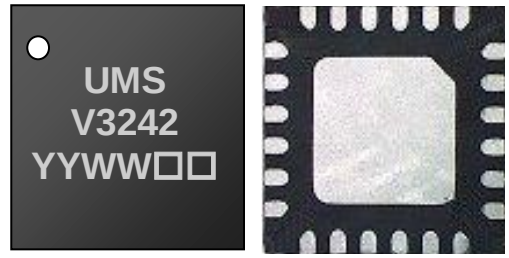
CHV3242-QDG

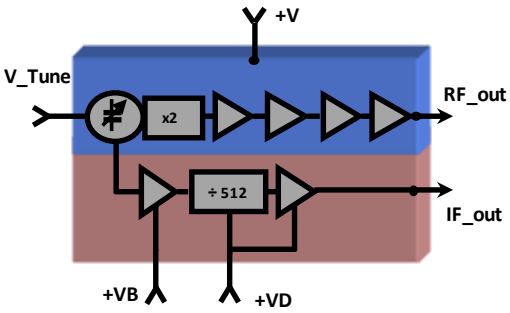
Fully integrated HBT K-Band VCO

Description

The CHV3242-QDG is a monolithic multifunction circuit suitable for frequency generation. It integrates an X-band "push-push" oscillator with frequency control (VCO) thanks to base-collector diodes, used as varactors, a K-band buffer amplifier and a divider by 512. All the active devices are internally self-biased.

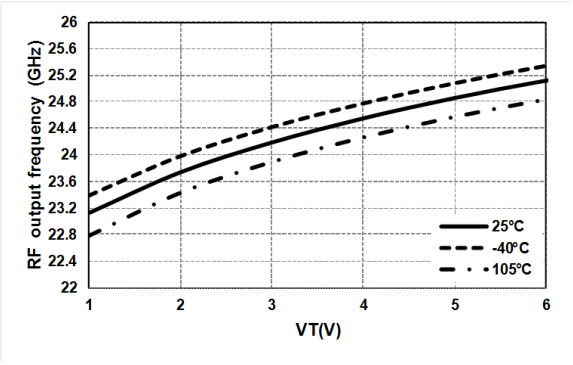
The circuit is delivered in a 24 Leads RoHS compliant QFN4x4 package.





Main Features

- K-band VCO + buffers + prescaler /512
- Prescaler and buffer switching capability with low pulling, for optimum efficiency
- Fully integrated VCO (no external resonator)
- Low phase noise
- High temperature range
- High output power
- High frequency stability
- 4th amplifier bias usable for power setting
- On chip self-biased devices
- Standard SMD package: 24L-QFN4x4
- MSL1



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output frequency range on RF_out port	24.0	24.125	24.25	GHz
F_vco	VCO frequency		F_out/2		GHz
IF_out	Output Intermediate frequency		F_out/1024		GHz
P_out	Output power on RF_out port		16		dBm
PFI	Output power at Intermediate freq. (IF)	-3	1		dBm
PN	SSB Phase Noise @F_out@100KHz		-94		dBc/Hz

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Electrical Characteristics

Note: Electrical parameters specified below are defined for an operating temperature range from -40°C to 105°C.

VCO & buffer section

Symbol	Parameters	Min	Typ	Max	Unit
F_out	Output Frequency range (Operating band)	24		24.25	GHz
F_vco	VCO frequency		F_out/2		GHz
V_Tune	Voltage Tuning range	1		6	V
T_sens	Tuning sensitivity	250	400	725	MHz/V
F_drift	Frequency drift rate		5		MHz/°C
H1	Harmonics 1/2F_out			-40	dBc
H3	Harmonics 3/2 F_out			-40	dBc
H4	Harmonics 2 F_out			-20	dBc
Pres_Rj	F_out prescaler spurious rejection	45	65		dBc
PN	SSB Phase Noise @ F_out @ 100 KHz		-94	-80	dBc/Hz
VSWR	Main Output (RF_Out) VSWR		2:1		
L_Pull	Load Pulling into 2:1 VSWR for all phases			8	MHz
PB_Pull	Prescaler & 12GHz buffer switching pulling		3		MHz
Push	Pushing @ within the V_tune range			250	MHz/V
P_out	Output Power on RF_out port @ 5V supply	12	16	19	dBm
+I	Positive supply current		130	170	mA
+V	Positive supply voltage	4.9	5	5.1	V

Prescaler & buffer section

Symbol	Parameters	Min	Typ	Max	Unit
IF_out	IF Output Frequency		F_out/1024		GHz
Pres_P	Output Power	-3	1		dBm
+ID	Prescaler & 12GHz buffer supply current	10	18	32	mA
+IB	12GHz prescaler's buffer supply current	2	4	6	mA

All the parameters are specified within F_out specified frequency range.

The minimum and maximum values take into account the spread due to the operating temperature and process spread.

These performances have been obtained with the chip in QFN package assembled on the recommended boards (ref. 500865) described in this document. These performances are highly dependent on this environment.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameters	Values	Unit
V_tune	Positive Tuning voltage	10	V
+V	Positive supply voltage/Minimum supply voltage	6 / -0.3	V
+ID	Positive supply current (Prescaler)	35	mA
+IB	Positive supply current (Prescaler's buffer)	7	mA
+IB1 / +IB2	Positive supply current (buffers 2 & 3)	50 / 60	mA
+I1 / +I2	Positive supply current (VCO+ buffer 1)	40 / 50	mA
Top	Operating temperature range (2)	-40 to +105	°C
Tcase Max	Absolute maximum rating Tcase temperature (2)	115	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Temperature of the back side of the QFN package

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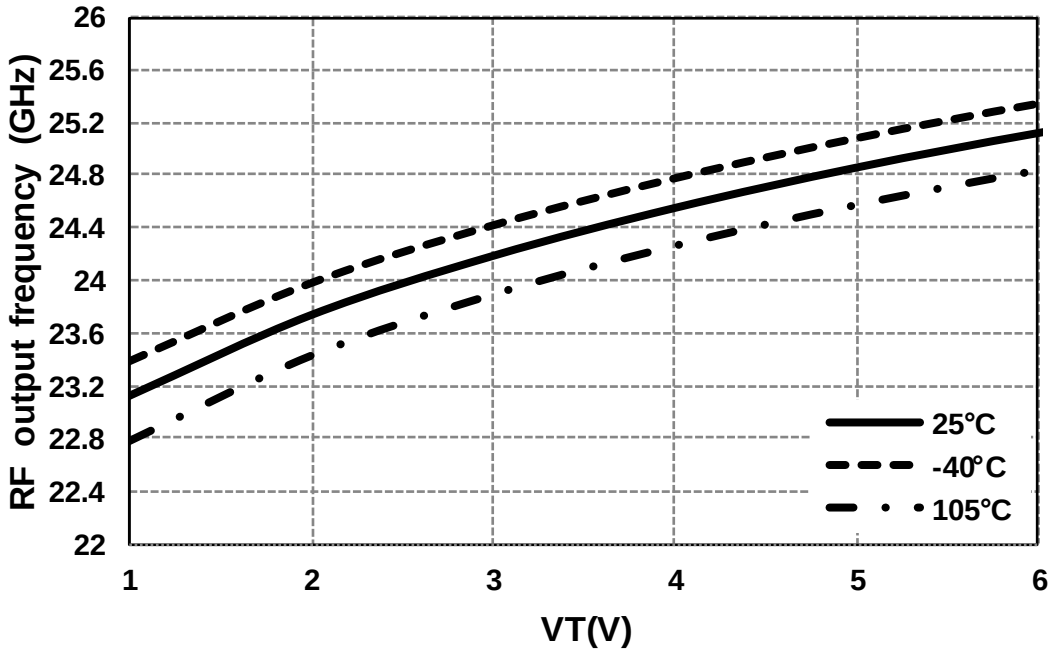
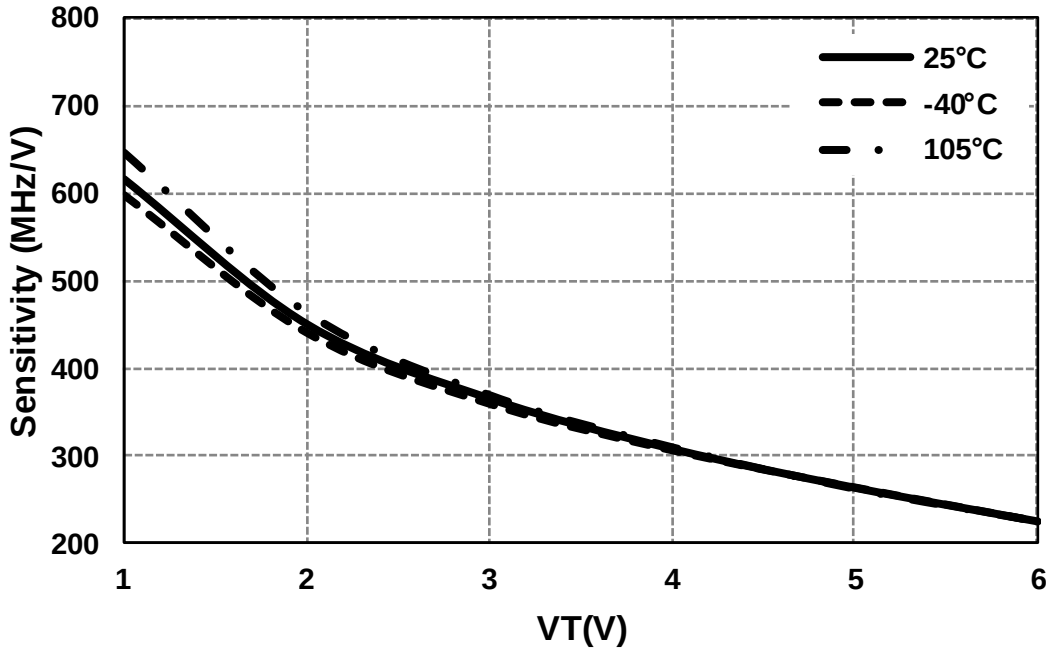
Typical QFN Measurements on board 500865 (at QFN accesses)

Note: The temperature mentioned below is taken at the back side of the QFN package.

RF Output Frequency versus V-tune



Sensitivity versus V-tune



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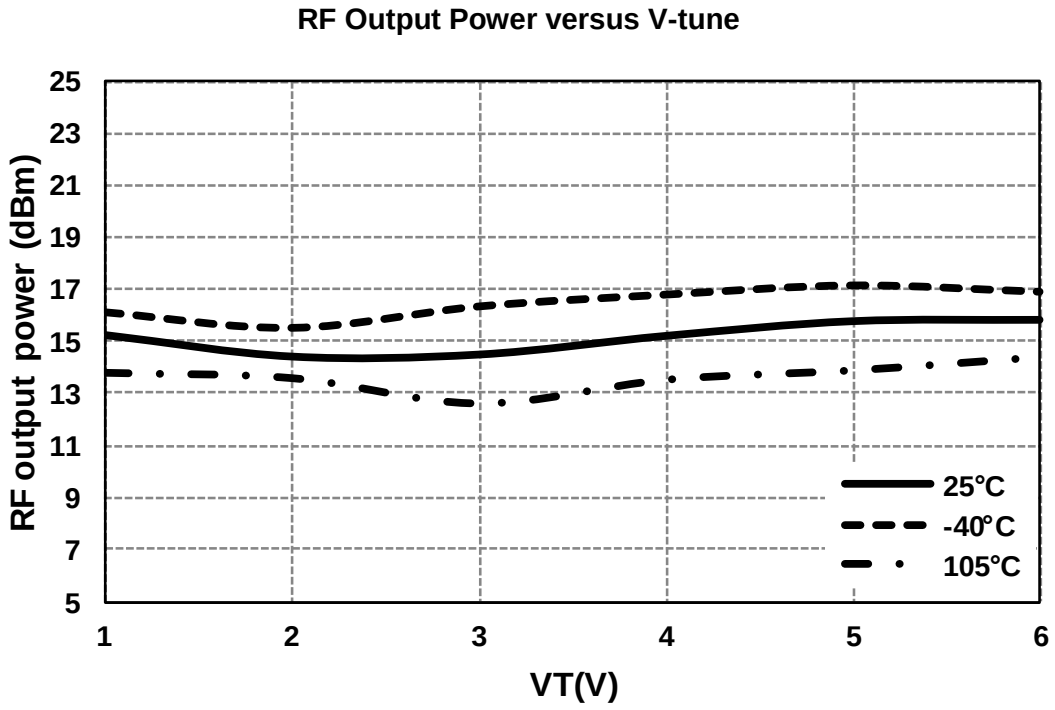
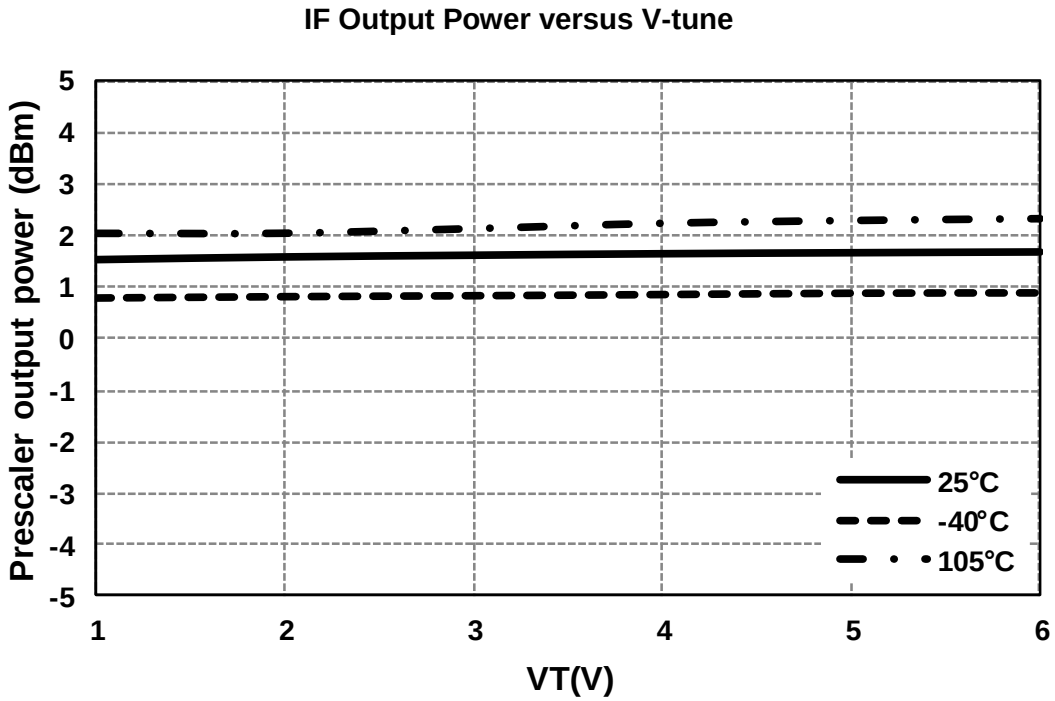
Typical QFN Measurements on board 500865 (at QFN accesses)





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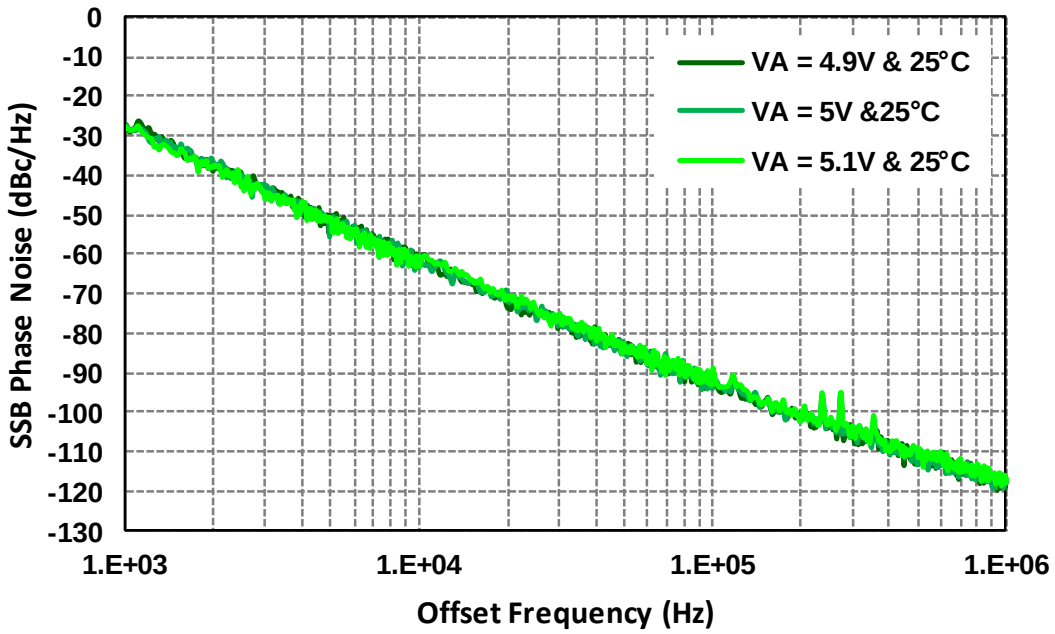
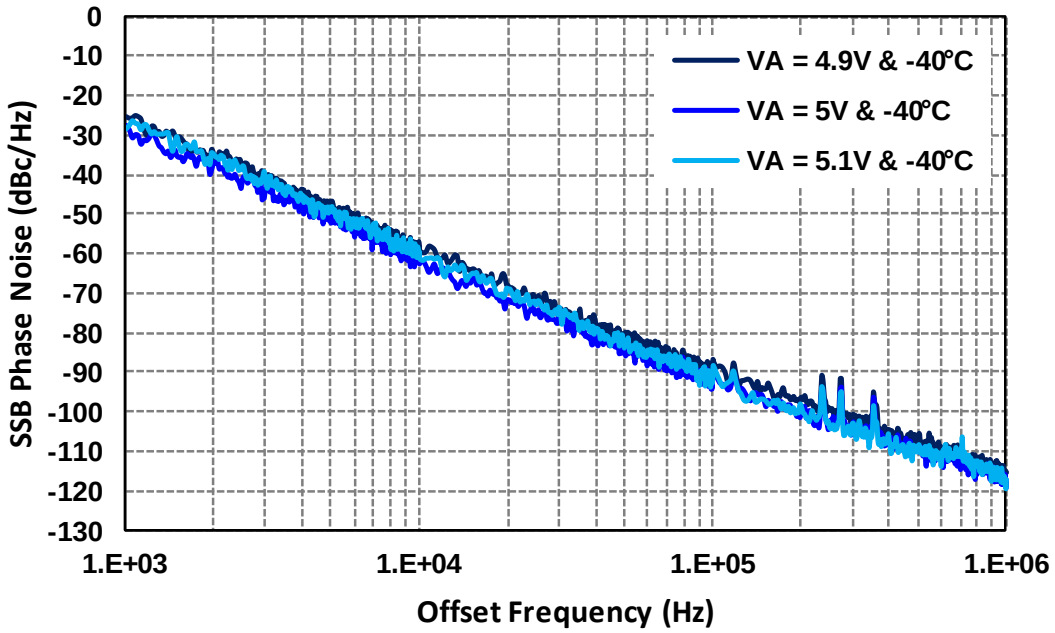
Typical QFN Measurements on board 500865 (at QFN accesses)

Phase Noise versus Offset frequency from 24GHz @ Top = +25°C
(VA=V1=V2=VB1=VB2=VD=VB)



Phase Noise versus Offset frequency from 24GHz @ Top = -40°C
(VA=V1=V2=VB1=VB2=VD=VB)



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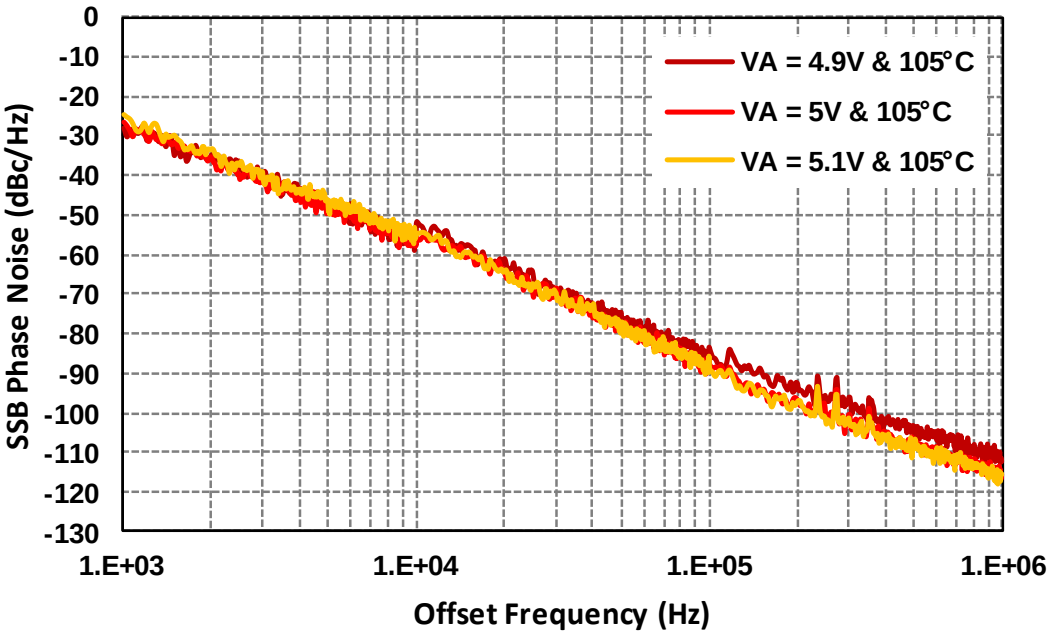
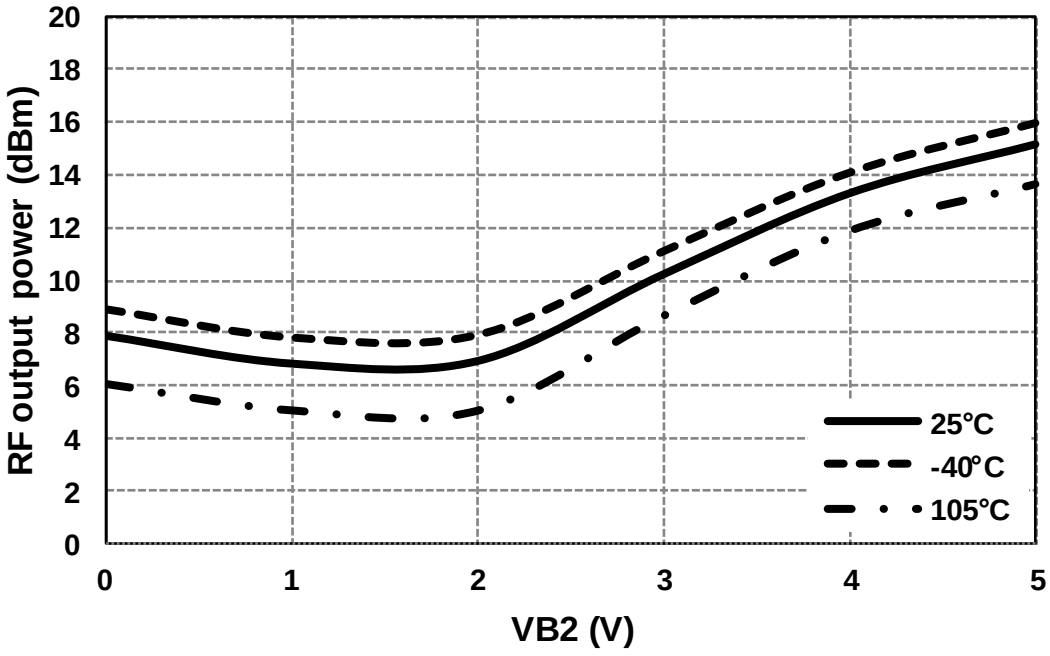
Typical QFN Measurements on board 500865 (at QFN accesses)

Phase Noise versus Offset frequency from 24GHz @ Top = 105°C
(VA=V1=V2=VB1=VB2=VD=VB)



4th stage of the RF amplifier bias VB2 used for power setting
Output power vs. VB2 @ 24 GHz



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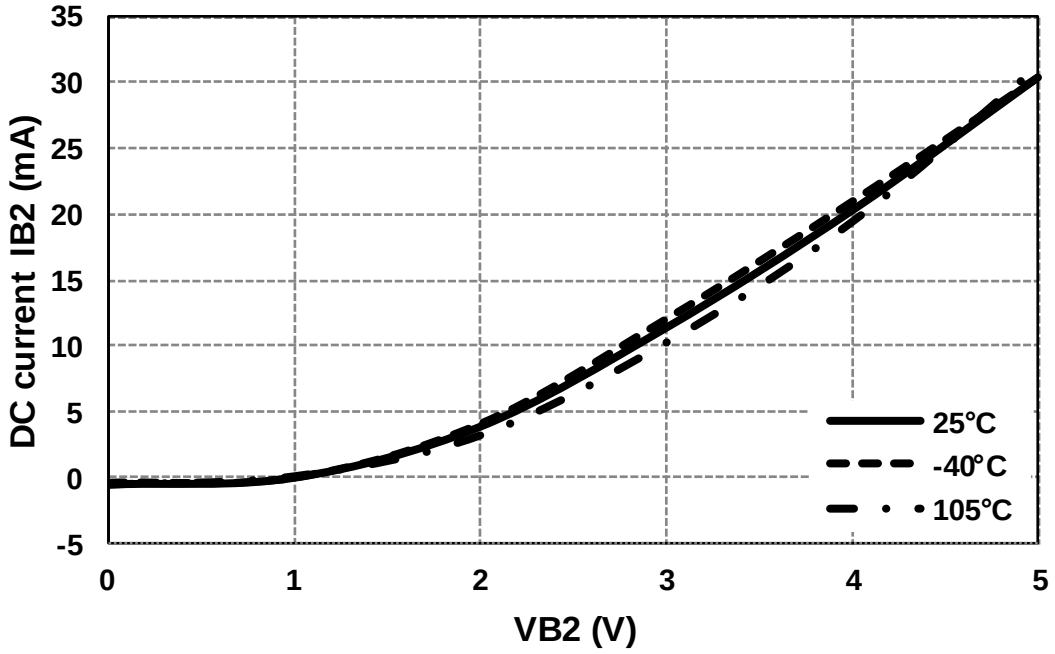
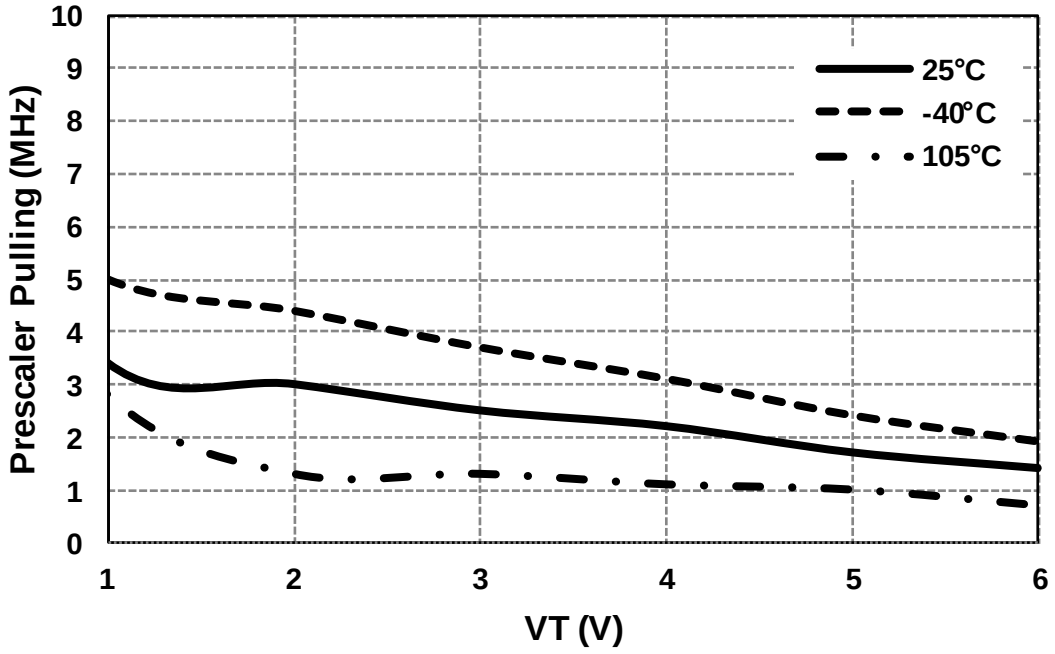
Typical QFN Measurements on board 500865 (at QFN accesses)

4th stage of the RF amplifier bias VB2 used for power setting
IB2 Current consumption vs. VB2 @ 24 GHz



Prescaler and 12 GHz buffer switching effect on VCO frequency (MHz)



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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the Tcase temperature cannot be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

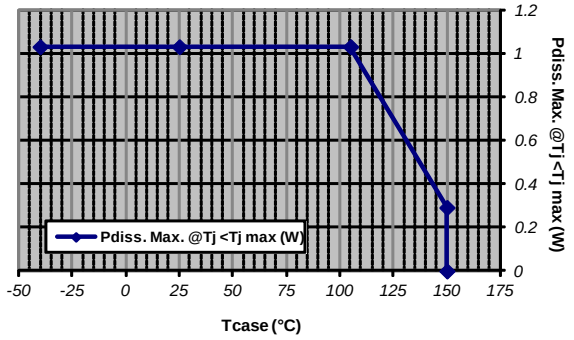
Note: the thermal specification is given by considering that all the voltage supply pins of the device are biased.

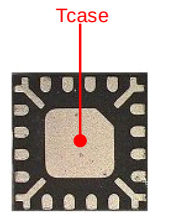
DEVICE THERMAL SPECIFICATION : CHV3242-QDG			
Recommended max. junction temperature (Tj max)	:	168	°C
Junction temperature absolute maximum rating	:	175	°C
Max. continuous dissipated power (Pdiss. Max.)	:	1.0	W
=> Pdiss. Max. derating above Tcase(1)= 105 °C	:	16	mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<60	°C/W
Minimum Tcase operating temperature(3)	:	-40	°C
Maximum Tcase operating temperature(3)	:	105	°C
Minimum storage temperature	:	-55	°C
Maximum storage temperature	:	150	°C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

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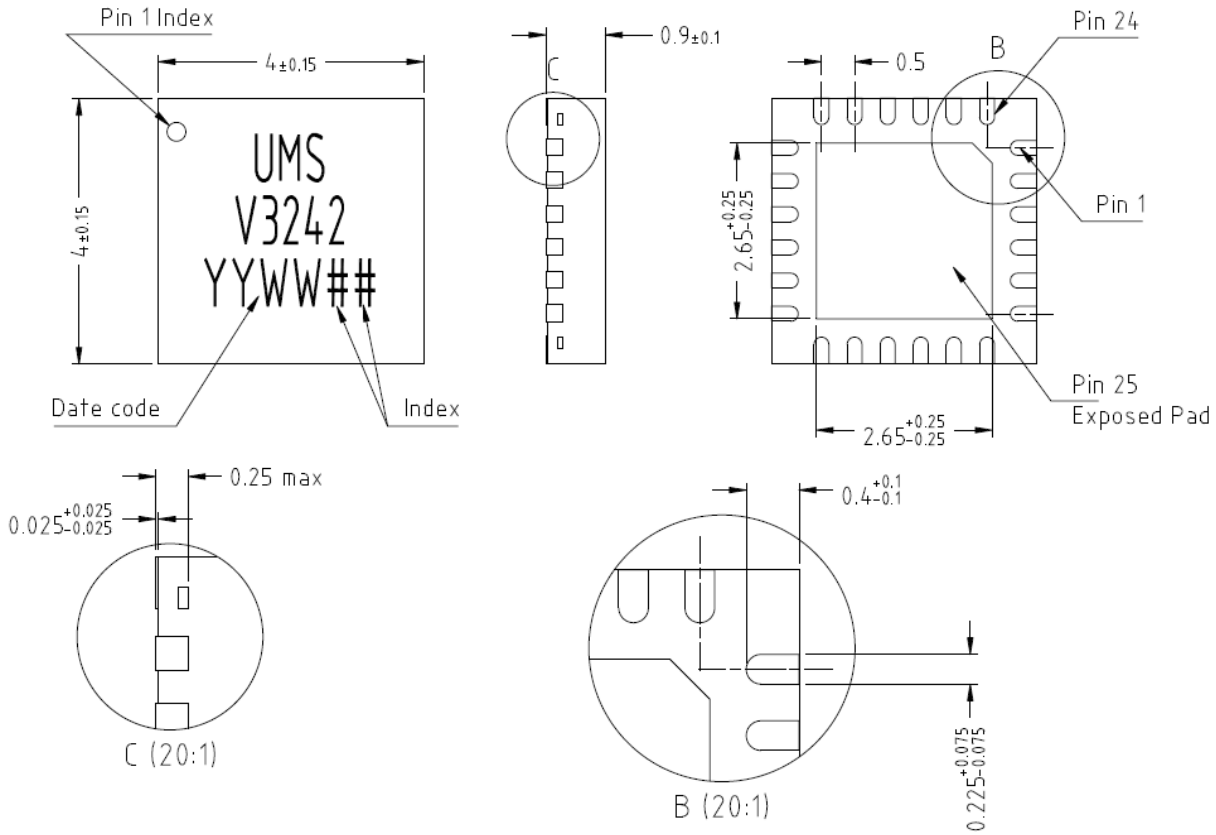
Package outline [1]



Matte tin, Lead Free	(Green)	1- Nc	9- Nc	17- Gnd[2]
Units :	mm	2- P	10- VB	18- Nc
From the standard :	JEDEC MO-220 (VGGD)	3- Nc	11- V1	19- Nc
		4- VT	12- Nc	20- VB2
		5- Nc	13- VB1	21- V2
		6- Nc	14- Nc	22- Nc
		7- Nc	15- Gnd[2]	23- VD
		8- Nc	16- RF	24- Nc

[1] The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.
[2] It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL1

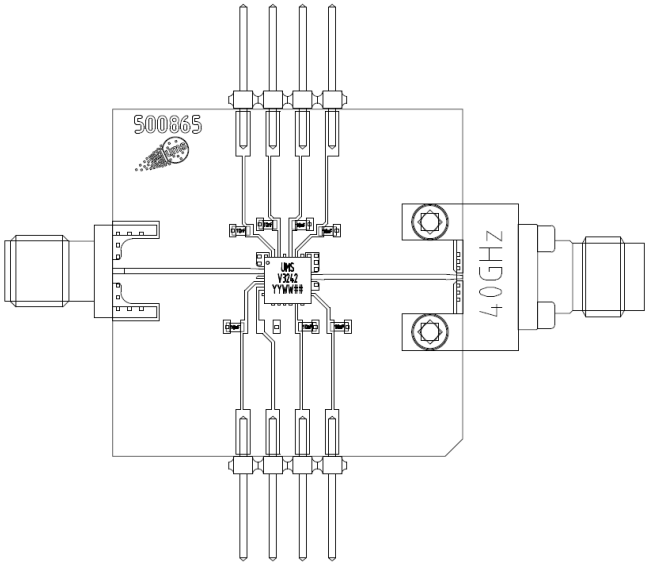
ESD sensitivity

Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)
ESD STM5.1-2001	HBM Class 1C (1000V to <2000V)

Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.

Recommended Test Fixture (Ref. 500865) for measurements over Temperature Range:



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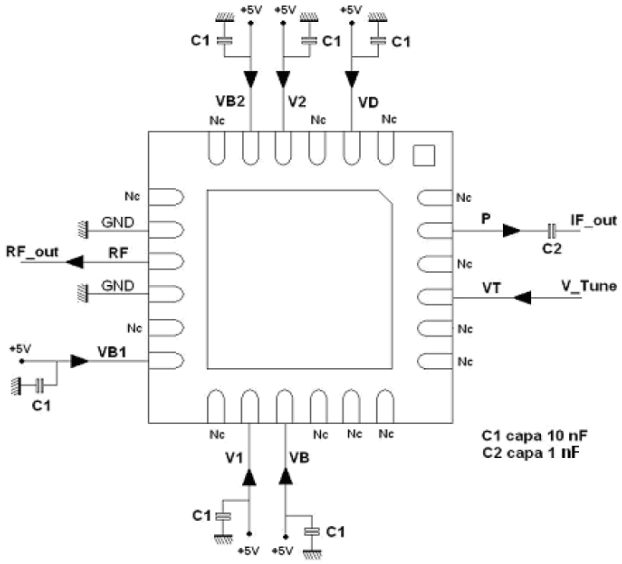
External Components and bias configuration (recommended)



Important: A capacitor is required on the prescaler output port as a DC block (C2).

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Notes:

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHV3242-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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