S-Band 6-bit Phase Shifter

GaAs Monolithic Microwave IC in SMD leadless package

Description

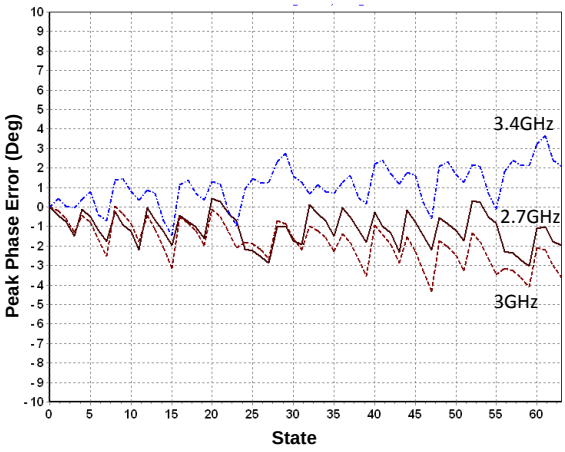
The CHP1102-QGG is 6-bit phase shifter with an amplifier at its input and output. The circuit is driven by a TTL compatible parallel interface. It is designed for radar systems.

The circuit is manufactured with a power pHEMT process, 0.25µm gate length, via holes through the substrate and air bridges.

It is supplied in RoHS compliant SMD package.

Main Features

- Operating frequency range: 2.7-3.4GHz
- 5.625° phase step
- 10dB gain
- 0/+3.3V phase shifter control voltage
- 13dBm output @ 1dB comp
- 28L-QFN5x5
- MSL 2



Peak Phase Error vs State @ 2.7, 3, 3.4GHz
(packaged device, board measurement)

Main Characteristics

Tamb= +25°C, V+= +5V, V-= -5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2.7		3.4	GHz
Gain	Small signal gain (state 0)	9	10		dB
RMS_PPE	RMS Peak Phase Error		1		deg

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	2.7		3.4	GHz
G	Small signal gain (state 0)	9	10		
Gvt	Small signal gain variation versus temperature		0.03		dB/°C
NF	Noise figure (state 0)		5.8		dB
S11	Input reflection coefficient			-10	dB
S22	Output reflection coefficient			-10	dB
PPEa	Peak phase error for states 1 to 2		+/- 1.5		°
PPEb	Peak phase error for states 3 to 14		+/- 3		°
PPEd	Peak phase error for states 15 to 63		+/- 5		°
RMS_PPE	RMS Peak phase error		1		°
Ava	Amplitude variation for states 1 to 4		+/- 0.3		dB
Avb	Amplitude variation for states 5 to 63		+/-0.7		dB
RMS_Av	RMS Amplitude variation		0.3		dB
StdDev_Av	Amplitude variation standard deviation		0.12		dB
P_{-1dB}	Output power at 1dB gain compression		13		dBm
V+	DC positive supply		+5		V
V-	DC negative supply		-5		V
Vctrl_L	Phase shifter control voltage (low state)	-	0	0.4	V
Vctrl_H	Phase shifter control voltage (high state)	2.4	3.3	7	V
I_V+	Courant I+ (state 0 and low level)		100		mA
I_V-	Courant I- (state 0 and low level)		23		mA

These values are representative of on board measurements as defined on the drawing at “Evaluation mother board” section.

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Peak Phase Error (PPE) definition

PPE(i) = measured_Phase(S21)@state(i) - measured_Phase(S21)@state(0) - theoreticalPhaseValue@State(i)

Amplitude Variation (Av) definition

Av(i) = Measured_dB(S21)@state(i) - Measured_dB(S21)@state(0)

RMS Peak Phase Error (RMS_PPE) definition

$$\text{RMS\_PPE} = \sqrt{\frac{\sum_{i=0}^{63}(PPE(i)-\overline{PPE})^2}{64}}$$

Where $\overline{PPE} = \frac{\sum_{i=0}^{63} PPE(i)}{64}$

RMS Amplitude variation (RMS_Av) definition

$$RMS\_AV = \overline{Av} = \frac{\sum_{i=0}^{63} Av(i)}{64}$$

Amplitude variation standart deviation (StdDev_Av) definition

$$\text{StdDev\_Av} = 20\log\left(1+\sqrt{\frac{1}{64}.\sum_{i=0}^{63}(1-Av(i)\_lin)^2}\right) \text{ (dB)}$$

The translation of Av(i) from dB to linear is given by: $Av(i)\_lin = 10^{\frac{Av(i)}{20}}$
(i) is in the range [0:63]

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V+	Maximum DC positive supply	+6	V
V-	Maximum DC negative supply	-6	V
Vctrl	Phase shifter control voltage (Vlow Vhigh)	-0.5 +5.5	V
Pin	Maximum peak input power overdrive	+11	dBm
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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Device thermal performances

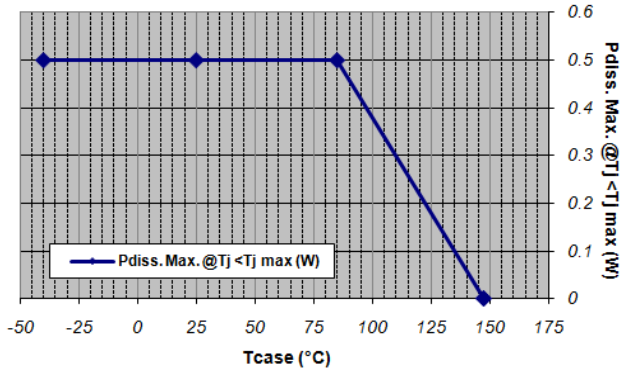
All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

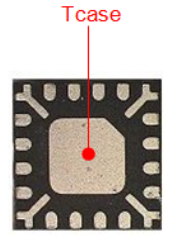
DEVICE THERMAL SPECIFICATION : CHP1102-QGG				
Recommended max. junction temperature (Tj max)			:	147 °C
Junction temperature absolute maximum rating			:	175 °C
Max. continuous dissipated power (Pdiss. Max.)			:	0.5 W
=> Pdiss. Max. derating above Tcase(1)=	85	°C	:	8 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)			:	<124 °C/W
Minimum Tcase operating temperature(3)			:	-40 °C
Maximum Tcase operating temperature(3)			:	85 °C
Minimum storage temperature			:	-55 °C
Maximum storage temperature			:	150 °C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

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Phase Shifter Control Interface

The 6-bit phase shifter is controlled by 6 voltages (A1 to A6). Reference state is “0”. State is “0” when 0V is applied, state is “1” when +3.3V is applied.

State	A1	A2	A3	A4	A5	A6	Phase (deg)
0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	5,625
2	0	1	0	0	0	0	11,25
3	1	1	0	0	0	0	16,875
4	0	0	1	0	0	0	22,5
5	1	0	1	0	0	0	28,125
6	0	1	1	0	0	0	33,75
7	1	1	1	0	0	0	39,375
8	0	0	0	1	0	0	45
9	1	0	0	1	0	0	50,625
10	0	1	0	1	0	0	56,25
11	1	1	0	1	0	0	61,875
12	0	0	1	1	0	0	67,5
13	1	0	1	1	0	0	73,125
14	0	1	1	1	0	0	78,75
15	1	1	1	1	0	0	84,375
16	0	0	0	0	1	0	90
17	1	0	0	0	1	0	95,625
18	0	1	0	0	1	0	101,25
19	1	1	0	0	1	0	106,875
20	0	0	1	0	1	0	112,5
21	1	0	1	0	1	0	118,125
22	0	1	1	0	1	0	123,75
23	1	1	1	0	1	0	129,375
24	0	0	0	1	1	0	135
25	1	0	0	1	1	0	140,625
26	0	1	0	1	1	0	146,25
27	1	1	0	1	1	0	151,875
28	0	0	1	1	1	0	157,5
29	1	0	1	1	1	0	163,125
30	0	1	1	1	1	0	168,75
31	1	1	1	1	1	0	174,375
32	0	0	0	0	0	1	180
33	1	0	0	0	0	1	185,625
34	0	1	0	0	0	1	191,25
35	1	1	0	0	0	1	196,875
36	0	0	1	0	0	1	202,5
37	1	0	1	0	0	1	208,125
38	0	1	1	0	0	1	213,75
39	1	1	1	0	0	1	219,375
40	0	0	0	1	0	1	225
41	1	0	0	1	0	1	230,625
42	0	1	0	1	0	1	236,25
43	1	1	0	1	0	1	241,875
44	0	0	1	1	0	1	247,5
45	1	0	1	1	0	1	253,125
46	0	1	1	1	0	1	258,75
47	1	1	1	1	0	1	264,375
48	0	0	0	0	1	1	270
49	1	0	0	0	1	1	275,625
50	0	1	0	0	1	1	281,25
51	1	1	0	0	1	1	286,875
52	0	0	1	0	1	1	292,5
53	1	0	1	0	1	1	298,125
54	0	1	1	0	1	1	303,75
55	1	1	1	0	1	1	309,375
56	0	0	0	1	1	1	315
57	1	0	0	1	1	1	320,625
58	0	1	0	1	1	1	326,25
59	1	1	0	1	1	1	331,875
60	0	0	1	1	1	1	337,5
61	1	0	1	1	1	1	343,125
62	0	1	1	1	1	1	348,75
63	1	1	1	1	1	1	354,375

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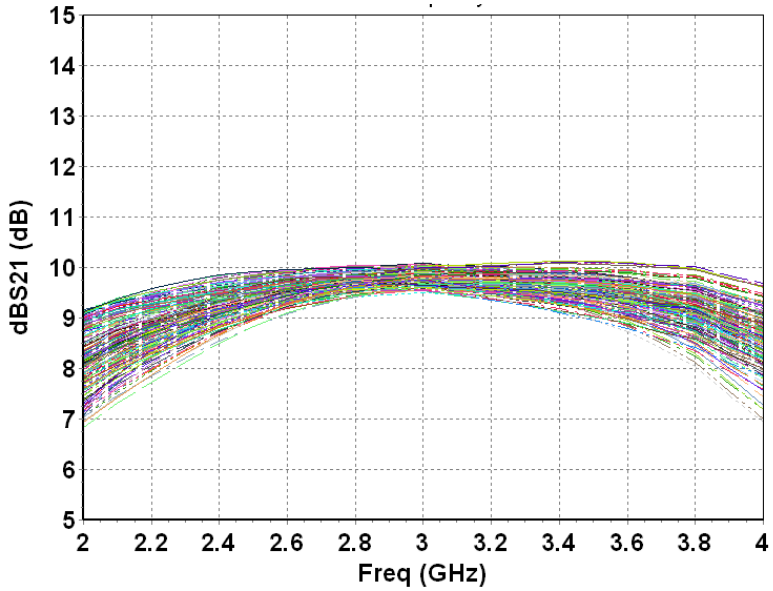
Typical S-parameter results

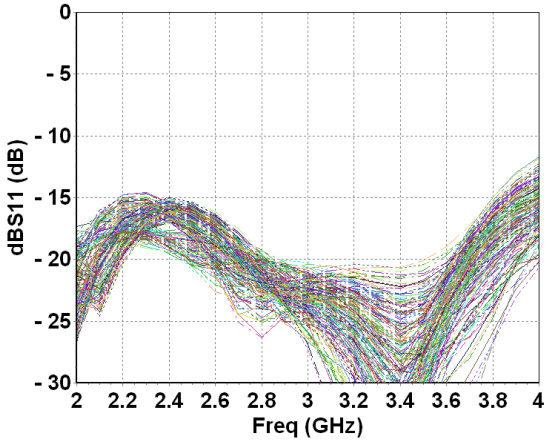
Tamb.= +25°C, V+ = +5V, V- = -5V, packaged device, not de-embedded board measurement (board drawing 97043)

[S] parameters

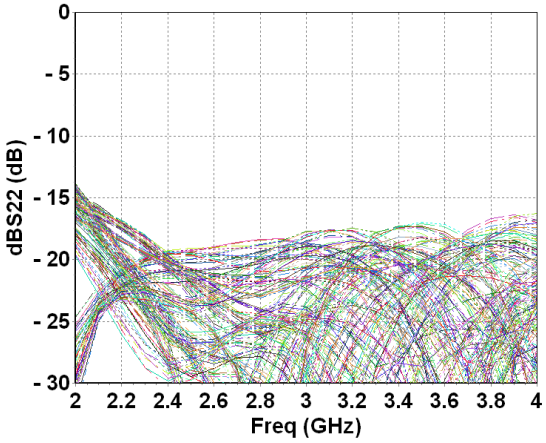
Gain versus Frequency
All phase states.



Input return loss versus. Frequency
All phase states.



Output return loss versus. Frequency
All phase states.



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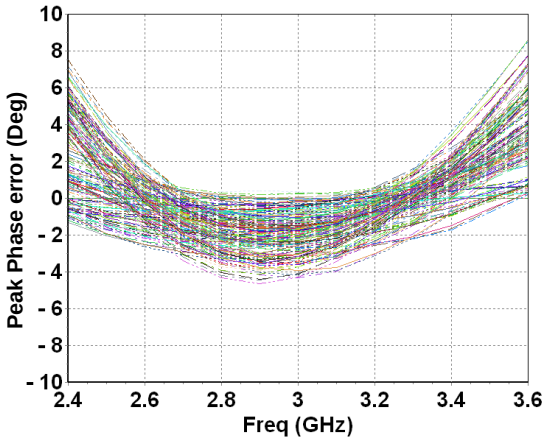
Typical S-parameter results

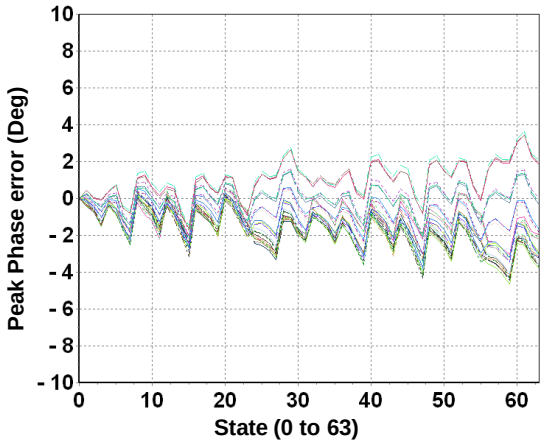
Tamb.= +25°C, V+ = +5V, V- = -5V, packaged device, not de-embedded board measurement (board drawing 97043)

Phase shifter performances: Phase error

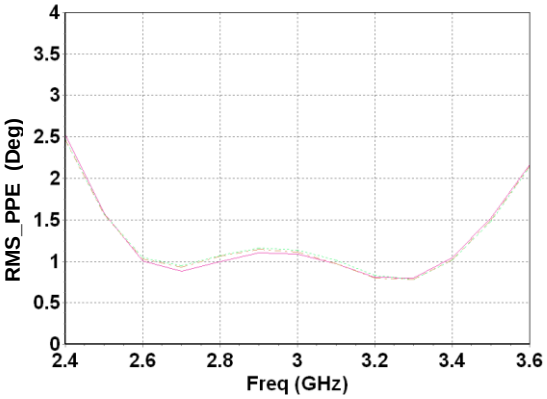
Peak phase error versus frequency (all states)



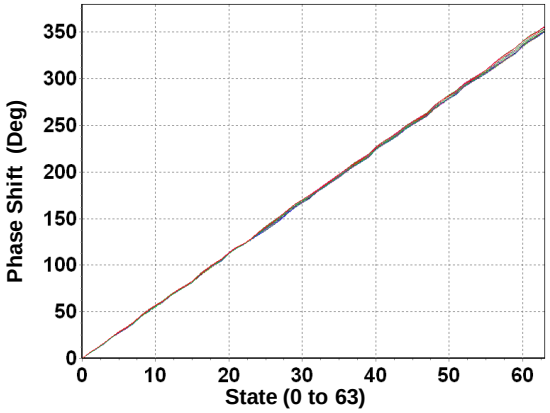
Peak phase error versus state 2.7GHz < frequency < 3.4GHz



RMS phase error versus frequency on 3 boards



Phase shift versus state 2.7GHz < frequency < 3.4GHz



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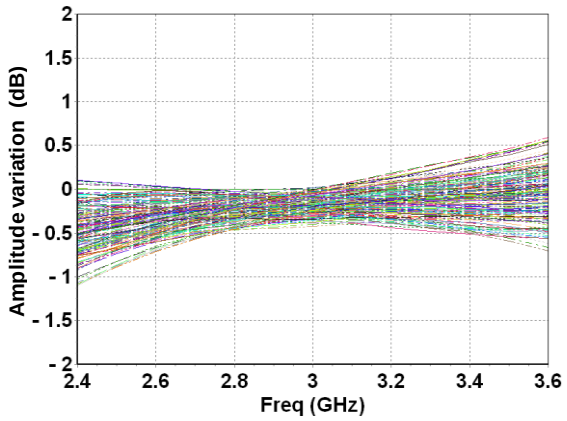
Typical Test Fixture Measurements in Temperature

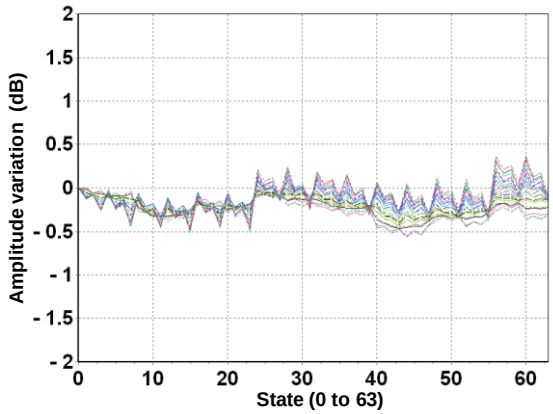
T= [-40, +25, +85] °C, V+ = +5V, V- = -5V, packaged device, not de-embedded board measurement (board drawing 97043)

Phase shifter performances: Amplitude variation

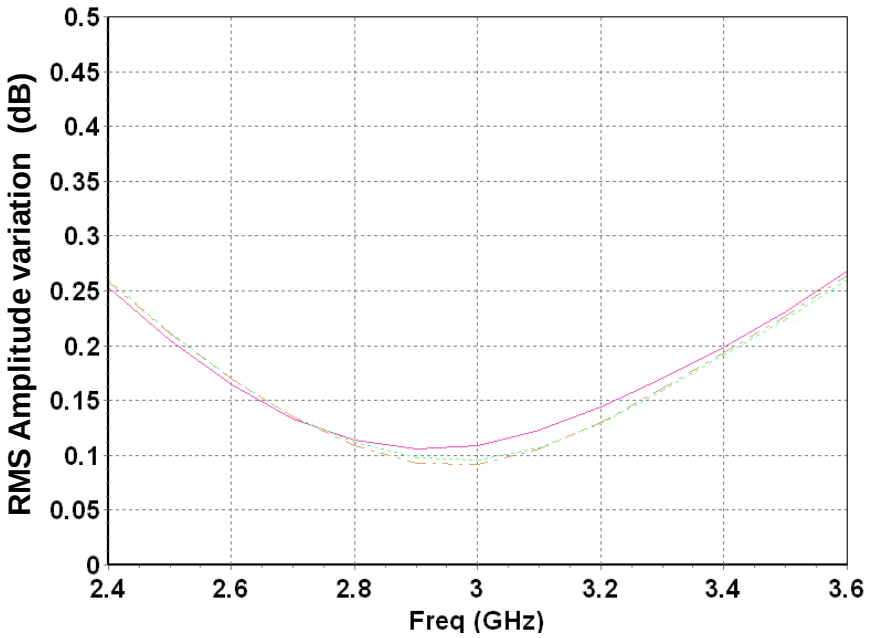
Amplitude variation versus frequency (all states)



Amplitude variation versus state 2.7GHz < frequency < 3.4GHz



RMS Amplitude Variation versus frequency on 3 boards



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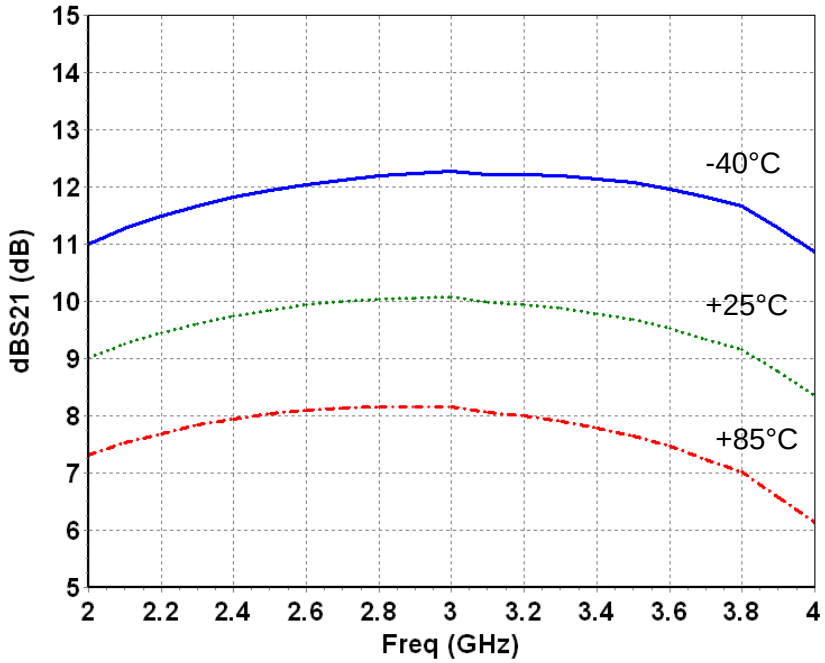
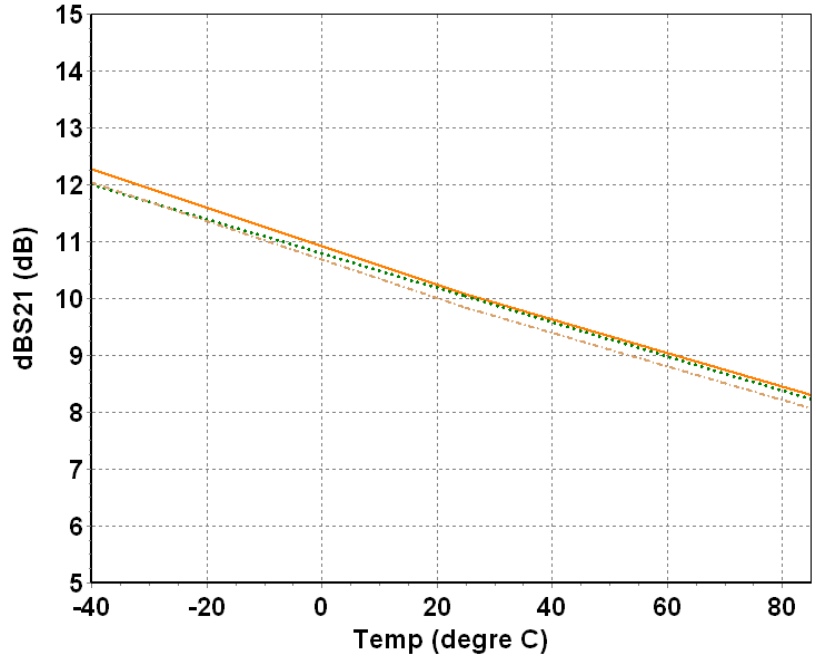
Typical Test Fixture Measurements in Temperature

T= [-40, +25, +85] °C, V+ = +5V, V- = -5V, packaged device, not de-embedded board measurement (board drawing 97043)

Gain versus Frequency
(Phase state 0)



Gain versus Temperature (f=3GHz and Phase state 0) for 3 boards



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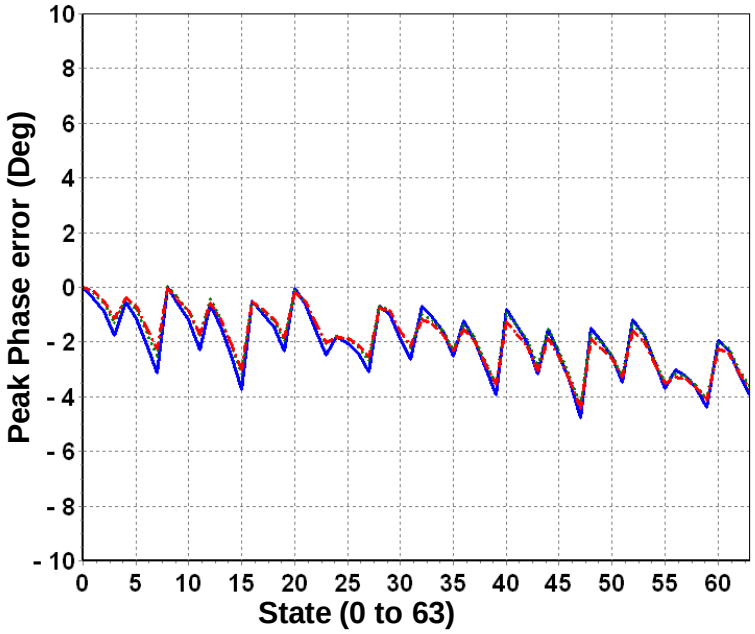
Typical Test Fixture Measurements in Temperature

T= [-40, +25, +85] °C, V+ = +5V, V- = -5V, packaged device, not de-embedded board measurement (board drawing 97043)

Peak phase error versus state and temperature (f = 3GHz)



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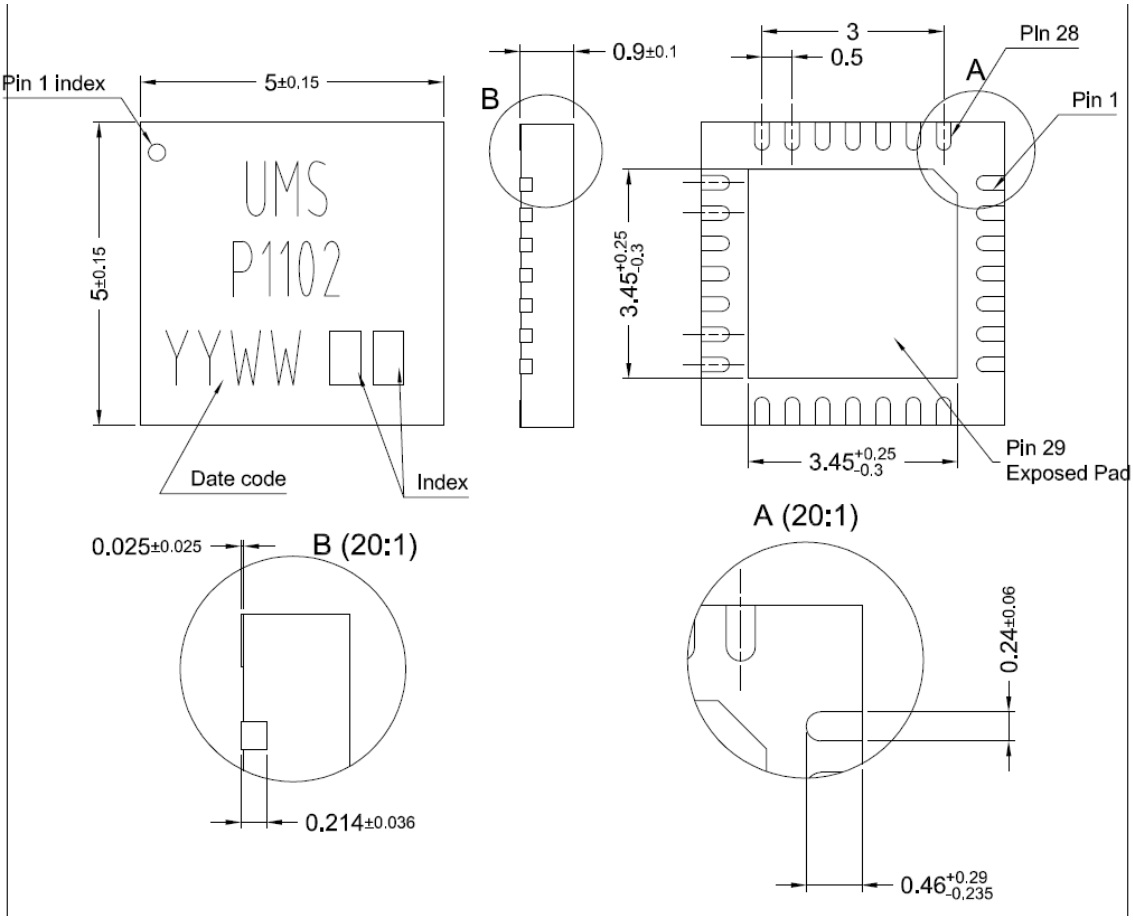
Package outline [1]



Matt tin, Lead Free (Green)		1- Gnd[2]	11- A4	21- Gnd[2]
Units : mm		2- Nc	12- A5	22- Gnd[2]
From the standard : JEDEC MO-220 (VGGD)		3- Gnd[2]	13- A6	23- V-
		4- Gnd[2]	14- V+	24- Nc
29- GND		5- RF in	15- Gnd[2]	25- Nc
		6- Gnd[2]	16- Gnd[2]	26- Nc
		7- Gnd[2]	17- Nc	27- Nc
		8- A1	18- Gnd[2]	28- Gnd[2]
		9- A2	19- Gnd[2]	
		10- A3	20- RF out	

[1] The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.
[2] It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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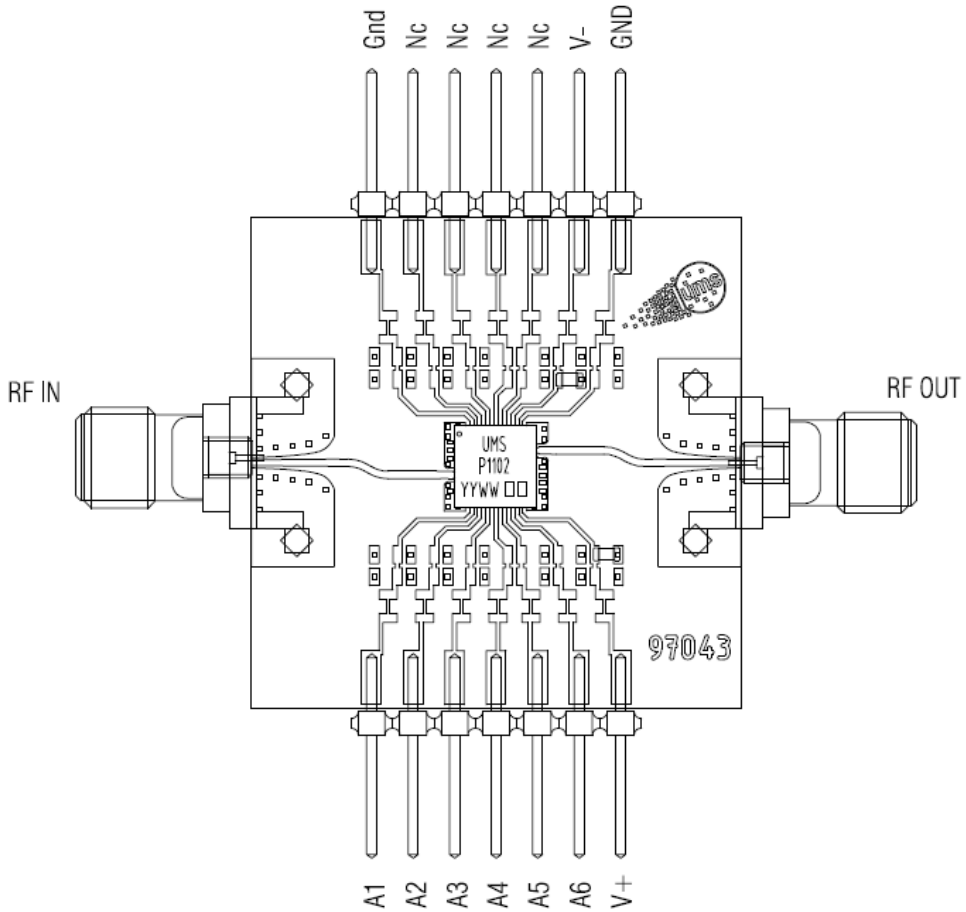
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended implementation for a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- (See application note AN0017 for details).



General Biasing conditions

Pad name	Value	Pad name	Value
V+	+5V	A3	0 or 3.3V
V-	-5V	A4	0 or 3.3V
A1	0 or 3.3V	A5	0 or 3.3V
A2	0 or 3.3V	A6	0 or 3.3V

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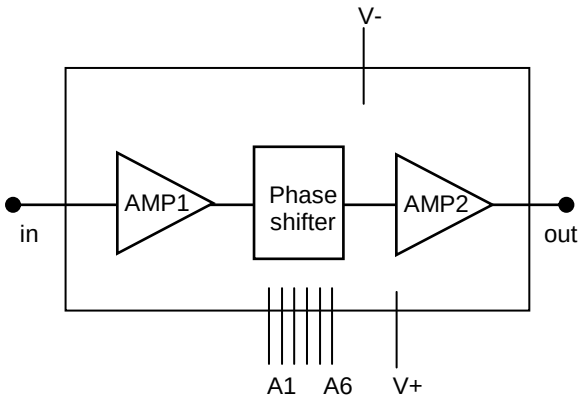
Schematic of the circuit



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 5x5 RoHS compliant package:	CHP1102-QGG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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