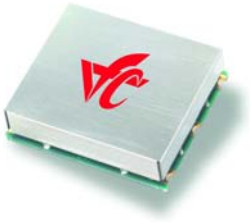
VFJA402
Jitter Attenuator with 3 Input Frequency Selections plus Free Run Mode

Valpey Fisher Corporation
High Frequency, Low Phase Noise Timing Solutions

Features

- Free Run Mode
- 8KHz to 200MHz Input Frequency Range
- Ultra Low Jitter and Phase Noise: -130dBc/Hz @ 1KHz
- Low Power: < 150mW typical



RoHS Status

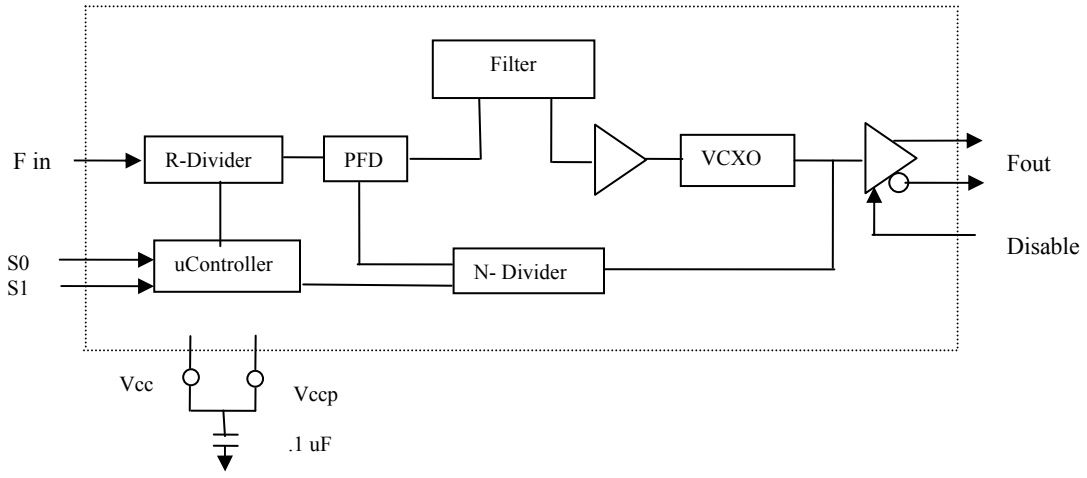
RoHS 6/6

Applications

- Synchronous Ethernet
- Wireless Infrastructure

Description

The VFJA402 is a jitter attenuator capable of providing an output frequency up to 200MHz. Two select inputs [S1,S0] allow the user to select 1 of 3 preset input frequencies or the free run mode. In free run mode the device provides the nominal output frequency and is not phase locked to the input frequency. Operating with a +3.3 volt power supply the device typically consumes 150mW. The output is configured as a differential LVPECL signal and requires external termination resistors. The VFJA402 is available in a 19.5mm x 15.5mm surface mount package.



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Break Down Voltage	Vcc		-0.5		5.5	V	
Storage Temperature	Ts		-55		+105°	°C	

Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Output Frequency Range	Fout		10		200	MHz	
Input Frequency Range	Fin		0.008		200	MHz	See Table 1
Input Level	Vin	AC coupled internally	0.4		3.3	V p-p	Note 2
Output Level Logic "1"	Voh	50 Ohm to Vcc-2V or Thevenin Equivalent	Vcc-0.96		Vcc-0.81	V	
Output Level Logic "0"	Vol		Vcc-1.85		Vcc-1.65	V	
Phase Jitter		12KHz to 20MHz		0.20	0.5	ps(rms)	
SSB Phase Noise	Φn	100Hz 1KHz 10KHz 100KHz		-100 -130 -145 -150		dBc/Hz	@ 155.52MHz
APR			± 32			ppm	
Modulation BW			10			Hz	Note 1
Free run Accuracy		-40 ºC to +85 ºC			+/- 35	ppm	
Duty Cycle		@ 50%	45	50	55	%	
Rise / Fall Time	Tr/Tf	20% to 80%			0.6	ns	
Start up time				2	10	ms	
Supply Voltage	Vcc		3.15	3.30	3.45	V	
Input Current	Icc			45	55	mA	
Operating Temperature Range	Ta		-40°		+85°	°C	
Enable / Disable Function	Input HIGH (>2.5V): Output Disabled (Fout="0"; nFout="1") Input LOW (<0.5V) or floating: Output Enabled						LVCMOS
Enable / Disable Time	Te/Td				100	ns	

Notes:
1. Consult factory for Bandwidth options
2. For Fin < 20 MHz , ensure SR > 50 V/µs
3. For best noise immunity use [S1, S0] = [0, 0]

How to Order

VFJA402 — **Suffix** (See Table 1)

Sample Frequencies **Table 1**

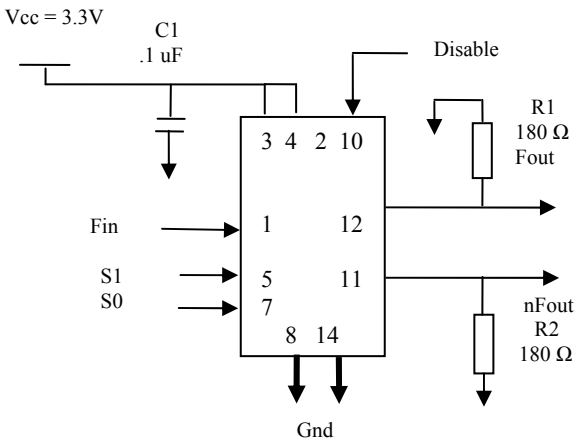
P/N suffix	S1:S0	Input Frequency (MHz)	Output Frequency (MHz)	P/N suffix	S1:S0	Input Frequency (MHz)	Output Frequency (MHz)
-001	00	Free Run Mode	156.25	-002	00	Free Run Mode	155.52
	01	0.008	156.25		01	0.008	155.52
	10	19.44	156.25		10	19.44	155.52
	11	161.1328125	156.25		11	155.52	155.52
-003	00	Free Run Mode	156.25	-004 Note 3	00	25	155.52
	01	161.1328125	156.25		01	25	155.52
	10	19.44	156.25		10	25	155.52
	11	125	156.25		11	25	155.52
-005	00	Free Run Mode	155.52	-006	00	Free Run Mode	156.25
	01	25	155.52		01	25	156.25
	10	100	155.52		10	125	156.25
	11	100	155.52		11	156.25	156.25

Once Input and Output frequencies have been submitted and approved, the Factory will assign a part number.

Environmental and Mechanical

Parameter	Specification
Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A
Vibration	Per MIL-STD-883, Method 2007, Condition A
Soldering Conditions	260°C for 10s max
Hermetic Seal	Leak rate less than $5x10^{-8}$ atm.cc/s of helium (crystal only)

Connection Diagram



Pin #	Description
1	Fin
2	DNC
3	Vccp
4	Vcc
5	S1
6	DNC
7	S0
8	Gnd
9	N/C
10	Disable
11	nFout
12	Fout
13	N/C
14	Gnd

* Connect pin #3 to pin #4 and add .1 uF

Mechanical Outline