MAUC-010506

Up Converter
17.68 - 23.62 GHz

Rev. V1

Features

- Integrates Image Reject (Balanced) Mixer, LO Buffer, LO Doubler, and RF Buffer
- 14 dB Conversion Gain
- 21 dBm Input Third Order Intercept (IIP3)
- -30 dBm (2x) LO Leakage (at RF Port)
- Variable Gain with Adjustable Bias
- Lead-Free 4 mm, 24 Lead QFN Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The MAUC-010506 is an integrated up-converter that has a typical conversion gain of 14 dB, and an image rejection of 25 dBc. The device includes a LO doubler, LO buffer amplifier, and RF buffer amplifier. Variable gain can be achieved by adjusting the bias, with turn-down trajectories optimized to maintain linearity and 2×LO leakage over the gain control range. The output IP3 is 33 dBm at maximum gain.

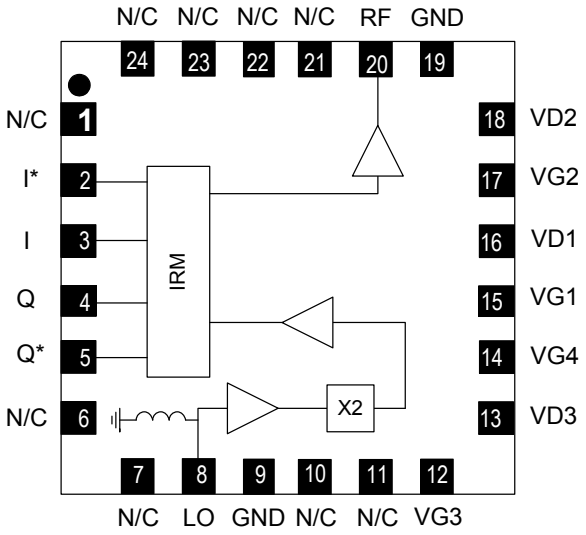
The MAUC-010506 is ideally suited for 18 and 23 GHz band point-to-point radios under both LSB and USB operation.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using an efficient pHEMT process.

Ordering Information

Part Number	Package
MAUC-010506-TR0500	500 Piece Reel
MAUC-010506-000SMB	Sample Board

Functional Schematic



Pin Configuration [1]

Pin No.	Function	Pin No.	Function
1	N/C	13	VD3
2	I*	14	VG4
3	I	15	VG1
4	Q	16	VD1
5	Q*	17	VG2
6	N/C	18	VD2
7	N/C	19	GND
8	LO	20	RF
9	GND	21	N/C
10	N/C	22	N/C
11	N/C	23	N/C
12	VG3	24	N/C
		25	Paddle[2]

1. For optimum RF performance, all N/C's should be terminated to ground.
2. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

• **North America** Tel: 800.366.2266 / Fax: 978.366.2266
• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Up Converter
17.68 - 23.62 GHz

Electrical Specifications[3]:
LO = 0 dBm, IF = -10 dBm, VD = 4 V, ID1 = 90 mA, ID2 = 90 mA, ID3 = 160 mA, T_A = 25°C

Parameter	Units	Min.	Typ.	Max.
Frequency Range (RF)	GHz	17.68	-	23.62
Frequency Range (LO)	GHz	7.09	-	13.56
Frequency Range (IF)	GHz	DC	-	3.5
LO Input Power (PLO)	dBm	-	0	-
Conversion Gain	dB	12	14	16.5
Image Rejection	dBc	-	25	-
Input IP3	dBm	-	21	-
Output IP3 (Pin = -10 dBm/tone)	dBm	29	35	-
Spurious (2xLO) [tuned]	dBm	-	-30	-
Spurious (1xLO)	dBm	-	-60	-
Current, Drain 1 (ID1)	mA	-	90	-
Current, Drain 2 (ID2)	mA	-	90	-
Current, Drain 3 (ID3)	mA	-	160	-
Gate Voltage (VG4)	V	-	-3	-
Gate Current (IG4)	mA	-	4.0	-

3. Apply gate voltages prior to drain voltages. Adjust VG1, VG2 and VG3 between –1.0 and –0.1 V to achieve specified drain current. Typical current, 340 mA = 90 (ID1) + 90 (ID2) + 160 (ID3). Refer to App Note [1] for biasing details.

Absolute Maximum Ratings [4,5,6]

Parameter	Absolute Max.
Drain Voltage	+4.3 V
Gate Bias Voltage (VG1,2,3)	-1.5V < VG < 0V
Gate Bias Voltage (VG4)	-4.0V < VG < 0V
Input Power	+10 dBm
LO Input Power	+13 dBm
Storage Temperature	-55°C to +150°C
Operating Temperature	-40°C to +85°C
Junction Temperature	150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. MACOM does not recommend sustained operation near these survivability limits.
6. Operating at nominal conditions with $T_J \leq 150°C$ will ensure MTTF > 1 x 10^6 hours.

Handling Procedures

Please observe the following precautions to avoid damage:

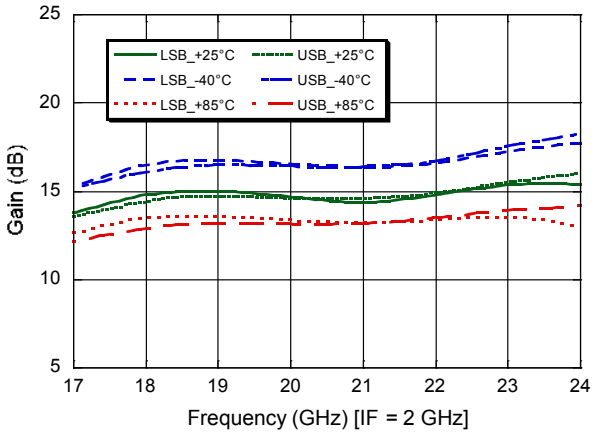
Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these static sensitive devices.

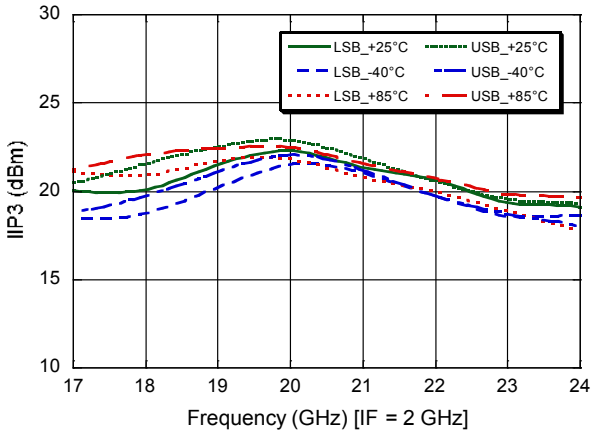
• **North America** Tel: 800.366.2266 / Fax: 978.366.2266
• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Typical Performance Curves: LO = 0 dBm, IF = -10 dBm/tone, Pdc = 1.5 W

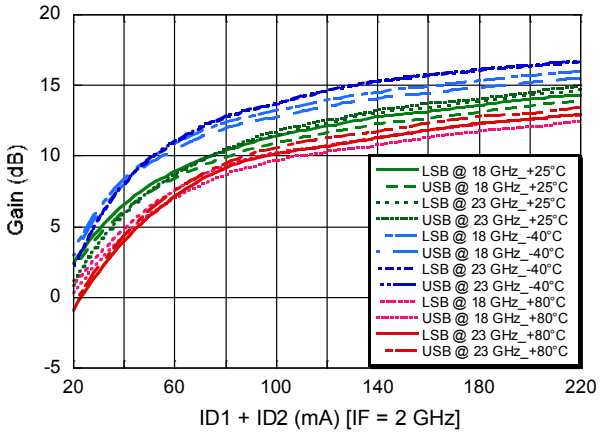
Conversion Gain



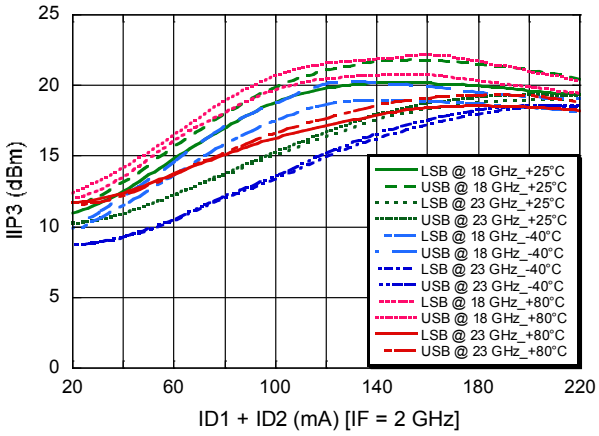
Input IP3



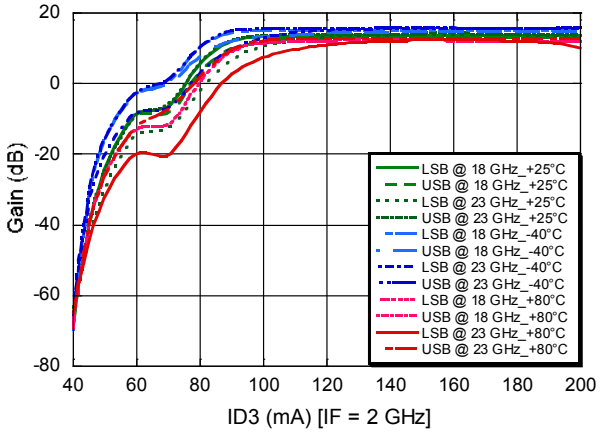
Conversion Gain



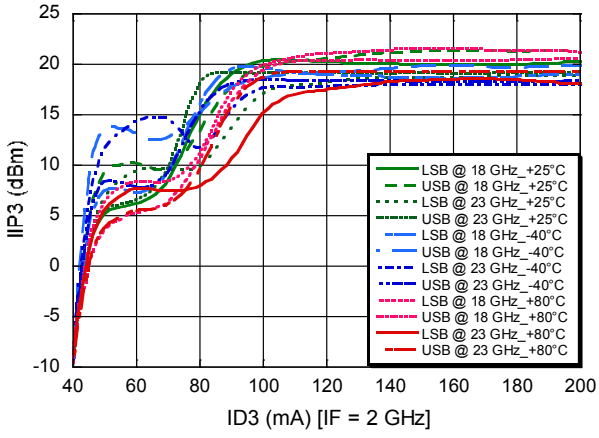
Input IP3



Conversion Gain



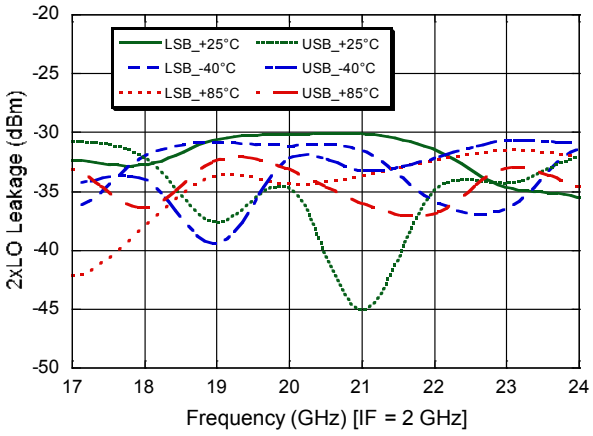
Input IP3



- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Typical Performance Curves: LO = 0 dBm, IF = -10 dBm/tone, Pdc = 1.5 W

2xLO Leakage



LO Leakage

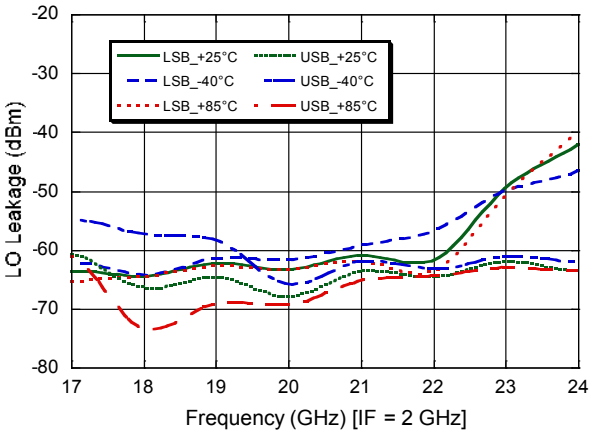
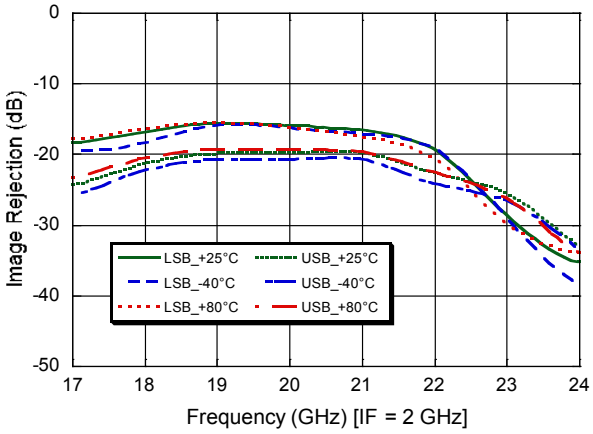


Image Rejection

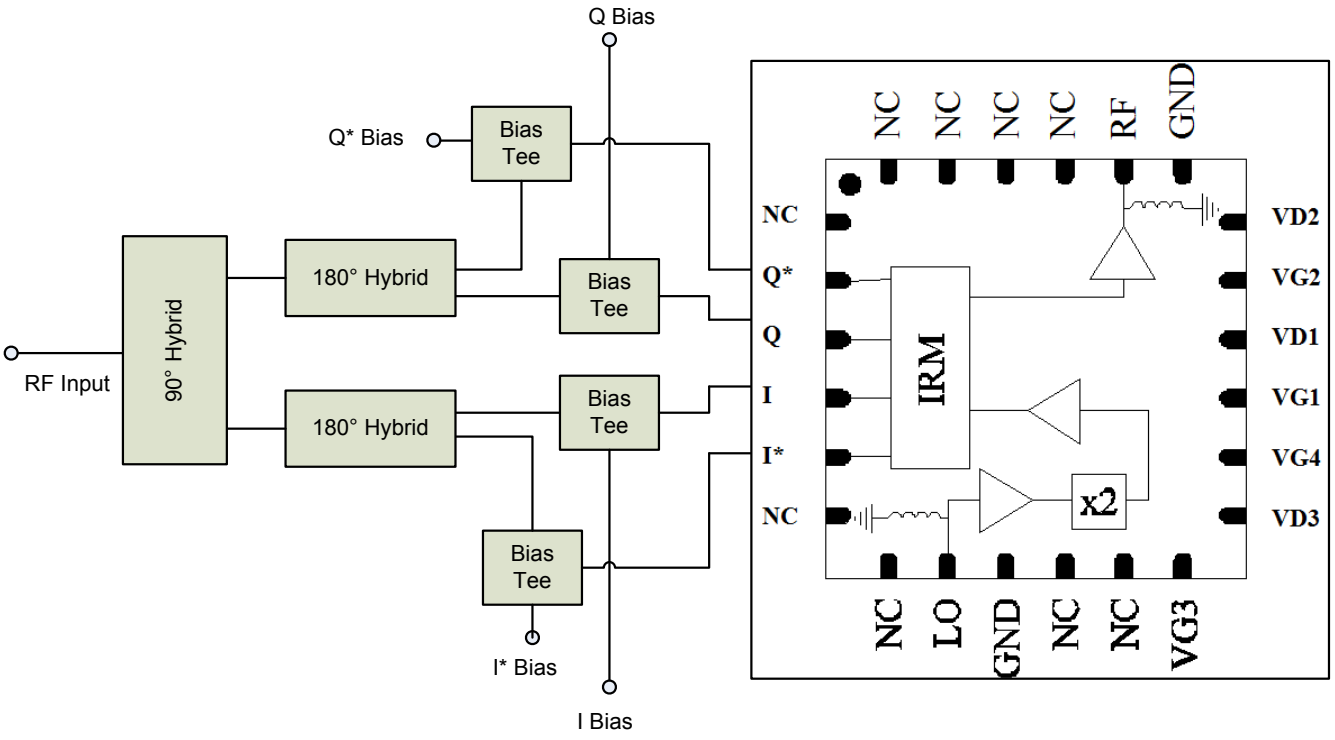


App Note [1] Biasing -

MAUC-010506 is operated by biasing Vd1, Vd2, and Vd3 at 4.0 V. The corresponding drain currents are set to 90 mA, 90 mA, and 160 mA respectively. Vg4 requires a fixed voltage bias of nominally -3 V. It is recommended to use active bias on Vg1, Vg2, Vg3 to keep the currents in Vd1, Vd2, and Vd3 constant, in order to maintain the best performance over temperature. Depending on the supply voltages available and the power dissipation constraints, the bias circuits may include a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply to sense the current. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] I/Q versus I*/Q* -

The IF input to the typical configuration is through a 90° hybrid coupler. The hybrid splits the IF input into inphase and quadrature phase components which feed into two 180° hybrid couplers splitting into 4 signals. These 4 signals enter the MAUC-010506 on I/I*, Q/Q* IF inputs. For highest gain, best image rejection and lowest noise figure, all of the 4 IF inputs should be used.

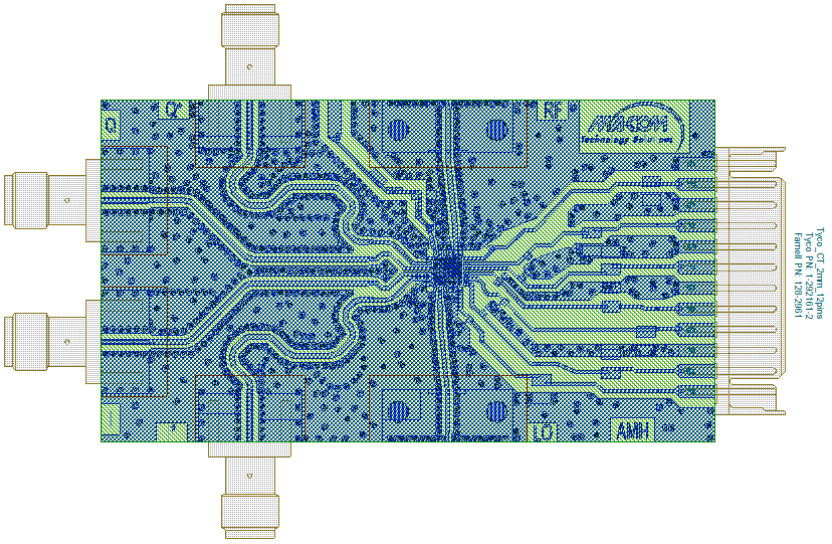


- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

App Note [3] Board Layout -

As shown in the recommended board layout, it is recommended to provide 100 pF decoupling capacitors as close to the bias pins as possible. Additional 10 nF and 1 µF on each of the bias lines are recommended placed a distance further away.

Recommended Board Layout



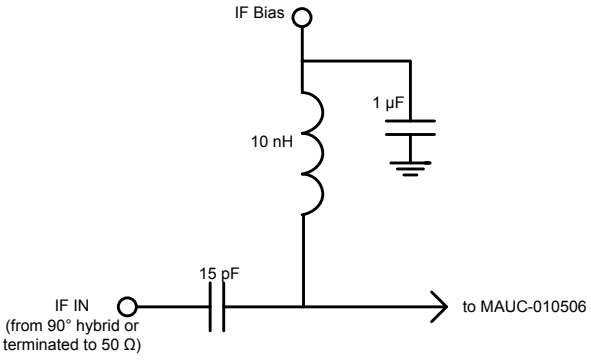
App Note [4] IF Bias -

To obtain optimum 2xLO leakage performance, tuning is achieved by adjusting the DC bias on each of the IF inputs (I, Q, I*, Q*). DC bias is implemented by adding simple bias tees to each of the four IF ports. The diagram below shows a typical bias tee design used.

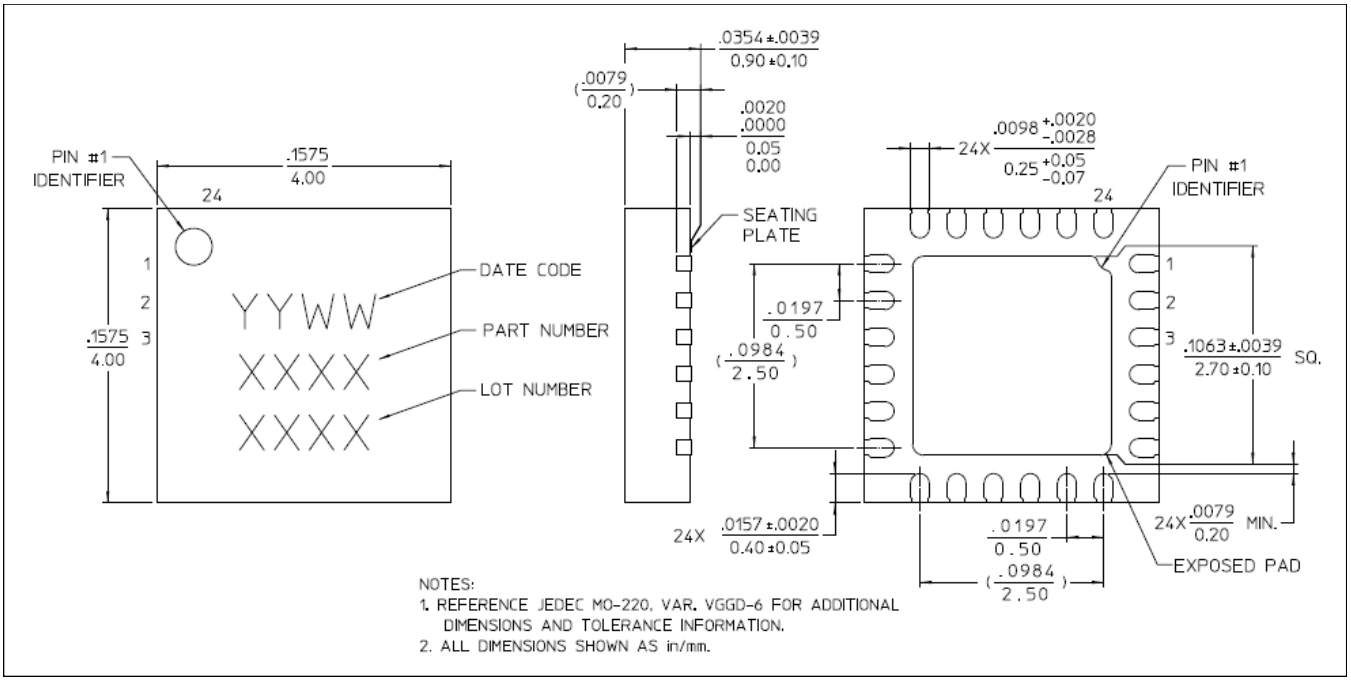
If the I and Q ports are used for the IF input, the I* and Q* ports are DC biased and terminated into 50 Ω. A typical tuning arrangement is to apply a fixed 0.3 V DC bias to both the used IF input ports: I, Q. The remaining two IF ports which have been terminated to 50 Ω tuning independently for minimum 2xLO leakage.

For minimum 2xLO leakage in a system, it may be necessary to correct the IF DC bias for different frequency and temperature conditions. This can be implemented by calibration and offset tables stored in memory, and used to control IF bias over all practical conditions.

Typical Configuration



Lead-Free 4 mm 24-Lead PQFN †



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is NiPdAuAg.

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298