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Altera-Lime Tool Kit Manual

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Altera Development Kit and Universal Wireless Communication Toolkit Connectivity

This chapter defines essential mechanical connection between Altera development kit and Universal Wireless Communication Toolkit (UWCT) board. The following sections describes connection and its associated features.

1.1 Basic connection

The Universal Wireless Communication Toolkit connects to Altera development kit via high speed mezzanine connector (HSMC). Once everything is connected, please see picture below, digital data exchange between the two boards can be enabled.

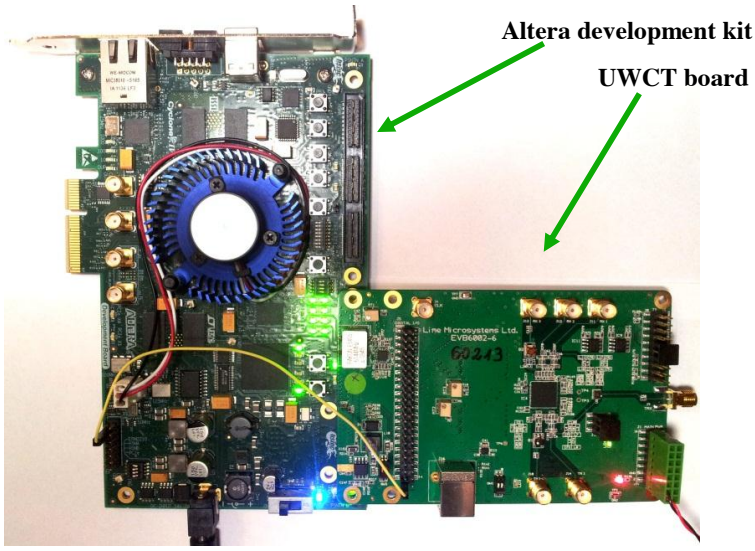


Figure 1 Altera development kit and UWCT board connection.

1.2 HSMC connector on UWCT board

The embedded HSMC connector to UWCT board enables connection to Altera family of FPGA development kits. The connector location on board is shown below.

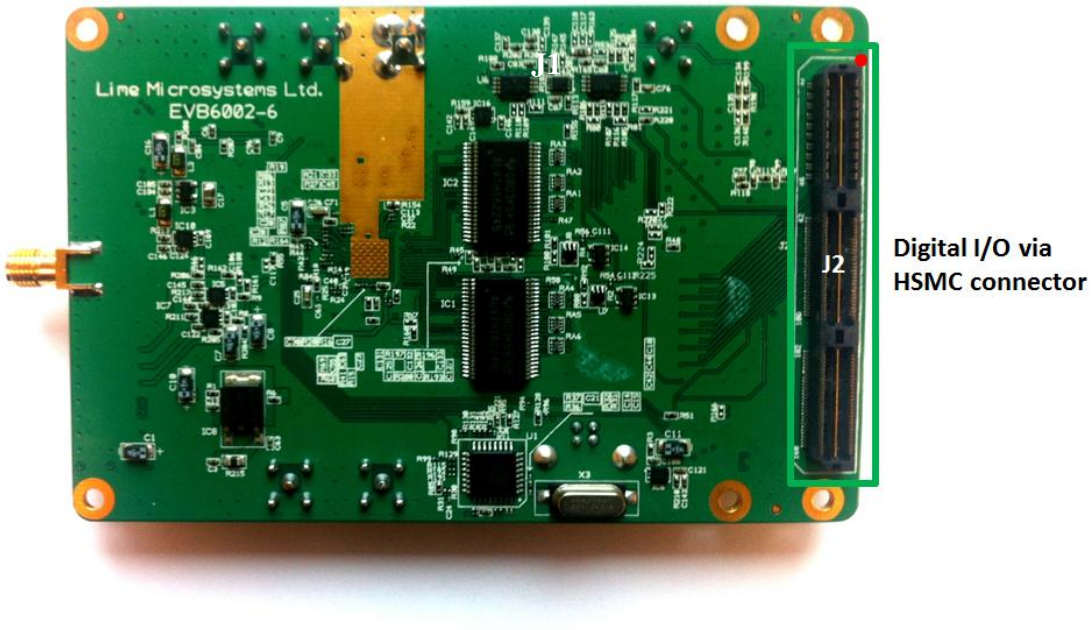
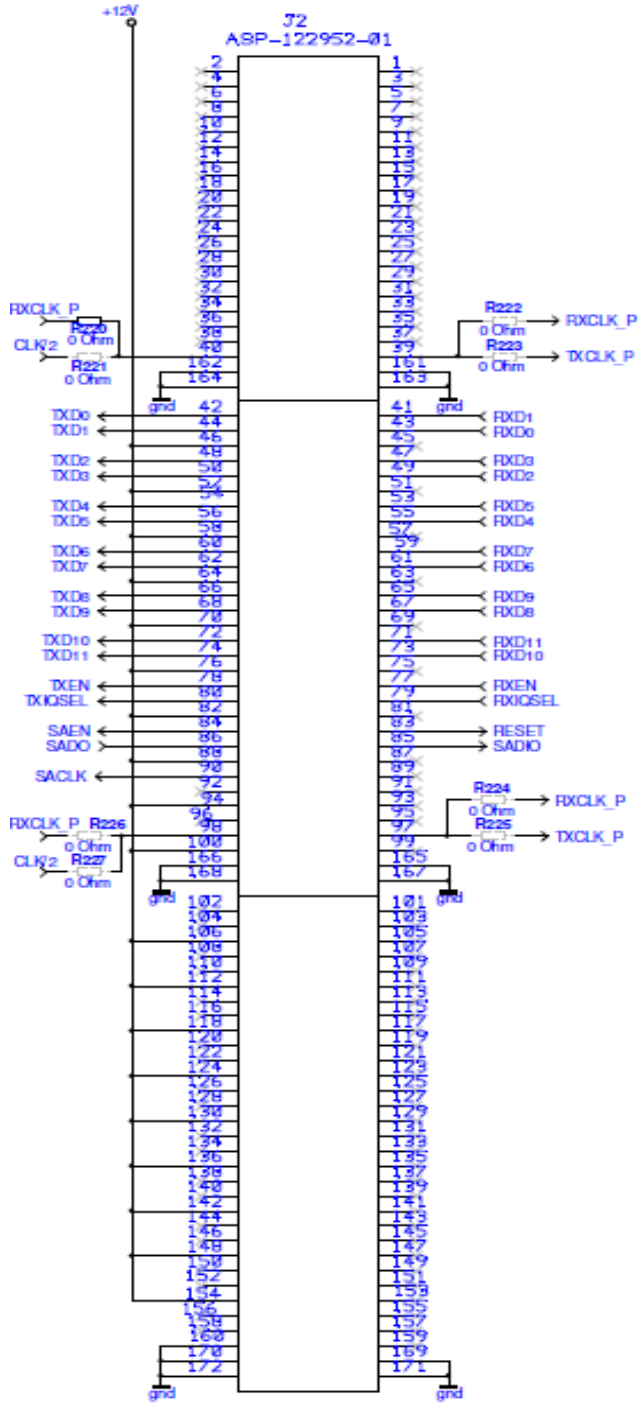


Figure 2: The UWCT board bottom view. The HSMC connector marked as J2.

1.2.1 J2 - Third Party Baseband Board Connector

The HSMC is a standard connector used by Altera development kit.



The HSMC (ASP-122952-01) is a standard connector used to interface the UWCT board directly to Altera design kit. Please note: Specific configuration settings, using 0 Ω resistors on the Lime design kit may need to be changed before connection to a baseband board, see section 3.5.

Figure 3 Connector J2 circuit diagram.

1.3 Clock configurations for Adaptor board

Altera development kit has various options to supply or to expecting clock for digital interface. The Lime design kit was also implemented with this in mind. There are three different clock options for Altera on the Lime board:

Option 1 – clock for Tx and Rx interface is supplied from Lime board.

Option 2 – clock for Tx and Rx is supplied from Altera development kit.

Option 3 – Clock is supplied from Lime Board to Altera kit, divided by internal divider and supplied back to Lime Tx and Rx via digital interface. This feature enables Altera kit to have fractional frequency sampling clock.

Altera development kit adopted clocking options			
	Option 1	**Option 2**	**Option 3**
	Default mode		
Rx data clock	From UWCT Board	To UWCT Board	Input from digital I/O card
Tx data clock	From UWCT Board	To UWCT Board	Input from digital I/O card
Design kit	**Component fit option 1**	**Component fit option 2**	**Component fit option 3**
Board clocking distribution	Option 1	Option 3	Option 3
R224	NF	NF	0R
R225	0R	0R	0R
R226	0R	0R	NF
R227	NF	NF	0R
R147	NF	NF	0R
R81	NF	0R	0R
R80	NF	0R	0R
R105	0R	NF	NF
R106	0R	NF	NF
R114	0R	NF	NF
R116	0R	NF	NF

Table 1 UWCT with Altera Clocking Schemes

2

Demo Project for Altera Development Kit

This chapter describes basics for setting up the Altera kit with Lime EVB and making tests.

2.1 NCO for Transmit Data Generation

The purpose of the Numerically Controlled Oscillator (NCO) implementation is to give a starting point for the user to verify the interconnection between Lime EVB6002-5 Evaluation board and Altera's Stratix IV GX 530 FPGA Development Kit.

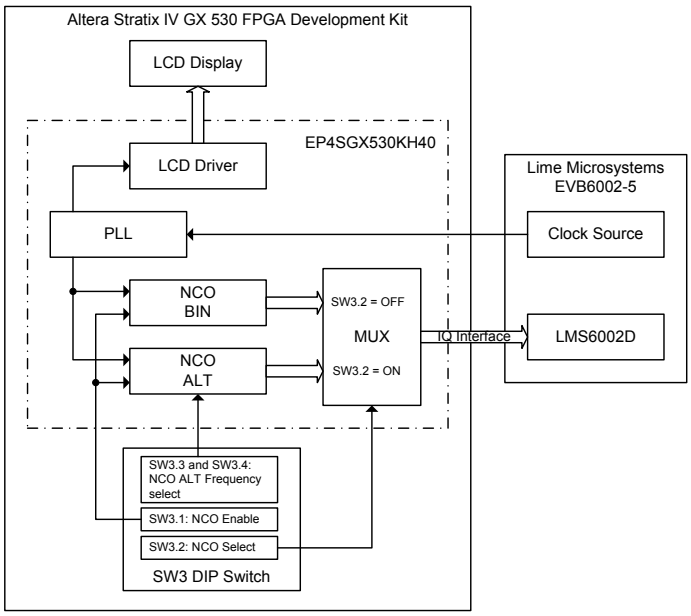


Figure 4 Test Project Block Diagram

Block diagram of the example test system is shown in Figure 9. There two continuous wave (CW) data sources implemented in this example to feed LMS6002D I and Q DACs (IQ interface) and test the transmitter chain:

- NCO BIN: Sine and cosine are approximated by the sequence 0,1,0,-1 for sine and by 1, 0, -1, 0 for cosine;
- NCO ALT: Sine and cosine are generated using Altera's NCO MegaCore IP component [1].

Clock source from the EVB6002-5 Evaluation board (which is 30.72MHz) feeds the DACs within the LMS6002D chip as well as feeding the PLL inside of the FPGA. PLL generates required clocks for both NCOs. Infact, PLL does not alter frequency, it just phase shifts the waveform by 180 degrees to have proper alignment of generated IQ interface data to the external clock, as shown in Figure 10.

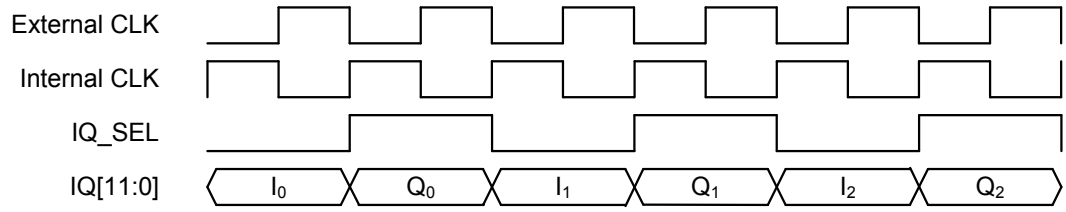


Figure 5 IQ Interface Data Align to the External Clock

There are a few NCO configuration options implemented. Key components used from the Altera's Stratix IV GX 530 FPGA Development Kit are shown in Figure 11.

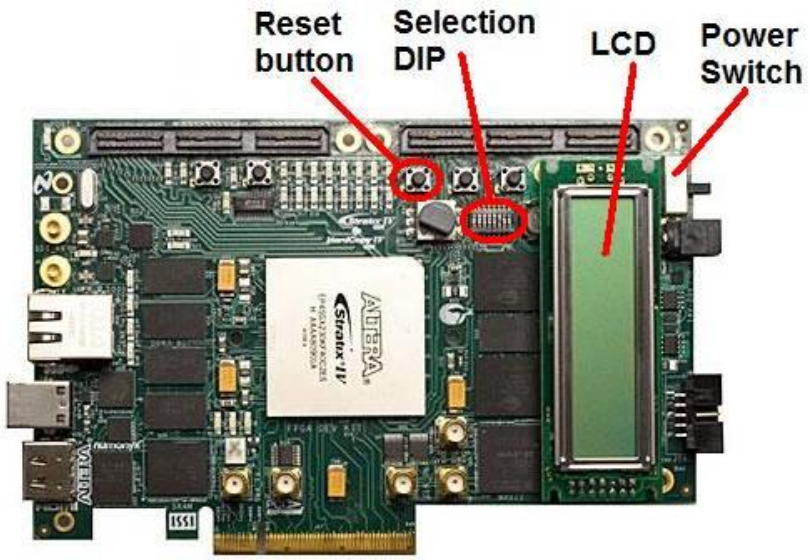


Figure 6 Key Components on Altera Stratix IV GX 530 FPGA Development Kit

Reset button (S3) will reset internal FPGA modules to the initial states. LCD two line alphanumeric display shows "Lime Micro: NCO ver: 1.00" when project is loaded to the

FPGA (please refer to section 2.1.1). Selection DIP switch (SW3, see Figure 11 and Figure 12) is used to control the NCOs.

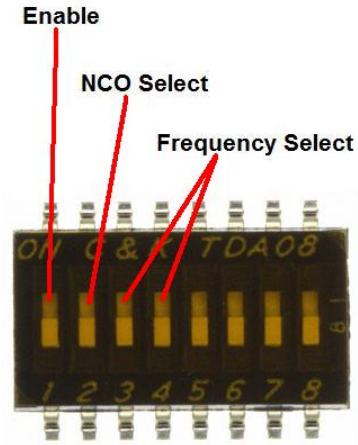


Figure 7 Selection DIP Used for NCO Control

NCO enable is controlled by selection of the DIP switch SW3.1 as described in table 3.

SW3.1 Position	Description
ON	NCO is enabled
OFF	NCO is disabled

Table 2 Enable Control of the NCO

Active NCO is selected by selection of the DIP switch SW3.2 as described in table 4.

SW3.2 Position	Description
ON	NCO ALT is selected
OFF	NCO BIN is selected

Table 3 Selection of the NCO

NCO ALT output frequency is controlled by selection of the DIP switches SW3.3 and SW3.4 as described in table 5. This enables user to choose from four different frequencies:1 MHz, 2MHz, 4 MHz and 8 MHz.
Frequency of NCO BIN is fixed to the 3.84MHz (this is input clock from Lime EVB6002-5 evaluation board divided by 8, i.e. 30.72MHz/8).

SW3.3 Position	SW3.4 Position	NCO ALT Output frequency
OFF	OFF	1MHz
OFF	ON	2MHz
ON	OFF	4MHz
ON	ON	8MHz

Table 4 Frequency Selection of the NCO ALT

Data from the selected NCO are fed to the Lime EVB6002-5 evaluation board.

2.1.1 Extracting Quartus II NCO project

NCO project supplied is archived using Quartus II (for extracting please use Quartus II program). Use command "Project ¬-> Extract Archived Project…" from Quartus II menu to extract supplied project. After this command window appears, select supplied project archive file lm_evb_ae_v1.00.qar as "Archive name:", choose desired folder where to extract as "Destination folder:" and press OK. Project will be open automatically after extraction.

There is compiled bit stream file in the extracted folder already, so no need to compile the project if you do not make any changes in the initial project. Just download (see "FPGA Programming over Embedded USB-Blaster" chapter for reference) "lm_evb_ae.sof" file from extracted archive to the FPGA.

2.1.2 Spectrum of the Transmitter

After configuring FPGA and LMS6002D (setup for LMS6002D is described in detailed in Quick Starter Manual for EVB), the spectrum of transmitter output can be measured.
Spectrum of the transmitter output when NCO BIN selected is shown in Figure 13. Switch SW3 is configured as follows:

- SW3.1 – ON
- SW3.2 – OFF

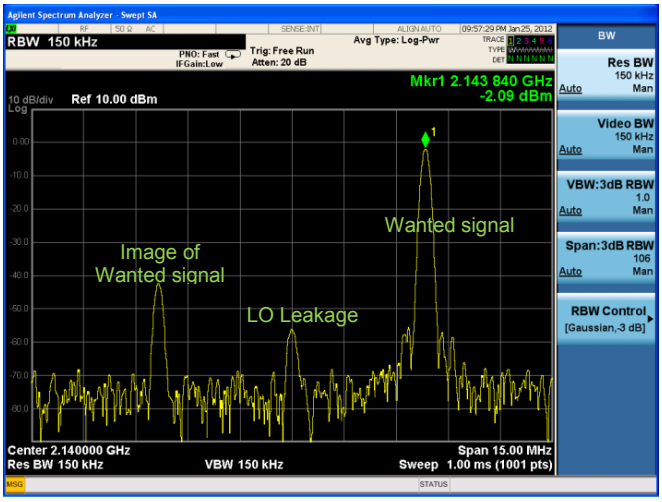


Figure 8 Transmitter Output, when NCO BIN is Selected

Spectrum of the transmitter output when NCO ALT selected is shown in Figure 14.
Switch SW3 is configured as follows:

- SW3.1 – ON
- SW3.2 – ON
- SW3.3 – ON
- SW3.4 – OFF

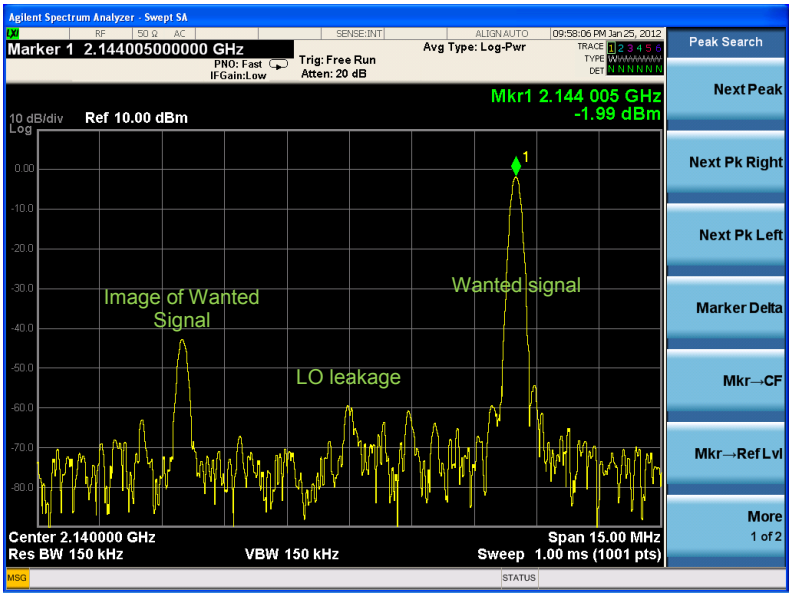


Figure 9 Transmitter Output, when NCO ALT 4MHz is Selected

The wanted signal is appears to be with the selected offset from the local oscillator (LO) frequency. Wanted signal image as well as LO leakage appears in the spectrum, while no IQ phase/gain error correction and LO calibration is applied.

2.2 FPGA Programming over Embedded USB-Blaster

It is possible to configure FPGA device from computer, as described in reference [2], page 6-24, chapter "Configuring the FPGA Using the Quartus II Programmer":

The Quartus II Programmer can be used to configure the FPGA with a specific *.sof file. Before configuring FPGA, ensure that the Quartus II Programmer and the USB-Blaster driver are installed on the host computer. USB cable must be connected to the FPGA development board, the board is power on and no other applications that uses JTAG chain is running. To configure the Stratix IV GX FPGA please perform the following steps:

- Start the Quartus II Programmer.
- Click Add File and select the path to the desired .sof.
- Turn on the Program/Configure option for the added file.
- Click Start to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

The window view of the Quartus II Programmer is shown in Figure 10. This view indicates successful configuration of FPGA.

After Quartus II Programmer is started please ensure that there is "USB-Blaster [USB-0]" line at the right of "Hardware Setup…" button. If the line indicates "No Hardware" instead, press "Hardware Setup…" button. Select "USB-Blaster [USB-0]" from the "Currently selected hardware:" drop-down list. If the drop-down list does not contain USB-Blaster, make sure you have connection between the PC and the board; please ensure that the driver is installed.

It is necessary to check if "Mode:" is set to "JTAG" in the Quartus II Programmer window. Choose JTAG, if any another mode is selected.

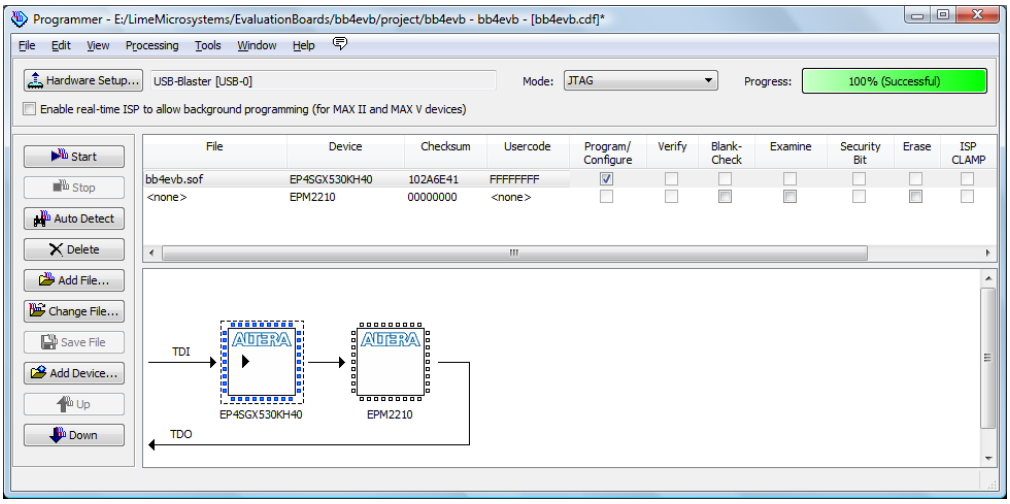


Figure 10 View of the Quartus II Programmer

3

References

[1] NCO MegaCore Function User Guide:
http://www.altera.com/literature/ug/ug_nco.pdf

[2] Information about setting up the Stratix IV GX FPGA development board, 530 edition and using the included software:
http://www.altera.com/literature/ug/ug_sivgx_fpga530_dev_kit.pdf

[3] Detailed information about board components and interfaces:
http://www.altera.com/literature/manual/rm_sivgx_fpga530_dev_board.pdf