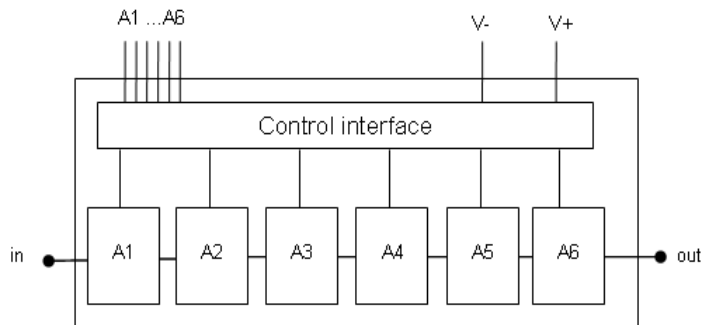


Advance Information

DC-6GHz 6-BIT DIGITAL ATTENUATOR

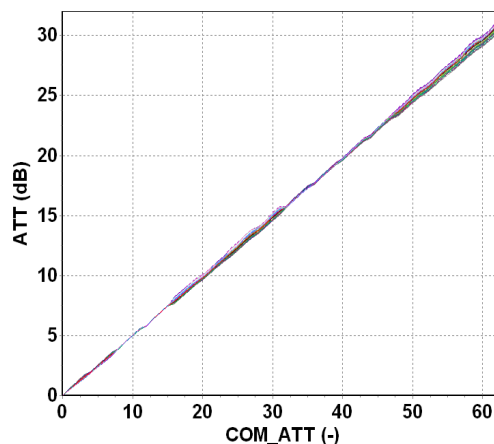
GaAs Monolithic Microwave IC



UMS is developing a DC-6GHz monolithic 6 bit digital attenuator with a LSB = 0.5dB offering a high dynamic range and a high accuracy, the RMS amplitude error is lower than 0.5dB. The circuit provides low insertion loss 2.5dB associated to input and output return losses better than 13dB. A CMOS and TTL compatible interface is available on chip.

The circuit is mainly dedicated to defence and space systems and is also well suited for a wide range of microwave applications and systems.

It is developed on a 0.25 μ m gate length pHEMT process. It is available as a bare die and soon in a standard surface mount 24 leads QFN4x4 compliant with the Restriction of Hazardous Substances (RoHS) European Union directive 2002/95/EC.

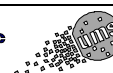


Attenuation versus attenuator state
from DC to 6GHz

Main Characteristics at room temperature

T= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Operating frequency	DC		6	GHz
IL	Insertion Loss		2.5		dB
S11	Input Return Loss		-15		dB
S22	Output Return Loss		-13		dB
P1dB	Input power at 1dB gain compression		20		dBm
Dyn	Dynamic		31.5		dB
LSB	Attenuator elementary step		0.5		dB
Att_er	Attenuation error		- 0.7/+0.4		dB
Rms_att_er	RMS attenuation error		0.3		dB
Phivar	Phase variation		-2 / +3		°
Rms_phivar	RMS phase variation		0.6		°
V+	Positive supply voltage		5		V
V-	Negative supply voltage		-5	-4	V
Vctrl_L	Control voltage low level		0	0.4	V
Vctrl_H	Control voltage high level	2.4		7	V
I_V+	Positive supply DC current		5		mA

Advanced Information

Absolute Maximum Ratings (1)

T= +25°C

Symbol	Parameter	Values	Unit
V+	Maximum positive bias voltage	8	V
V-	Minimum negative bias voltage	-8	V
Ai	CTRL voltage (Vctrl_low, Vctrl_high)	-2, 8	V
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

- (1) Operation of this device above anyone of these parameters may cause permanent damage.

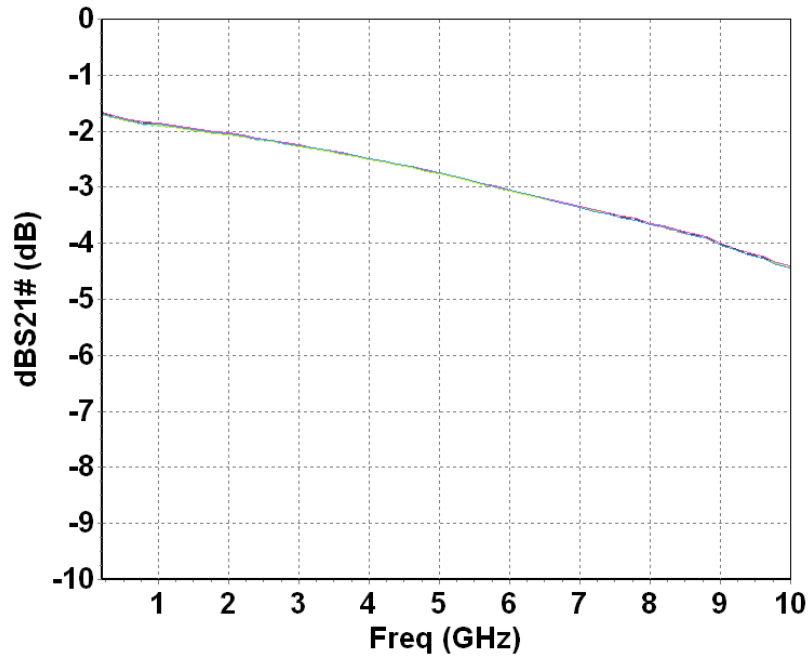
Advanced Information

Typical Measurements

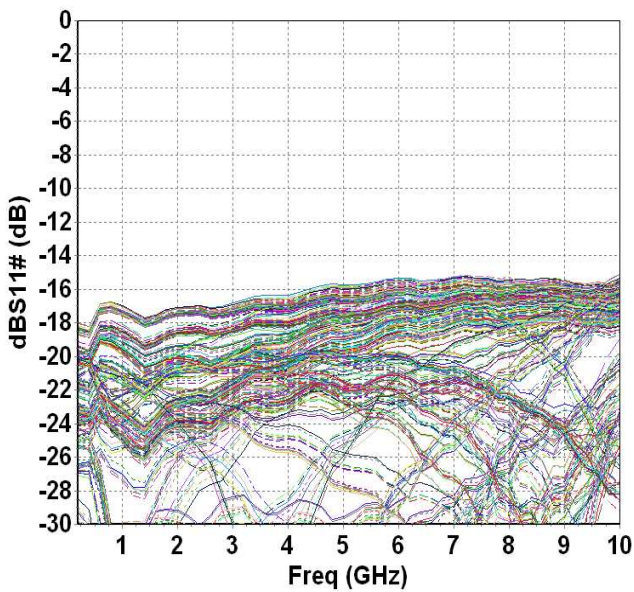
T= +25°C

[S] parameters

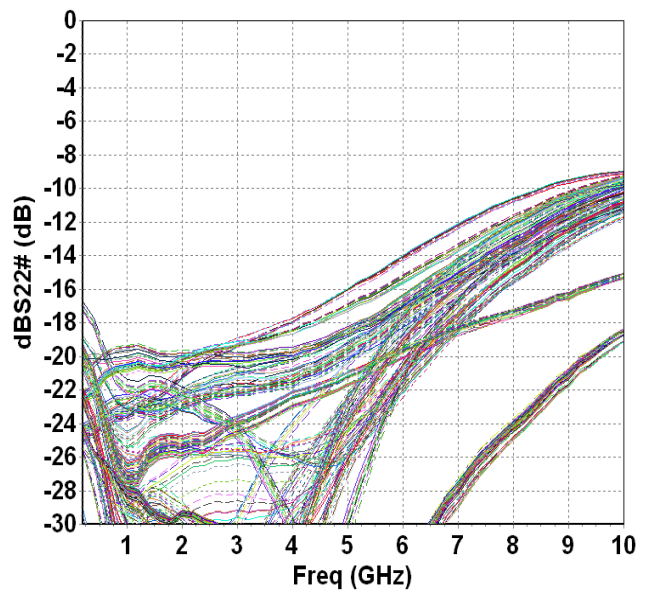
S21 vs. Frequency
Attenuator state 0



S11 vs. Frequency
All attenuator states



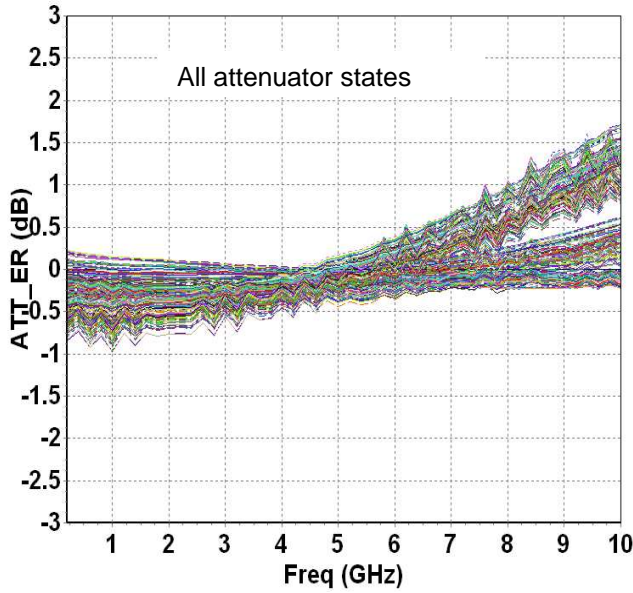
S22 vs. Frequency
All attenuator states



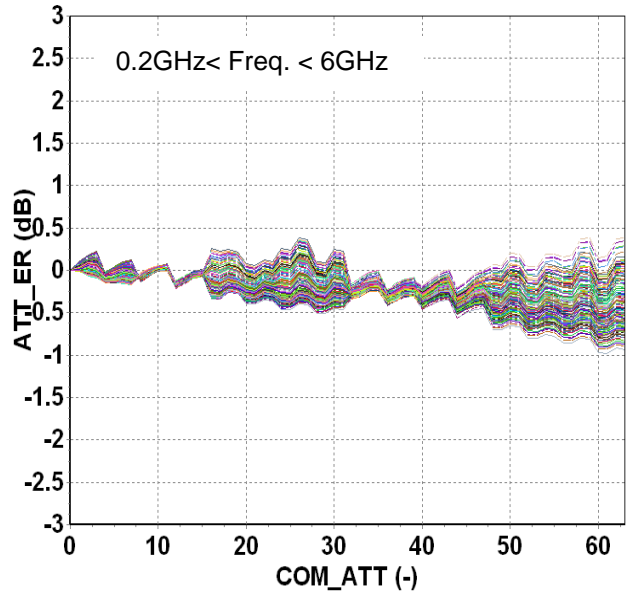
Advanced Information

Attenuator performances: Attenuation error

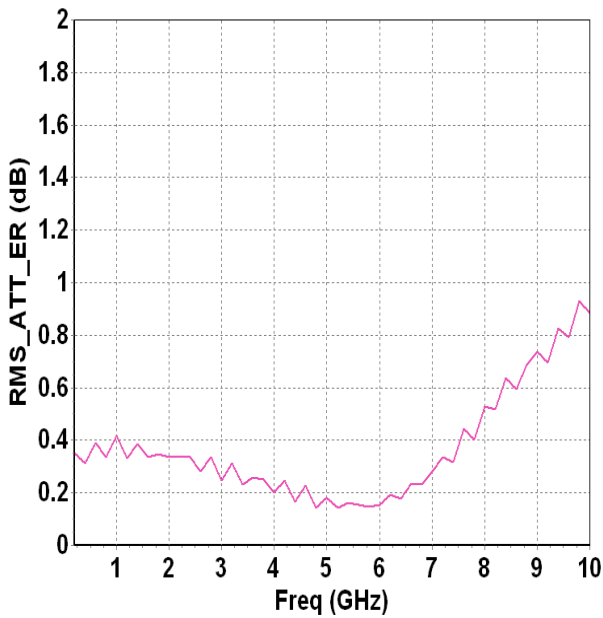
Attenuation error vs. frequency



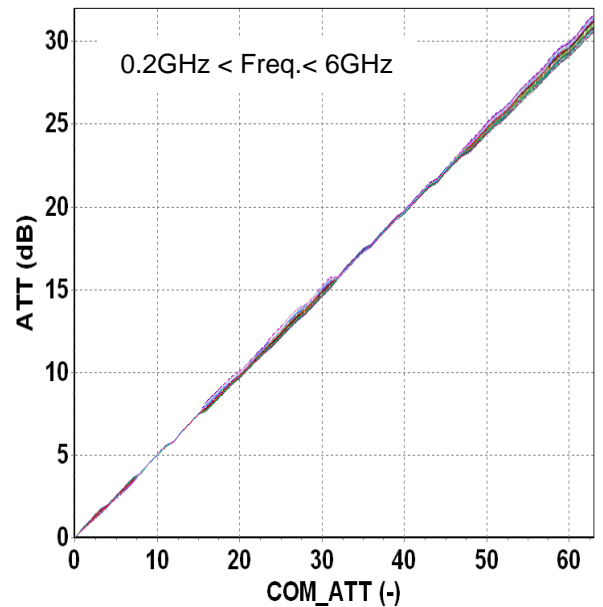
Attenuation error vs. Attenuator state



RMS of Attenuation error



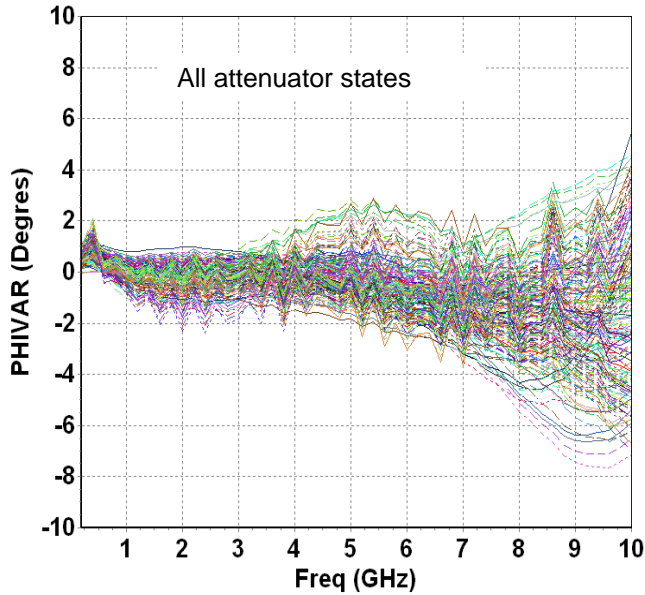
Attenuation vs. attenuator state



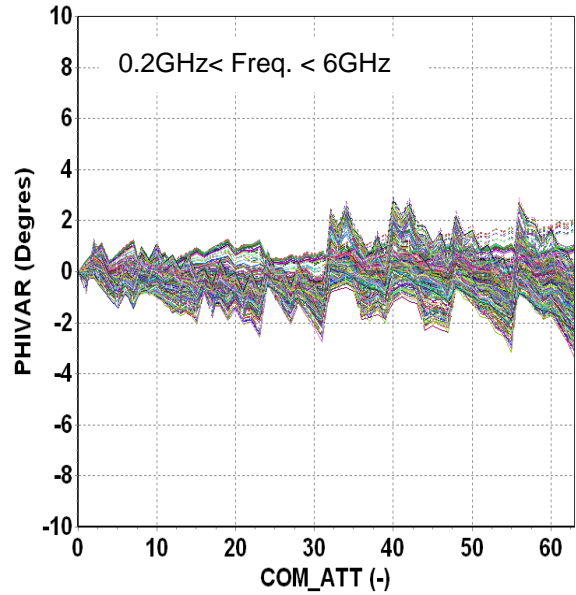
Advanced Information

Attenuator performances: Phase variation

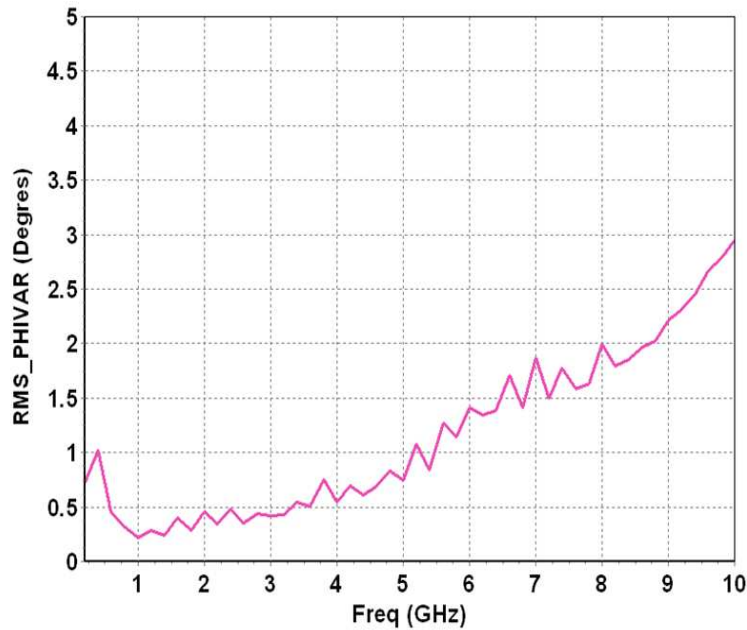
Phase variation vs. frequency



Phase variation vs. Attenuator state



RMS of Phase variation



Advanced Information

Advanced Information

Ref. : AI10050165 -14 Jun 10

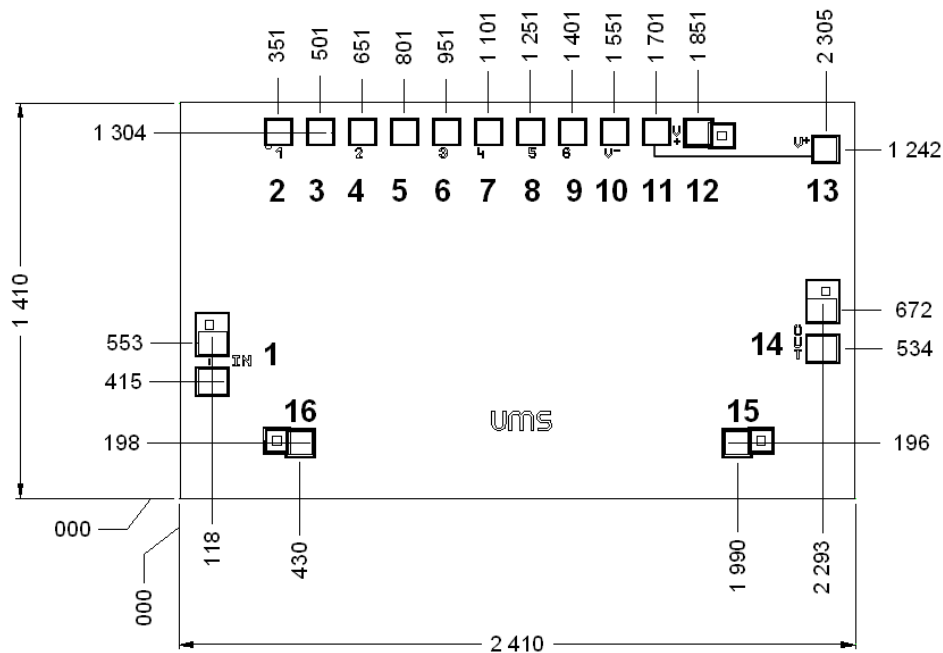
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Mechanical dimensions and pad allocation



UNITS: μm
Tol: $\pm 35\mu\text{m}$

Chip thickness = $100\mu\text{m} \pm 10\mu\text{m}$.

RF pads (1, 14) = $122 \times 100\mu\text{m}^2$

DC and control pads (2, 4, 6, 7, 8, 9, 10, 13, 12, 15, 16) = $100 \times 100\mu\text{m}^2$

Pin number	Pad name	Description
1	IN	Input RF:
2	A1	Attenuator bit 1
4	A2	Attenuator bit 2
6	A3	Attenuator bit 3
7	A4	Attenuator bit 4
8	A5	Attenuator bit 5
9	A6	Attenuator bit 6
10	V-	-5V supply voltage: interface
13	V+	+5V supply voltage: interface (*)
14	OUT	Output RF
3, 5		NC
11	V+	NC (*)
12, 15, 16	GND	NC

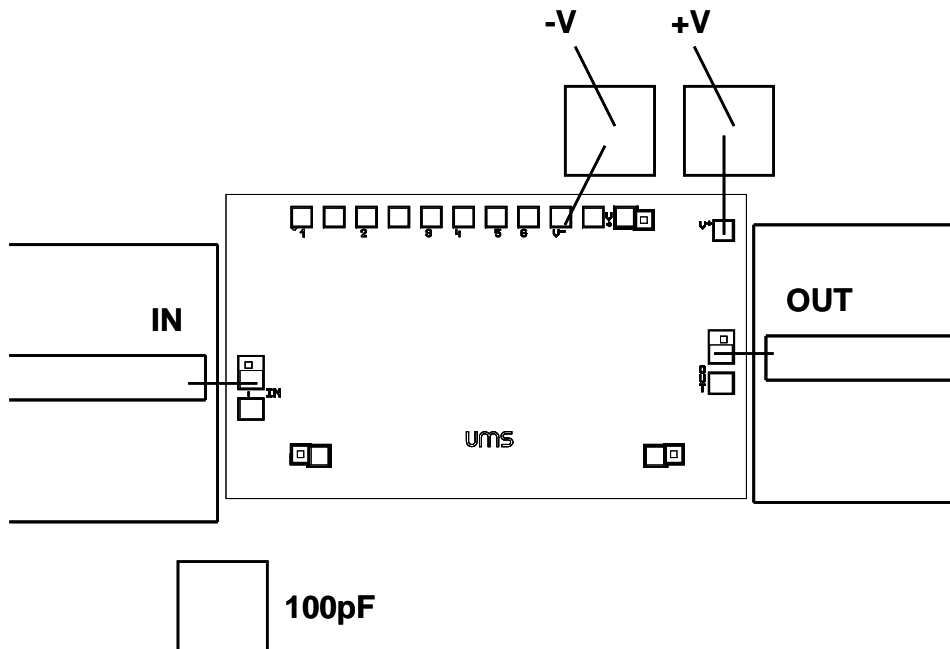
(*): Pin n° 11 is internally connected to Pin n° 13 . Each one of these pins can be indifferently used to supply the control interface with +5V

Advanced Information

Bonding recommendations

Port	Connection
IN(1) OUT (14)	Inductance (L _{bonding}) = 0.3nH two wires: diameter 25µm, length 0.5µm
DC and Interface pads	Inductance (L _{bonding}) = 0.8nH one wire: diameter 25µm, length 1mm

Recommended assembly diagram



Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

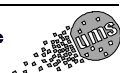
Advanced Information

Biassing conditions

Pin number	Pad name	Value
2	A1	0V / 3.3V
4	A2	0V / 3.3V
6	A3	0V / 3.3V
7	A4	0V / 3.3V
8	A5	0V / 3.3V
9	A6	0V / 3.3V
10	V-	-5V
13	V+	+5V

Biassing conditions

NOTE: control voltages of the attenuator bits are both CMOS and TTL compatible

Advanced Information

Attenuator control table

Voltage to apply on the pads A1 to A6

state	Att (dB)	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0.5	0	0	0	0	0	3.3
2	1	0	0	0	0	3.3	0
3	1.5	0	0	0	0	3.3	3.3
4	2	0	0	0	3.3	0	0
5	2.5	0	0	0	3.3	0	3.3
6	3	0	0	0	3.3	3.3	0
7	3.5	0	0	0	3.3	3.3	3.3
8	4	0	0	3.3	0	0	0
9	4.5	0	0	3.3	0	0	3.3
10	5	0	0	3.3	0	3.3	0
11	5.5	0	0	3.3	0	3.3	3.3
12	6	0	0	3.3	3.3	0	0
13	6.5	0	0	3.3	3.3	0	3.3
14	7	0	0	3.3	3.3	3.3	0
15	7.5	0	0	3.3	3.3	3.3	3.3
16	8	0	3.3	0	0	0	0
17	8.5	0	3.3	0	0	0	3.3
18	9	0	3.3	0	0	3.3	0
19	9.5	0	3.3	0	0	3.3	3.3
20	10	0	3.3	0	3.3	0	0
21	10.5	0	3.3	0	3.3	0	3.3
22	11	0	3.3	0	3.3	3.3	0
23	11.5	0	3.3	0	3.3	3.3	3.3
24	12	0	3.3	3.3	0	0	0
25	12.5	0	3.3	3.3	0	0	3.3
26	13	0	3.3	3.3	0	3.3	0
27	13.5	0	3.3	3.3	0	3.3	3.3
28	14	0	3.3	3.3	3.3	0	0
29	14.5	0	3.3	3.3	3.3	0	3.3
30	15	0	3.3	3.3	3.3	3.3	0
31	15.5	0	3.3	3.3	3.3	3.3	3.3
32	16	3.3	0	0	0	0	0

33	16.5	3.3	0	0	0	0	3.3
34	17	3.3	0	0	0	3.3	0
35	17.5	3.3	0	0	0	3.3	3.3
36	18	3.3	0	0	3.3	0	0
37	18.5	3.3	0	0	3.3	0	3.3
38	19	3.3	0	0	3.3	3.3	0
39	19.5	3.3	0	0	3.3	3.3	3.3
40	20	3.3	0	3.3	0	0	0
41	20.5	3.3	0	3.3	0	0	3.3
42	21	3.3	0	3.3	0	3.3	0
43	21.5	3.3	0	3.3	0	3.3	3.3
44	22	3.3	0	3.3	3.3	0	0
45	22.5	3.3	0	3.3	3.3	0	3.3
46	23	3.3	0	3.3	3.3	3.3	0
47	23.5	3.3	0	3.3	3.3	3.3	3.3
48	24	3.3	3.3	0	0	0	0
49	24.5	3.3	3.3	0	0	0	3.3
50	25	3.3	3.3	0	0	3.3	0
51	25.5	3.3	3.3	0	0	3.3	3.3
52	26	3.3	3.3	0	3.3	0	0
53	26.5	3.3	3.3	0	3.3	0	3.3
54	27	3.3	3.3	0	3.3	3.3	0
55	27.5	3.3	3.3	0	3.3	3.3	3.3
56	28	3.3	3.3	3.3	0	0	0
57	28.5	3.3	3.3	3.3	0	0	3.3
58	29	3.3	3.3	3.3	0	3.3	0
59	29.5	3.3	3.3	3.3	0	3.3	3.3
60	30	3.3	3.3	3.3	3.3	0	0
61	30.5	3.3	3.3	3.3	3.3	0	3.3
62	31	3.3	3.3	3.3	3.3	3.3	0
63	31.5	3.3	3.3	3.3	3.3	3.3	3.3

Advanced Information

Sampling request reference:

ES-CHT4012-98F (Die)

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