TAT9988

CATV GaN Power Doubler MMIC

Applications

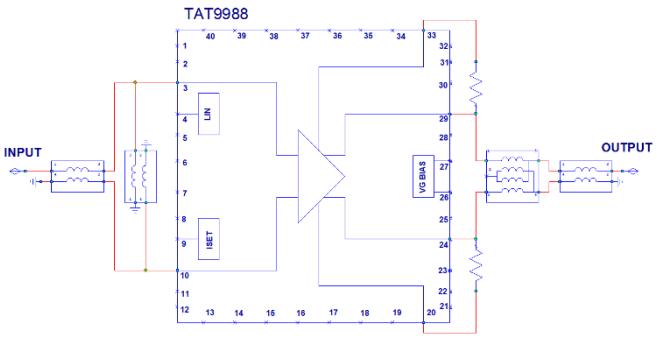
- HFC Nodes
- CATV Line Amplifiers
- Head End Equipment

40 Pin 5x7 mm QFN Package

Product Features

- Excellent High Output Linearity
- High Gain 24dB @ 1000MHz
- 50MHz – 1000MHz Bandwidth
- Ultra-Low CSO/CTB/XMOD
- Low Noise
- Excellent Input/Output Match
- Variable Bias Control
- Compact Size
- High Reliability
- 24V, 445mA

Functional Block Diagram



General Description

The TAT9988 is an ultra-linear, packaged GaAs/GaN amplifier intended for output stage amplification in CATV infrastructure applications.

The TAT9988 features a push-pull cascode design which provides flat gain along with ultra-low distortion, making it ideal for use in CATV distribution systems requiring high output power capability.

The TAT9988 draws 445mA from a 24V supply and exceeds the output linearity performance of traditional GaAs-based amplifiers.

The TAT9988 allows users to adjust the bias current and the bias voltage externally in order to optimize output performance.

The TAT9988 is packaged in an industry standard 40 pin 5x7 mm^2 QFN package.

Pin Configuration

Pin No.	Label
3	Non-Inverting Amplifier Input
4	Linearizer Current-Adjust
6,7	Common Source Node
9	Amplifier Current-Adjust
10	Inverting Amplifier Input
20	Feedback to Inverting Input
24	Non-Inverting Amplifier Output
26	Output Device Gate Bias 1
27	Output Device Gate Bias 2
29	Inverting Amplifier Output
33	Feedback to Non-Inverting
1,2,5,8,11-12, 21-23,25, 28, 30-32,	No connect
13-19, 34-40	Ground

Ordering Information

Part No.	Description
TAT9988	CATV GaN Power Doubler MMIC
TAT8888	50-1000 MHz Hybrid Evaluation Board

Standard T/R size =1000 pieces on a 7” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-40 to +100°C
RF Input Power, CW, 75Ω, T=25°C	70 dBmV
Supply Voltage (V_{DD})	+30 V
Supply Current (I_{DD})	600 mA

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})		24		V
Case Temperature	-30		+100	°C
Junction Temperature, Tj			155	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Typical Performance – Push-Pull Configuration (1)

Test conditions unless otherwise noted: V_{DD}=+24 V, 75 Ω System, Base Temp=+35°C.

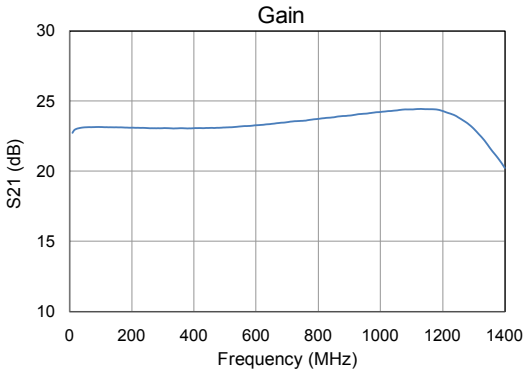
Parameter	Conditions	Min	Typ	Max	Units
Operating Frequency		50		1000	MHz
Gain	Tested at 1000 MHz	23	23.5	24.25	dB
Gain Slope	45 to 1003 MHz	0.25		1.5	dB
Gain Flatness	Relative to Slope Line		±0.5	±0.8	dB
Input Return Loss (2)			18		dB
Output Return Loss (2)			19		dB
CSO	79 channels NTSC 75 channels QAM, -6dB offset, 60 dBmV virtual output, 18dB Tilt		-69	-65	dBc
CTB			-75	-69	dBc
XMOD			-65		dBc
CCN		55	59		dBm
Output IP3	Pout= 19 dBm/tone, at 500 MHz Δf = 6 MHz		53		dB
Noise Figure			3.5		dB
Supply Current, I_{DD}		410	445	470	mA
Thermal Resistance, θ_{jc}	Junction to case		5		°C/W

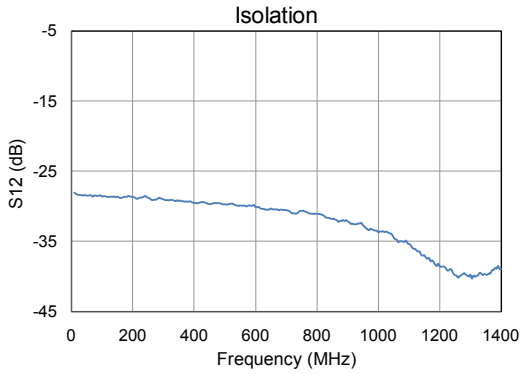
Notes:

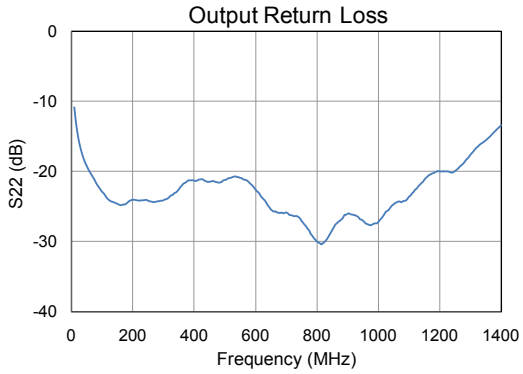
1. Includes balun, board, and connector losses.
2. Return losses dependent on balun and transformer selection.

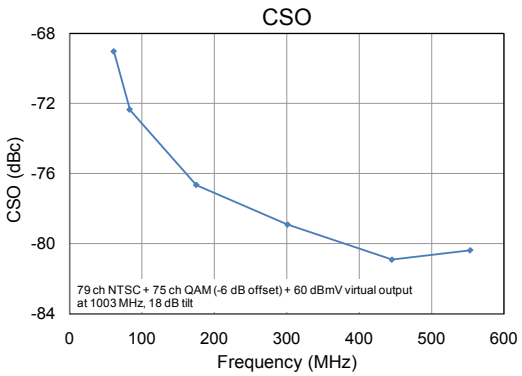
Performance Plots – TAT8888 Hybrid Evaluation Board

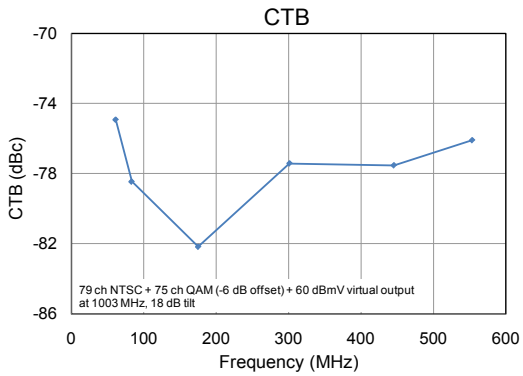
Test conditions unless otherwise noted: V_{DD}=+24 V, 75 Ω System, Base Temp=+35°C.

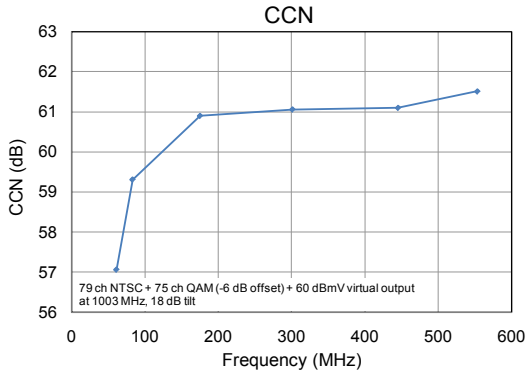




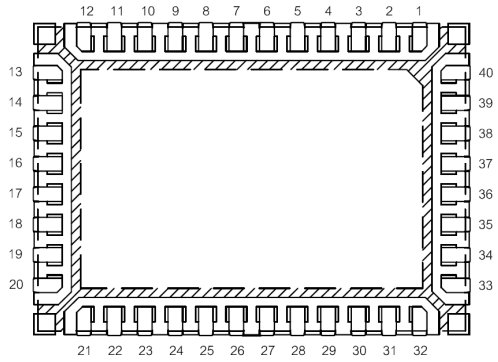








Pin Configuration and Description



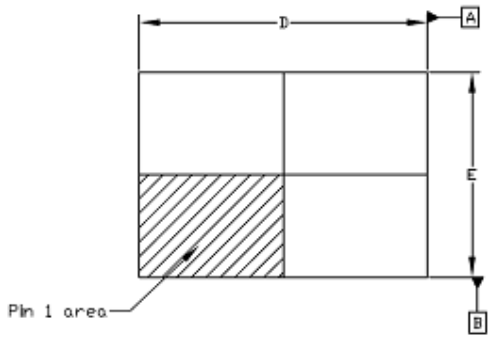
Pin No.	Function	Description

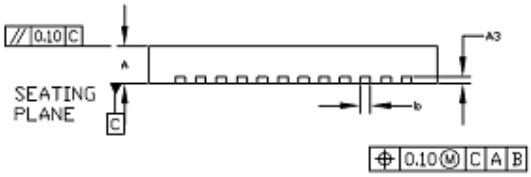
3	Non-Inverting Amplifier Input	Requires AC coupling from input balun
4	Linearizer Current-Adjust	Connect to VDD through resistors R4 and R8
6,7	Common Source Node	DC GND. DC resistance to be minimized from this node to GND.
9	Amplifier Current-Adjust	Connect to VDD through resistor R3.
10	Inverting Amplifier Input	Requires AC coupling from input balun
20	Feedback to Inverting Input	Connects to non-inverting output (Pin 24). Path is layout sensitive and should be kept as short as possible.
24	Non-Inverting Amplifier Output	RF choke required to VDD through output transformer center tap.
26	Output Device Gate Bias 1	Set to 3.25V using resistive divider network between VDD and GND.
27	Output Device Gate Bias 2	Set to 3.25V using resistive divider network between VDD and GND.
29	Inverting Amplifier Output	RF choke required to VDD through output transformer center tap.
33	Feedback to Non-Inverting Input	Connects to inverting output (Pin 29). Path is layout sensitive and should be kept as short as possible.
Backside Paddle	RF/DC GND	Very low DC, RF and thermal resistance required from this node to the heatsink. Recommended via pattern should be followed to minimize thermal resistance.

Package Marking and Dimensions

Marking: Line 1: TriQuint Logo –
Line 2: TAT9988 = Product code
Line 3: YYWW CCCC = Date code, country code
Line 4: AaaXXXX = Aaa = vendor code, Lot #

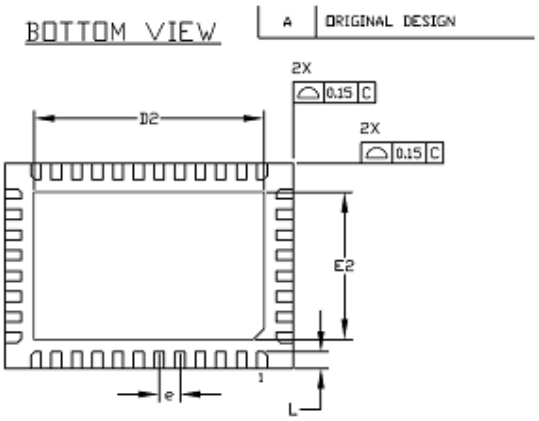
TOP VIEW





SIDE VIEW

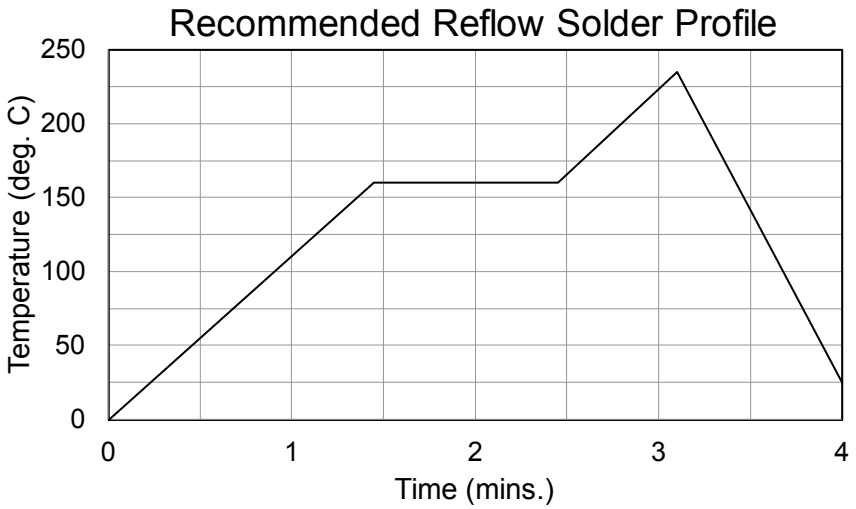
BOTTOM VIEW



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.034	0.036	0.038
A3	0.203 REF			0.008 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	6.85	7.00	7.15	0.269	0.275	0.281
D2	5.50	5.60	5.70	0.216	0.220	0.224
E	4.85	5.00	5.15	0.190	0.196	0.202
E2	3.50	3.60	3.70	0.137	0.141	0.145
e	0.50 REF			0.020 REF		
L	0.30	0.40	0.50	0.012	0.016	0.020

Recommended Reflow Solder Profile

The following solder reflow profile is for a typical SAC305 no-lead solder paste application and assumes that industry standard PCB layout rules have been followed. Solder paste manufacturers will recommend a "typical" solder reflow profile depending on their particular solder paste's flux and metal composition. PCB size & composition, component density & position and reflow equipment are some of the factors that will impact and dictate the optimum reflow profile in specific manufacturing scenarios.



Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 0
Value: <250 Volts
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class III
Value: 500 to 1000 Volts
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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