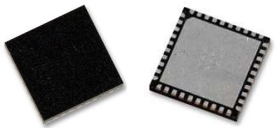
TAT3814

5-300 MHz Variable Gain Return Path Amplifier

Applications

- Return Path Amplifier
- System Amplifier
- Line Amplifier
- DOCSIS Return Path VGA
- Bonded Channel Cable Modem Return Path

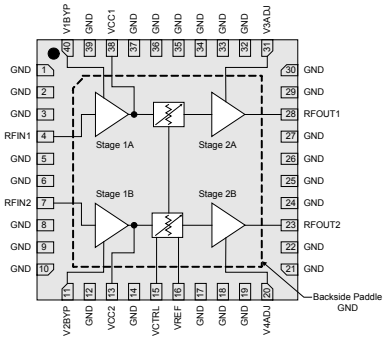


6x6 mm 40 Pin leadless SMT Package

Product Features

- Integrates Attenuation and Amp Functionality
- 5-300 MHz Performance
- 75 Ohm
- Variable gain attenuator: 20 dB typical range
- Max gain setting: 36 dB typical
- 15 dB typical return loss across gain range
- 5 dB typical Noise Figure
- 40dBm typical OIP3
- +8 V Supply (Lower supply voltages possible)
- 320 mA Operating Current
- Compact 6x6 mm integrated package

Functional Block Diagram



General Description

The TAT3814 is a variable gain return path amplifier designed for head-end and system amplifier infrastructure applications. The TAT3814 provides up to 37 dB gain with 20dB automatic gain control capability.

The small size, 6x6 mm and efficient power dissipation, nominal 2.5 watts, provide an ideal solution for high density head-end applications and compact system amplifiers.

Standard supply voltage for the TAT3814 is +8V. Operation from lower supply voltages is possible. Contact TriQuint CATV applications for guidance.

The TAT3814 is fabricated using 6-inch GaAs pHEMT and HBT technologies to optimize performance and cost.

Pin Configuration

Pin No.	Symbol
1-3, 5-6, 8-10, 12, 14, 17-19, 21-22, 24-27, 29-30, 32-37, 39	GND
4 / 7	RFIN1 / RFIN2
11	V2BYP
40	V1BYP
13 / 38	VCC2 / VCC1
15	VCTRL
16	VREF
20	V4ADJ
23 / 28	RFOUT2 / RFOUT1
31	V3ADJ
Backside Paddle	GND

Ordering Information

Part No.	Description
TAT3814	Return path VGA
TAT3814-PCB	5-300 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7” x 12mm reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150°C
RF Input Power, CW, 75 Ω, T=25°C	+24 dBm
V_{CC} (pins 13, 23, 28, 38)	+10 V
I_{CC} (Stage 1A or 1B, pins 13 or 38)	55 mA
I_{CC} (Stage 2A or 2B, pins 23 or 28)	135 mA
V_{REF} and V_{CTRL}	+10 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{SUPPLY}	7.75	8.0	8.25	V
T_{CASE}	-40		+85	°C
Tj for >10^6 hours MTTF			+150	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

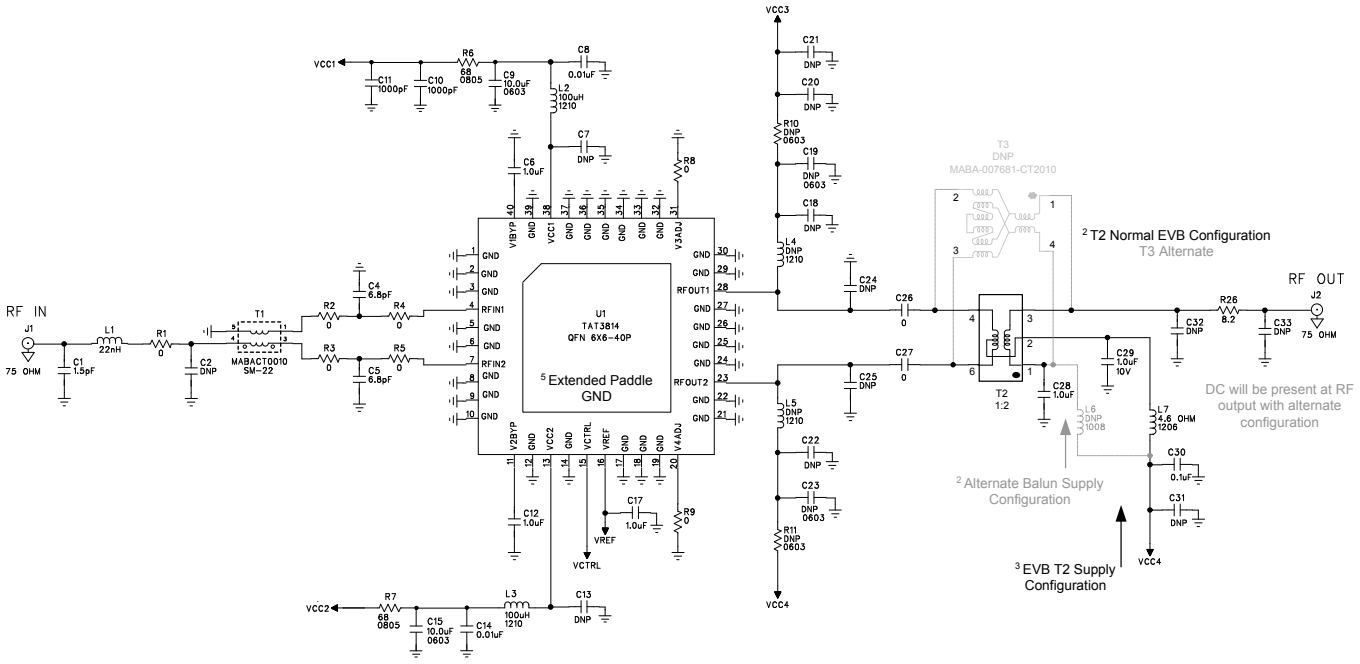
Test conditions unless otherwise noted: +25°C, V_{DD} =+8V, 75 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		5		300	MHz
Gain	Test Freq=300 MHz	35	36	38	dB
Gain Flatness			± 1		dB
Output Return Loss		15	20		dB
Output P1dB	Test Freq=300 MHz	+24	+26		dBm
Output IP3	Pout / tone= 6 dBm f1 = 294 MHz f2 = 300 MHz		+40		dBm
Gain Control Range	V_{CTRL} = 0 to +7V		20		dB
Noise Figure	Test Freq=300MHz		5	6	dB
I_{CC} Stage 1A or 1B	Pin 13 or 38 (note 1)		45		mA
I_{CC} Stage 2A or 2B	Pin 23 or 28 (note 1)		104		mA
I_{REF}	Pin 16		7		mA
I_{CTRL}	Pin 15		11	20	mA
Thermal Resistance (jnc to case)			12		°C/W

Notes:

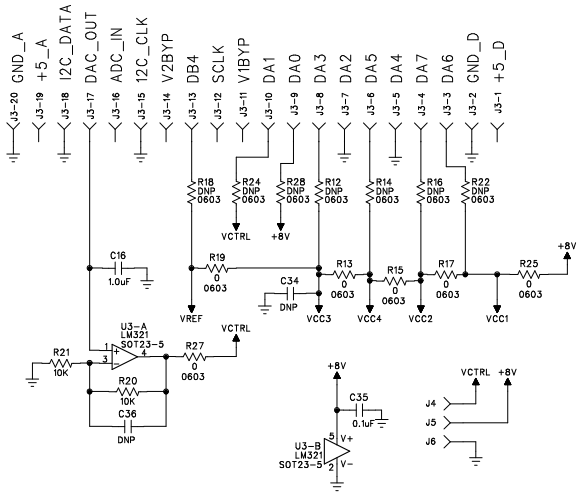
1. Total amplifier current is Icc Stages 1A+1B+2A+2B

TAT3814-PCB Evaluation Board



Notes:

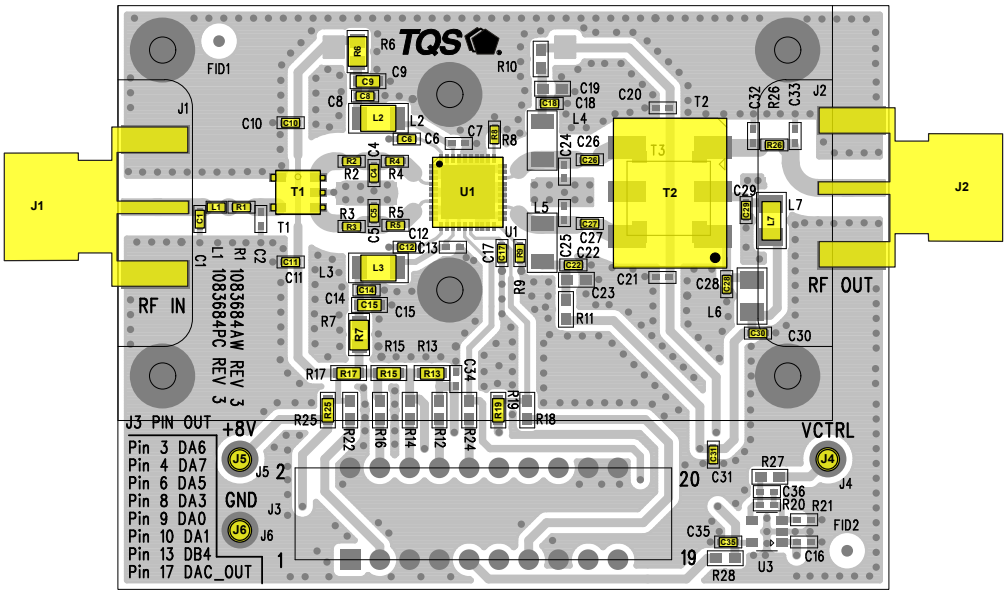
1. Supply 8V to J5-1 and VCTRL to adjust gain at J4-1, using common ground at J6-1. No turn on sequence is required, 0V at VCTRL will give max gain and OiP3.
2. While the device only requires a few basic supporting components, the EVB has additional complexity to accommodate two choices of output baluns (T2 or T3) and to allow Vcc4 bias to be either through the output balun or through RFC L4 and L5. This feature is provided to potentially improve distortion characteristics of the transformer by not having an offset fixed DC magnetic flux in the core
3. Standard evaluation board configuration is VCC4 bias through T2.
4. Vcc and Vref use jumpers to the +8V supply, only one other 0 to 7V supply is needed to vary the internal gain setting through VCTRL.
5. The TAT3814 backside paddle is both RF and thermal ground which is mounted to a block to assist in dissipation. See PCB Mounting Pattern at the end of this data sheet.
6. All 0ohm resistors can be replaced by Cu trace on PCB
7. BOM supersedes schematic values should there be a discrepancy
8. DNP = Do Not Place



DC Supply & Gain Control Options

Option	V_{CTRL}	+8V	GND	R12, R14, R16, R24, R28	R13, R15, R17, R19, R25	R18, R22	R27	C16, C34	C36	U3	R20	R21
On Board Turrets	J4	J5	J6	DNP	0 Ω	DNP	DNP	DNP	DNP	DNP	DNP	DNP
20 Pin Connector	J3-10	J3-3, J3-4, J3-6, J3-8, J3-9, J3-12 J3-13	J3-2, J3-20	0 Ω	DNP	0 Ω	DNP	DNP	DNP	DNP	DNP	DNP
Ext. USB Controller	Refer to EVH Documentation			DNP	0 Ω	0 Ω	0 Ω	0.1 uF	1000 pF	LM321MF	10 KΩ	10 KΩ

TAT3814-PCB Evaluation Board



Bill of Material - TAT3814-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	TAT3814	TriQuint	TAT3814
T1	n/a	1:1 Balun	MA/COM	MABACT0010
T2	n/a	2:1 Balun	Mini-Circuits	ADT2-32-1+
L1	24 nH	Ind 0402 ±2%	Murata	LQW15AN24NG00D
L2-L3	100 uH	Ind 1212 ±20% 200mA	Murata	LQH3NPN101MM0
L7	4.64 Ω	Res 1206 ±1% 1/4W	various	
C1	1.5 pF	Cap 0402 ±0.1pF 50V NPO/COG	various	
C4, C5	6.8 pF	Cap 0402 ±0.1pF 25V Accu-P	AVX	04023J6R8BBSTR
C6, C12, C17, C28, C29	1 uF	Cap 0402 ±10% 10V X5R	various	
C9, C15	10 uF	Cap 0603 ±20% 10V X5R	various	
C8, C14, C18, C22	0.01 uF	Cap 0402 ±10% 16V X7R	various	
C30, C35	0.1 uF	Cap 0402 ±10% 10V X5R	various	
C10, C11, C31	1000 pF	Cap 0402 ±10% 50V X7R	various	
C26, C27, R1-R5, R8, R9	0 Ω	Res 0402	various	
R13, R15, R17, R19, R25	0 Ω	Res 0603	various	
R6, R7	68 ohm	Res 0805 ±1% 1/8W	various	
R26	8.2 Ω	Res 0402 ±1% 1/16W	various	
C2, C7, C13, C16, C19-C21, C23-C25, C32-C34, C36	n/a	DNP	n/a	n/a
L4-L6	n/a	DNP	n/a	n/a
R10-R12, R14, R16, R18, R20-R22, R24, R27-R28	n/a	DNP	n/a	n/a

Typical Performance TAT3814-PCB

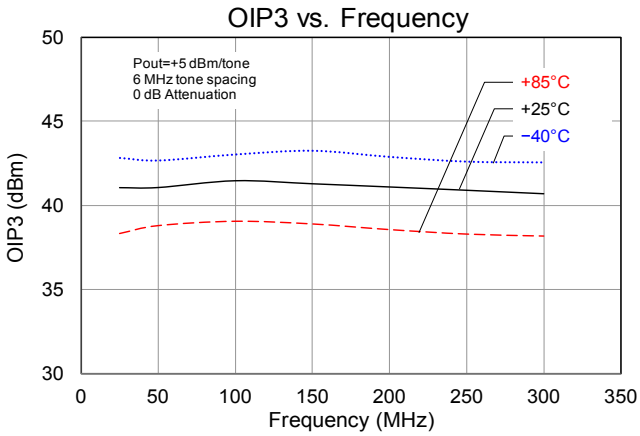
Test conditions unless otherwise noted: V_{CC}=+8 V, V_{REF}=+8V, V_{CTRL}=0V, I_{CC} = 320 mA, T_{CASE} = +25°C, 75 Ω system

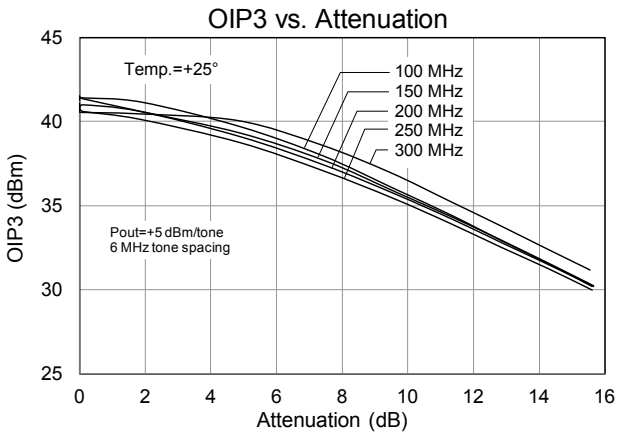
Parameter	Conditions	Typical Value				Units
Frequency		5	100	200	300	MHz
Gain	Max Gain Setting	36	36	35.8	35.4	dB
Input Return Loss	Max Gain Setting	18	15	15	20	dB
Output Return Loss	Max Gain Setting	16	17	17	20	dB
Output P1dB		25	25	24.8	24.4	dBm
OIP3	Pout= 6 dBm/tone, Δf=6 MHz	41	42	41	39	dBm
Noise figure		5.5	5.0	4.8	5.5	dB
Stage 1A or 1B Current	Pin 11 or 38 (note 1)	50				mA
Stage 2A or 2B Current	Pin 23 or 28 (note 1)	104				mA
V_{REF} Current	V_{CTRL}= 0 to 7V at pin 16	7 to 0				mA
V_{CTRL} Current	V_{CTRL}= 0 to 7V at pin 15	0 to 11				mA

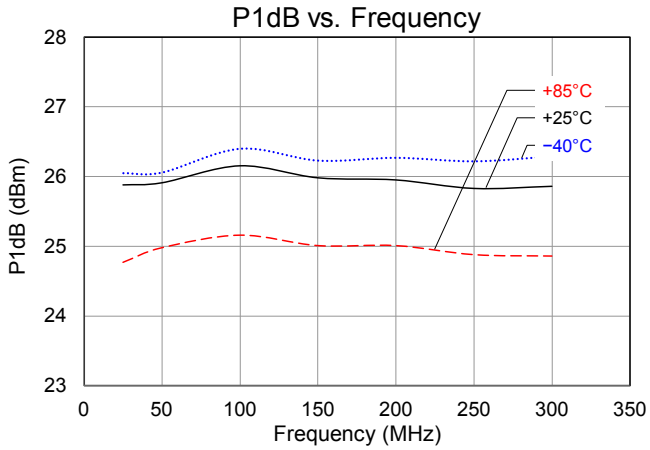
Notes:
1. Total amplifier current is Icc Stages 1A+1B+2A+2B

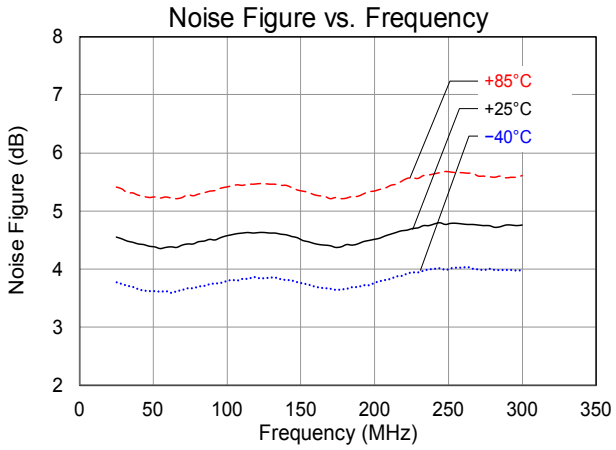
Performance Plots - TAT3814-PCB

Test conditions unless otherwise noted: V_{CC}=+8 V, V_{REF}=+8V I_{CC} = 320 mA, T_{CASE} = +25°C, 75 Ω system



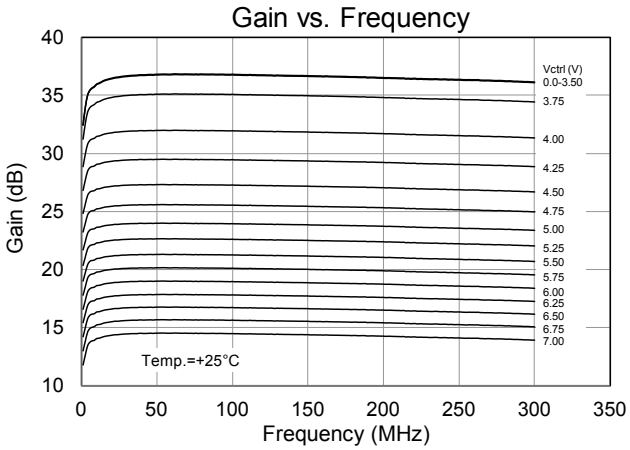


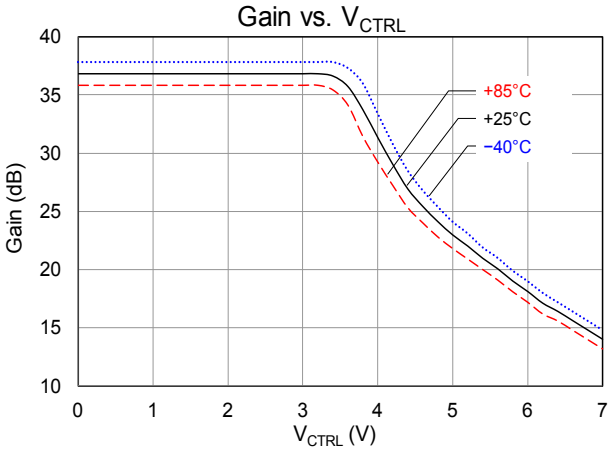


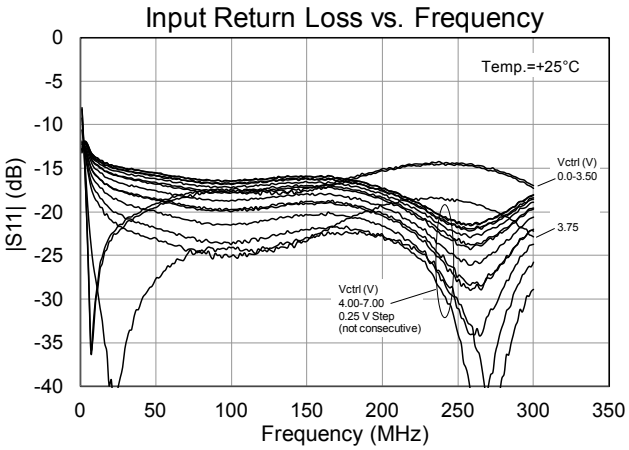


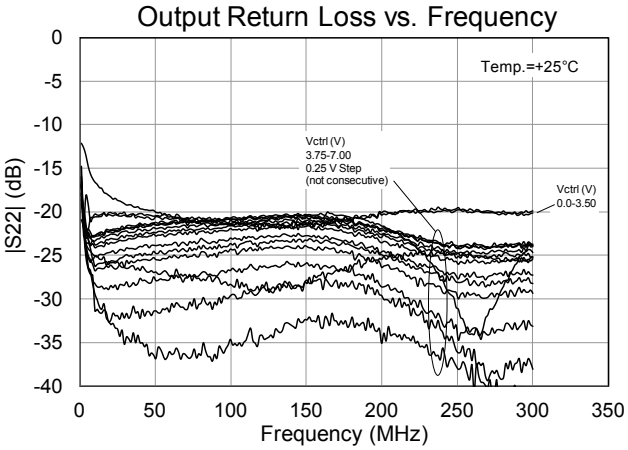
Performance Plots - TAT3814-PCB

Test conditions unless otherwise noted: V_{CC}=+8 V, V_{REF}=+8V I_{CC} = 320 mA, T_{CASE} = +25°C, 75 Ω system

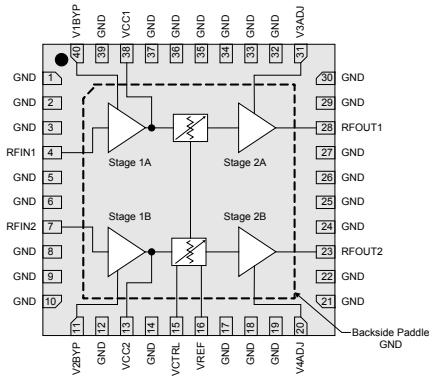








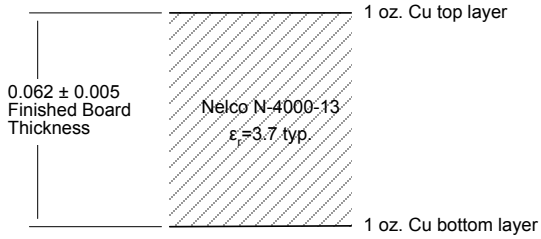
Pin Configuration and Description



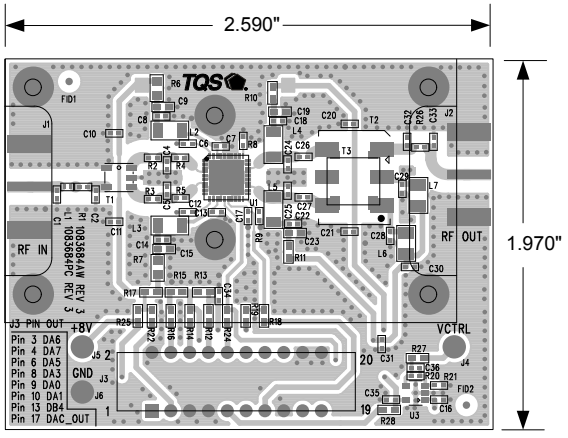
Pin No.	Symbol	Description
1-3, 5-6, 8-10, 12, 14, 17-19, 21-22, 24-27, 29-30, 32-37, 39	GND (Ground)	RF/DC Ground
4, 7	RFIN1 / RFIN2	RF Input 1A / RF Input 1B Impedance matching required.
11, 40	V2BYP / V1BYP	Stage 1B bypass / Stage 1A bypass
13, 38	VCC1 / VCC2	Stage 1A/ Stage 1B DC supply. Bias choke and dropping resistor required.
15	VCTRL	Gain Control (0 to +7V)
16	VREF	Fixed DC Gain Control reference (+8V)
20, 31	V4ADJ / V3ADJ	Stage 2B bias adjust / Stage 2A bias adjust
23	RFOUT2	RF output / Stage 2A DC supply. Impedance matching, DC block and bias choke required.
28	RFOUT1	RF output / Stage 2B DC supply. Impedance matching, DC block and bias choke required.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

TriQuint PCB 1083684 Material and Stack-up



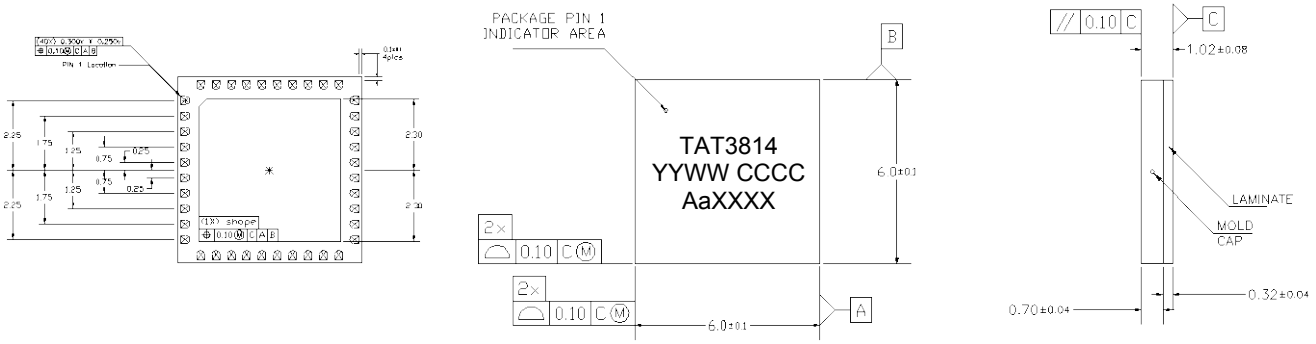
Dielectric Core = 0.059 ± 0.005"



Mechanical Information

Package Marking and Dimensions

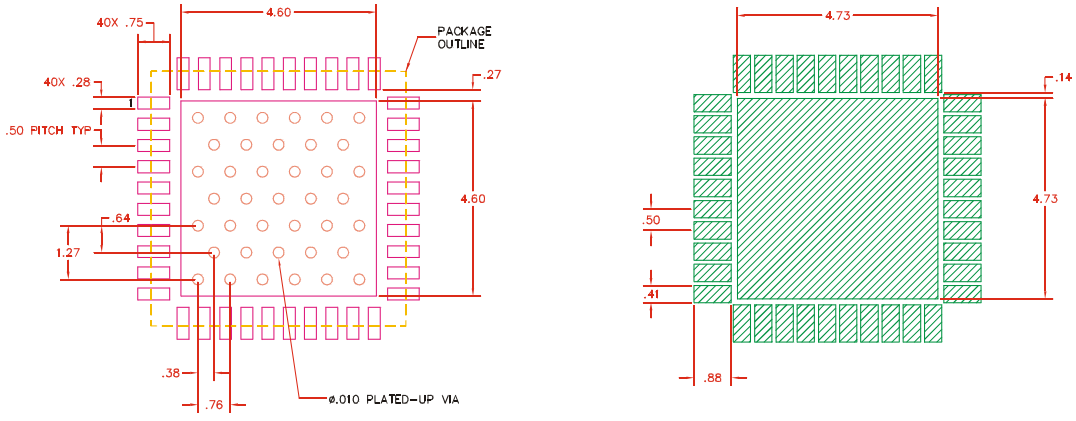
Marking: Part number – TAT3814
Year/week/Country Code - YYWW CCCC
Lot Code – AaXXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



TOP VIEW LAND PATTERN

TOP VIEW SOLDER MASK

NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
5. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
6. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating:	Class 1B
Value:	Passes ≥ 600 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 2000 V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

MSL Rating:	Level 3
Test:	260°C convection reflow
Standard:	JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

Package contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Important Notice

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.503.615.9000
Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information: **Email:** sjcapplications.engineering@tqs.com

Contact Information

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