

35-40GHz Low Noise, Variable Gain Amplifier

GaAs Monolithic Microwave IC

Description

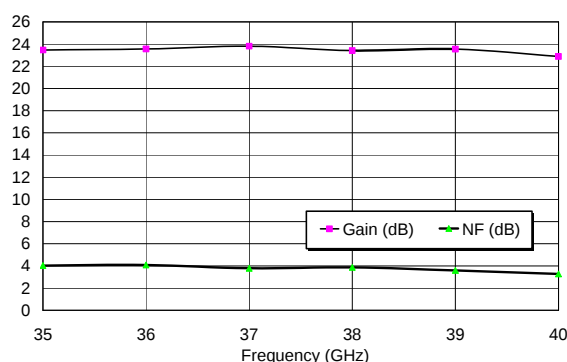
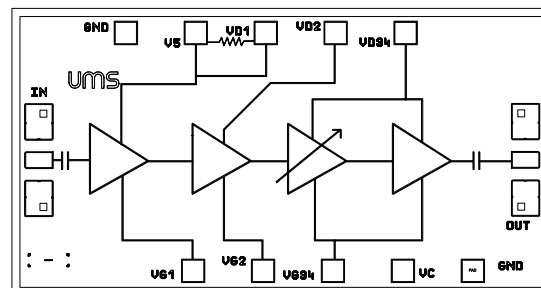
The CHA2294 is a high gain four-stage monolithic low noise amplifier with variable gain. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.

Main Features

- Frequency range: 35-40GHz
- 4.0dB Noise Figure.
- 22dB gain
- Gain control range: 15dB
- Low DC power consumption, 120mA @ 5V
- Chip size: 2.32 X 1.235 X 0.10 mm



Typical on wafer measurements : Gain & NF

Main Characteristics

Tamb. =25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	35		40	GHz
G	Small signal gain	20	22		dB
NF	Noise figure		4	4.5	dB
Gctrl	Gain control range with Vc variation	10	15		dB
Id	Bias current		120		mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precaution

Electrical Characteristics for Broadband OperationT_{amb} = +25°C, V₅=V_{d2}=V_{d,3,4}=5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	35		40	GHz
G	Small signal gain (1)	20	22		dB
ΔG	Small signal gain flatness (1)		±1.0		dB
Is	Reverse isolation (1)		50		dB
NF	Noise figure with V _c =1.2V		4	4.5	dB
Gctrl	Gain control range versus V _c	10	15		dB
P1dB	Output power at 1dB compression with V _c =1.2V		11		dBm
VSWRin	Input VSWR (1)			2.0:1	
VSWRout	Output VSWR (1)			1.5:1	
Vd	DC voltage V ₅ = V _{d2} =V _{d3,4} V _c	-1.5	5 [-0.7, +1.2]	+1.3	V V
Id1	Bias current (2) with V _c =1.2V		20		mA
Id	Bias current total (3) with V _c =1.2V		120		mA

(1) These values are representative of on-wafer measurements that are made without bonding wires at RF ports.

(2) For optimum noise figure, the bias current Id1 should be adjust to 20mA with Vg1 voltage.

(3) With Id1=20mA, adjust Vg2,3,4 voltage for a total drain current around 120mA.

Absolute Maximum RatingsT_{amb.} =25°C (1)

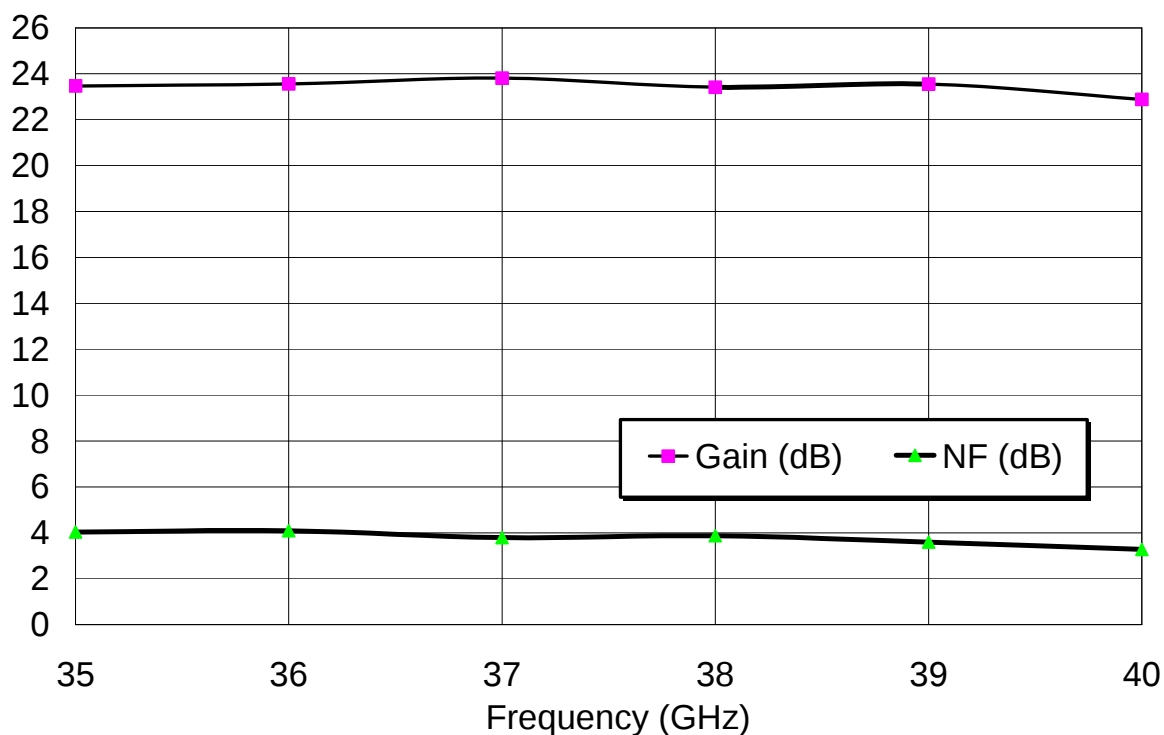
Symbol	Parameter	Values	Unit
Vd	Maximum Drain bias voltage	+5.2	V
Id	Maximum drain bias current	200	mA
Vg	Gate bias voltage	-2.5 to +0.4	V
Vc	Maximum Control bias voltage	+1.5	V
Vdg	Maximum drain to gate voltage (V _d - V _g)	+5.0	V
Pin	Maximum input power overdrive (2)	+15	dBm
Tch	Maximum channel temperature	+175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

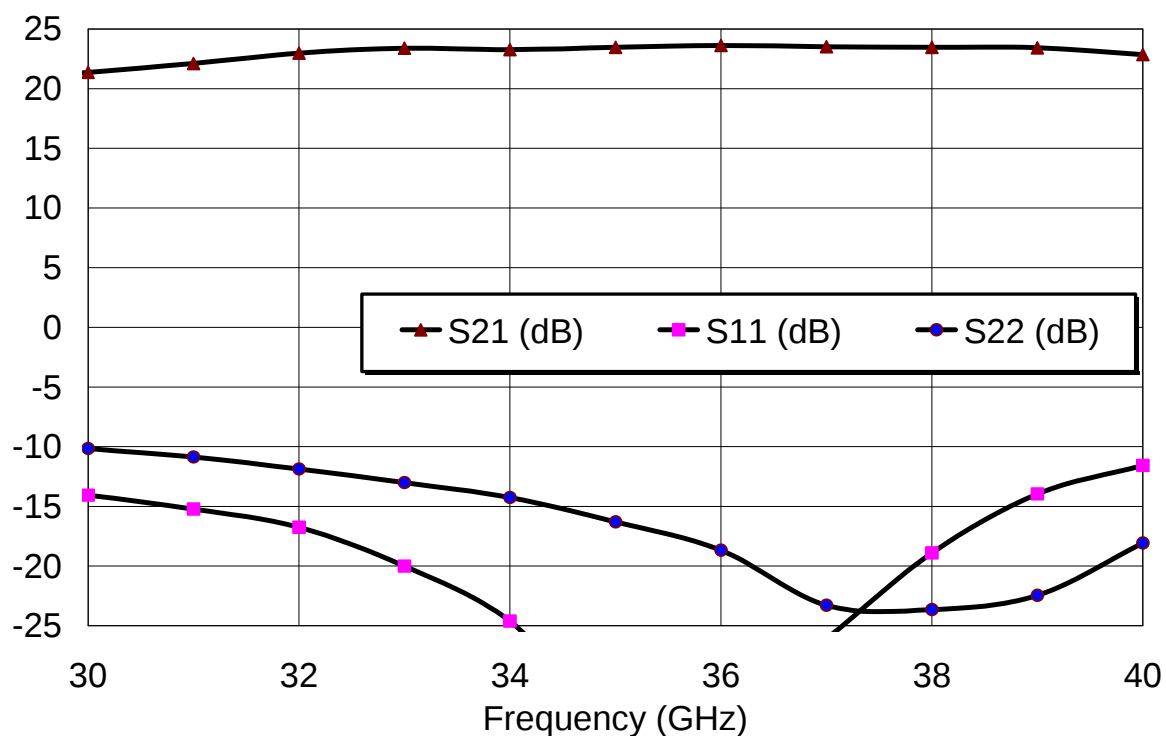
(2) Duration < 1s.

Typical on wafer Measurements

Bias Conditions : $V_5=V_{d2}=V_{d3,4}=5V$, V_{g1} for $I_{d1}=20mA$, $V_{g2}=V_{g3,4}=-0.3V$,
 $V_c=+1.2V$



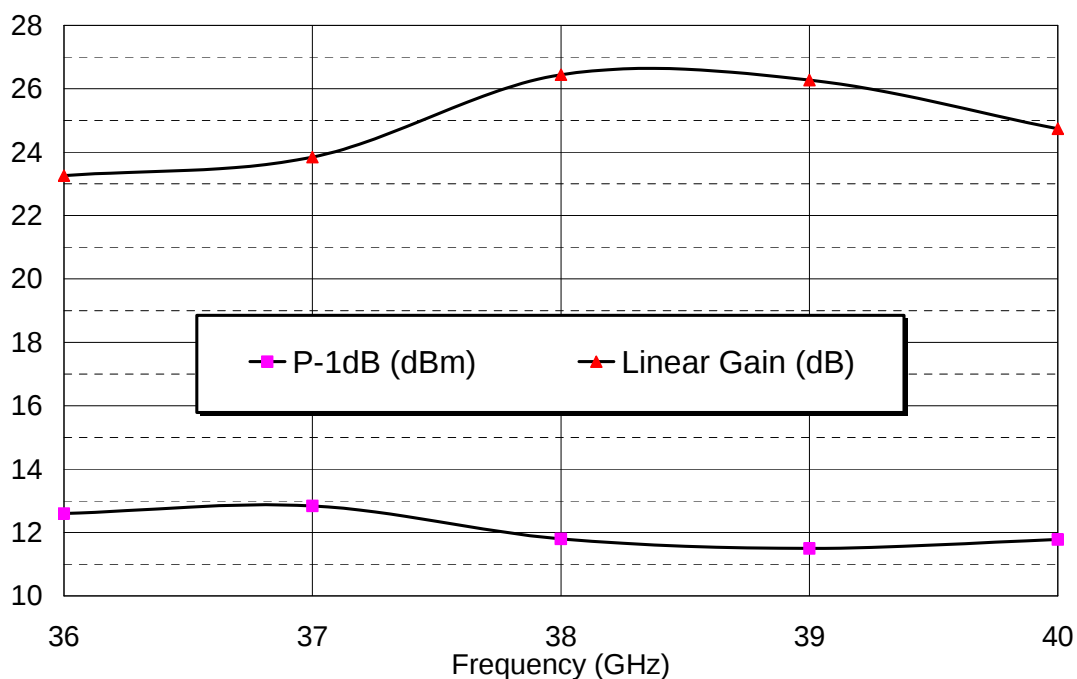
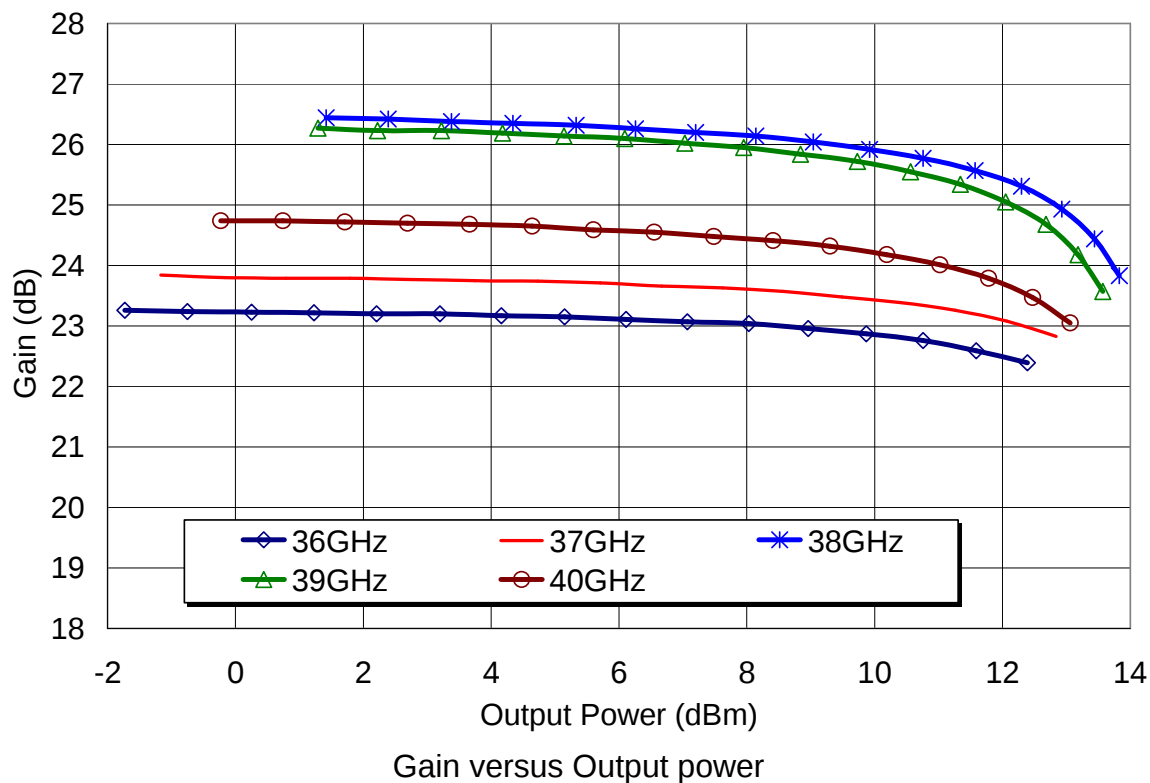
Gain & Noise Figure versus frequency

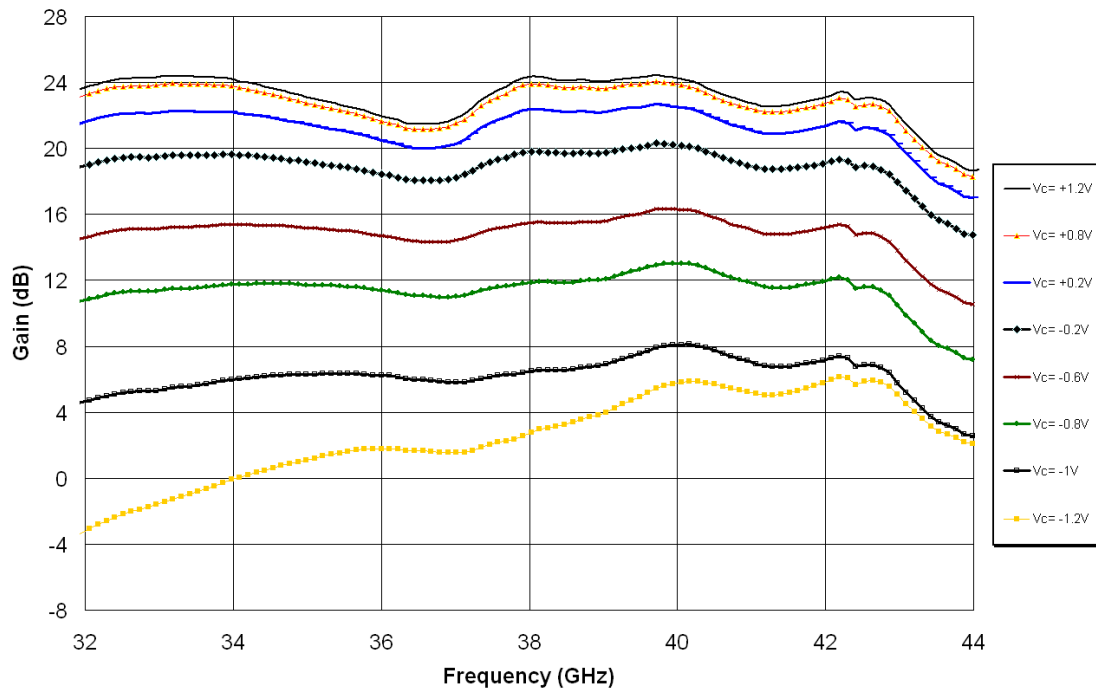


Gain & Return Loss versus frequency

In jig Measurements

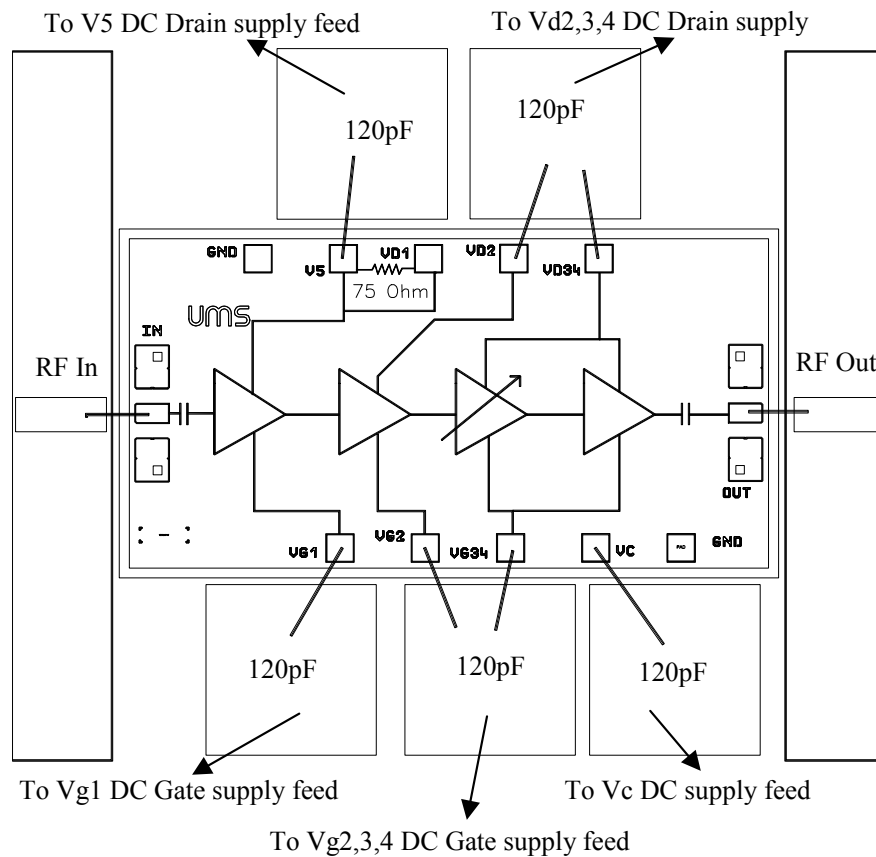
Bias Conditions : $V_5=V_{d2}=V_{d3,4}=5V$, $V_{g1}=V_{g2}=V_{g3,4}=-0.3V$, $V_c=+1.2V$



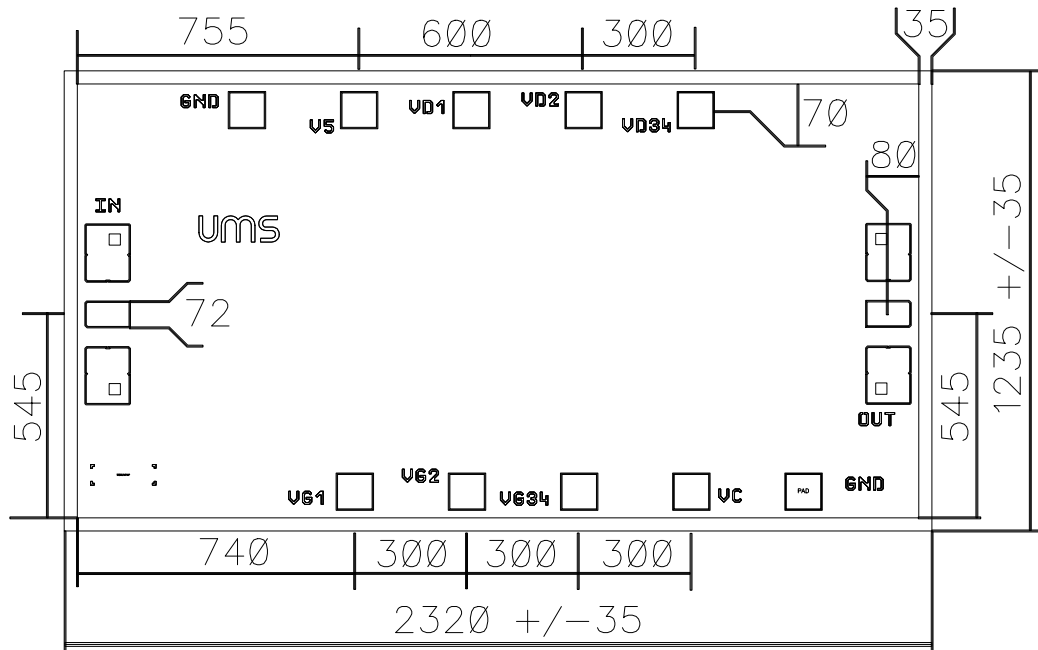


Gain versus frequency and Vc

Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25 μ m diameter gold wire is recommended
Bond Pad: 100 x 100 μ m



Bonding pad positions

(Chip thickness : 100µm. All dimensions are in micrometer)

Ordering Information

Chip form : CHA2294-99F/00

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