12.5-30GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

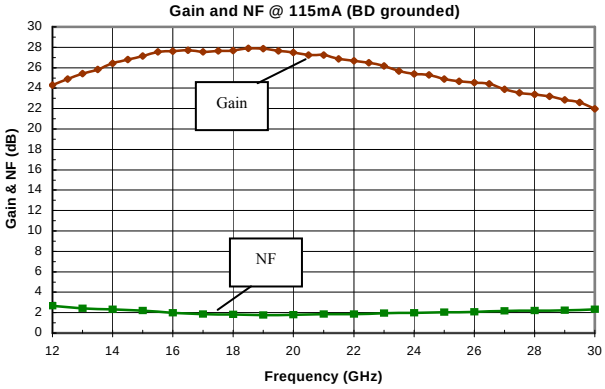
The CHA3688aQDG is a three-stage self-biased wide band monolithic low noise amplifier.

The circuit is manufactured with a standard P-HEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in lead-free package.

Main Features

- Broadband performance 12.5 - 30GHz
- 2.1dB noise figure
- 26dB gain
- 26dBm Output IP3
- Low DC power consumption
- 24L-QFN4x4 SMD package
- RF ports ESD protected (see page 14)



Main Characteristics

Tamb = +25°C, Vd1=Vd2=Vd3 = +4V Pads: B, D = GND (High current configuration)

Symbol	Parameter	Min	Typ	Max	Unit
NF	Noise figure		2.1	2.5	dB
G	Gain	21	26		dB
OIP3	3rd order intercept point (16 - 30GHz)	24	26		dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics (low current configuration)

Tamb = +25°C, Vd1=Vd2=Vd3= +4V **Pads B, D not connected**

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	12.5		30	GHz
G	Linear Gain (12.5 - 24GHz)	22	25		dB
	Linear Gain (24.5 - 30GHz)	20	23		dB
ΔG	Gain flatness (12.5 - 24GHz)		±1.5		dB
	Gain flatness (24.5 - 30GHz)		±2		dB
NF	Noise figure (12.5 - 16GHz)		2.3	2.6	dB
	Noise figure (16.5 - 24GHz)		2.0	2.3	dB
	Noise figure (24.5 - 30GHz)		2.2	2.5	dB
IS11I	Input return loss (12.5 - 16GHz) (27 – 30GHz)		2.5:1	3.0:1	
	Input return loss (16.5 - 26.5GHz)		2.0:1	2.5:1	
IS22I	Output return loss		2.0:1	2.5:1	
OIP3	3rd order intercept point @ Pout SCL < 8dBm from 16 to 30GHz	23	25		dBm
P1dB	Output power at 1dB gain compression	13	14		dBm
Id	Drain bias current		85	115	mA
Vd	Drain bias voltage		4		V

These values are representative of onboard measurements as defined on the drawing 96270 (see below).

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Electrical Characteristics (high current configuration)

Tamb = +25℃, Vd1=Vd2=Vd3 = +4V **Pads B, D = GND**

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	12.5		30	GHz
G	Linear Gain (12.5 - 24GHz)	23	26		dB
	Linear Gain (24.5 - 30GHz)	21	24		dB
ΔG	Gain flatness		±2		dB
NF	Noise figure (12.5 - 16GHz)		2.3	2.6	dB
	Noise figure (16.5 - 24GHz)		2.0	2.3	dB
	Noise figure (24.5 - 30GHz)		2.2	2.5	dB
IS11I	Input return loss (12.5 - 16GHz) (27 – 30GHz)		2.5:1	3.0:1	
	Input return loss (16.5 - 26.5GHz)		2.0:1	2.5:1	
IS22I	Output return loss		2.0:1	2.5:1	
OIP3	3rd order intercept point @ Pout SCL < 8dBm from 16 to 30GHz	24	26		dBm
P1dB	Output power at 1dB gain compression	14	15		dBm
Id	Drain bias current		115	150	mA
Vd	Drain bias voltage		4		V

These values are representative of onboard measurements as defined on the drawing 96270 (see below).

Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Pin	RF input power	10	dBm
Top	Operating temperature range	-40 to +85	℃
Tj	Junction temperature (2)	175	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

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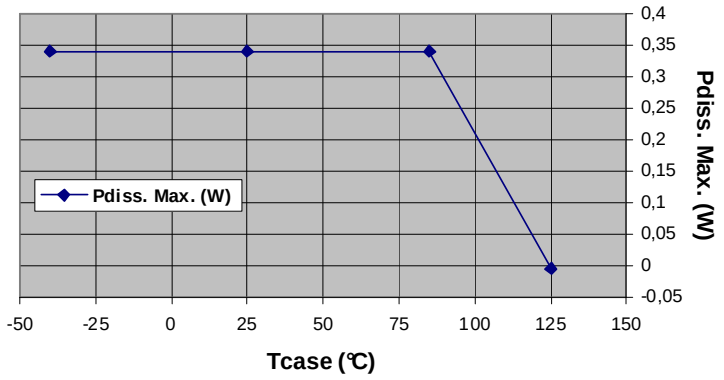
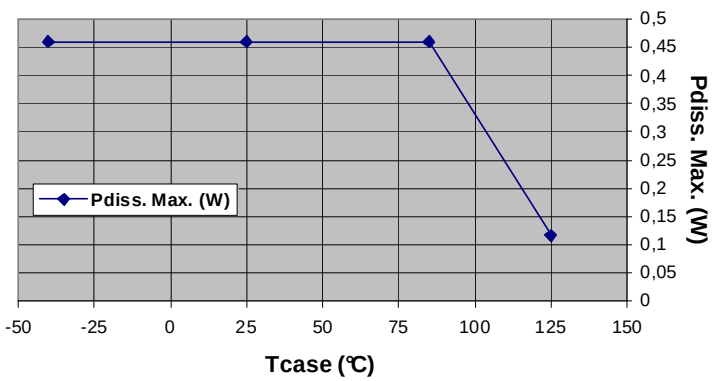
Thermal data based on board defined page 15

DEVICE THERMAL SPECIFICATION : CHA3688a-QDG low current config.				
Max. junction temperature (Tj max)			:	125 ℃
Max. continuous dissipated power @ Tcase=	85	℃	:	0,3 W
=> Pdiss derating above Tcase=	85	℃	:	8,6 mW/℃
Device thermal resistance (Rth)			:	116,4 ℃/W
Min. package back side operating temperature			:	-40 ℃
Max. package back side operating temperature			:	85 ℃
Min. storage temperature			:	-55 ℃
Max. storage temperature			:	125 ℃



DEVICE THERMAL SPECIFICATION : CHA3688a-QDG with BD grounded				
Max. junction temperature (Tj max)			:	139 ℃
Max. continuous dissipated power @ Tcase=	85	℃	:	0,5 W
=> Pdiss derating above Tcase=	85	℃	:	8,6 mW/℃
Device thermal resistance (Rth)			:	116,4 ℃/W
Min. package back side operating temperature			:	-40 ℃
Max. package back side operating temperature			:	85 ℃
Min. storage temperature			:	-55 ℃
Max. storage temperature			:	125 ℃



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Typical Package Sij parameters for low current configuration

Tamb = +25°C, Vd1=Vd2=Vd3= +4V, Id = 85 mA **Pads B, D not connected**

Freq (GHz)	dB(S11)	P(S11) (°)	dB(S12)	P(S12) (°)	dB(S21)	P (S21) (°)	dB(S22)	P(S22) (°)
2	-1,3	66	-63,8	-33	-67,2	-134	-1,4	61
3	-1,2	14	-62,8	61	-57,0	24	-1,5	0
4	-1,1	-34	-62,9	140	-57,9	30	-1,7	-60
5	-1,0	-79	-68,4	99	-31,8	-63	-2,4	-120
6	-0,9	-124	-61,8	-70	-13,3	-143	-4,8	-178
7	-1,3	-178	-59,6	71	1,2	118	-9,9	126
8	-2,6	117	-61,0	-1	9,1	24	-19,3	87
9	-4,8	42	-62,0	-111	15,9	-62	-23,9	-14
10	-5,6	-27	-59,3	164	19,5	-144	-14,5	-159
11	-5,3	-83	-53,6	134	22,0	142	-12,9	136
12	-4,8	-128	-52,4	94	23,7	74	-14,1	89
13	-4,8	-167	-55,4	43	24,8	13	-15,3	58
14	-5,2	157	-51,0	33	25,8	-44	-15,3	27
15	-6,1	122	-56,9	36	26,8	-101	-13,7	-6
16	-7,6	91	-57,5	176	27,0	-157	-12,2	-40
17	-9,4	56	-47,2	-157	27,0	151	-10,3	-70
18	-12,0	26	-51,8	92	27,1	101	-9,0	-111
19	-14,5	-6	-49,0	67	27,3	49	-8,8	-149
20	-17,2	-28	-58,8	30	26,8	0	-9,6	-179
21	-20,2	-34	-49,9	34	26,4	-46	-10,4	149
22	-16,7	-69	-49,0	40	25,9	-93	-13,6	130
23	-14,6	-107	-47,2	20	25,3	-140	-15,7	125
24	-13,3	-146	-48,4	-5	24,7	176	-15,7	117
25	-12,2	-175	-48,2	-3	24,2	129	-17,2	122
26	-10,5	161	-50,6	-12	23,7	86	-15,7	118
27	-8,6	130	-47,7	2	23,2	38	-13,7	102
28	-7,7	91	-45,5	-17	22,9	-9	-13,2	79
29	-7,7	53	-47,8	47	22,0	-60	-13,4	39
30	-6,4	2	-37,9	-51	21,1	-116	-14,9	-5
31	-4,9	-55	-42,9	-24	18,5	-176	-14,0	-55
32	-4,4	-106	-37,5	-65	14,5	134	-11,3	-96
33	-3,1	-141	-44,7	-110	10,9	84	-7,8	-133
34	-2,1	-172	-43,4	-69	6,4	38	-5,1	-162
35	-1,2	162	-46,5	27	1,3	-6	-3,5	173
36	-1,2	139	-34,6	-70	-4,4	-44	-2,3	150
37	-1,2	122	-33,9	-90	-10,7	-73	-1,6	131
38	-1,2	105	-32,7	-103	-17,8	-98	-1,3	113
39	-1,6	90	-38,1	-114	-24,8	-113	-1,6	93
40	-2,6	71	-39,0	-118	-32,8	-85	-2,8	75

Refer to the “definition of the Sij reference planes” section below.

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Typical Package Sij parameters for high current configuration

Tamb = +25°C, Vd1=Vd2=Vd3= +4V, Id = 115 mA **Pads B, D = GND**

Freq (GHz)	dB(S11)	P(S11) (°)	dB(S12)	P(S12) (°)	dB(S21)	P (S21) (°)	dB(S22)	P(S22) (°)
2	-1,3	66	-75,4	159	-77,1	115	-1,4	61
3	-1,2	14	-62,1	-168	-56,8	7	-1,5	0
4	-1,1	-34	-74,0	65	-57,0	6	-1,7	-61
5	-1,0	-79	-79,6	-146	-30,6	-61	-2,6	-120
6	-0,9	-124	-84,9	160	-12,4	-144	-5,0	-178
7	-1,3	-178	-63,2	24	1,8	118	-9,8	128
8	-2,7	117	-64,3	31	9,9	23	-20,6	92
9	-4,9	42	-73,9	84	16,6	-62	-27,6	-18
10	-5,7	-27	-56,5	-150	20,2	-145	-13,9	-168
11	-5,3	-83	-57,7	126	22,7	142	-12,4	130
12	-4,8	-128	-54,9	86	24,3	74	-13,5	84
13	-4,7	-167	-55,2	30	25,4	13	-14,8	53
14	-5,1	158	-53,6	116	26,4	-44	-15,4	21
15	-6,2	122	-48,5	-47	27,2	-100	-13,0	-8
16	-7,4	91	-57,7	140	27,6	-156	-11,6	-44
17	-9,4	54	-55,6	135	27,6	152	-9,8	-75
18	-11,6	27	-51,6	119	27,7	103	-8,7	-112
19	-14,0	-5	-51,0	75	27,9	52	-8,5	-150
20	-16,4	-29	-48,8	58	27,5	2	-9,0	179
21	-19,3	-48	-49,5	59	27,2	-44	-10,0	148
22	-16,8	-72	-48,5	29	26,7	-92	-13,0	128
23	-15,0	-109	-47,6	25	26,2	-139	-15,5	117
24	-13,7	-149	-49,0	-17	25,4	177	-15,9	112
25	-12,0	-176	-47,4	3	24,9	131	-18,0	116
26	-10,3	158	-48,6	2	24,5	87	-16,6	113
27	-9,0	129	-47,1	-24	23,9	38	-14,4	102
28	-8,3	91	-38,4	-21	23,4	-7	-14,2	75
29	-7,5	51	-42,0	16	22,8	-58	-14,2	39
30	-6,3	2	-40,8	-34	22,0	-115	-14,9	-6
31	-5,1	-57	-41,5	-56	19,4	-175	-14,6	-54
32	-4,5	-107	-37,7	-58	15,3	134	-11,4	-98
33	-3,0	-142	-43,9	-115	11,8	84	-7,8	-133
34	-2,1	-173	-50,3	-135	7,2	38	-5,2	-163
35	-1,2	162	-39,6	-15	2,1	-6	-3,6	172
36	-1,2	139	-34,6	-45	-3,9	-45	-2,3	148
37	-1,4	122	-32,7	-105	-10,2	-74	-1,6	129
38	-1,3	105	-38,2	-109	-16,9	-92	-1,4	112
39	-1,7	90	-38,3	-142	-22,1	-91	-1,8	92
40	-2,4	70	-39,4	-105	-25,1	-73	-2,1	75

Refer to the “definition of the Sij reference planes” section below.

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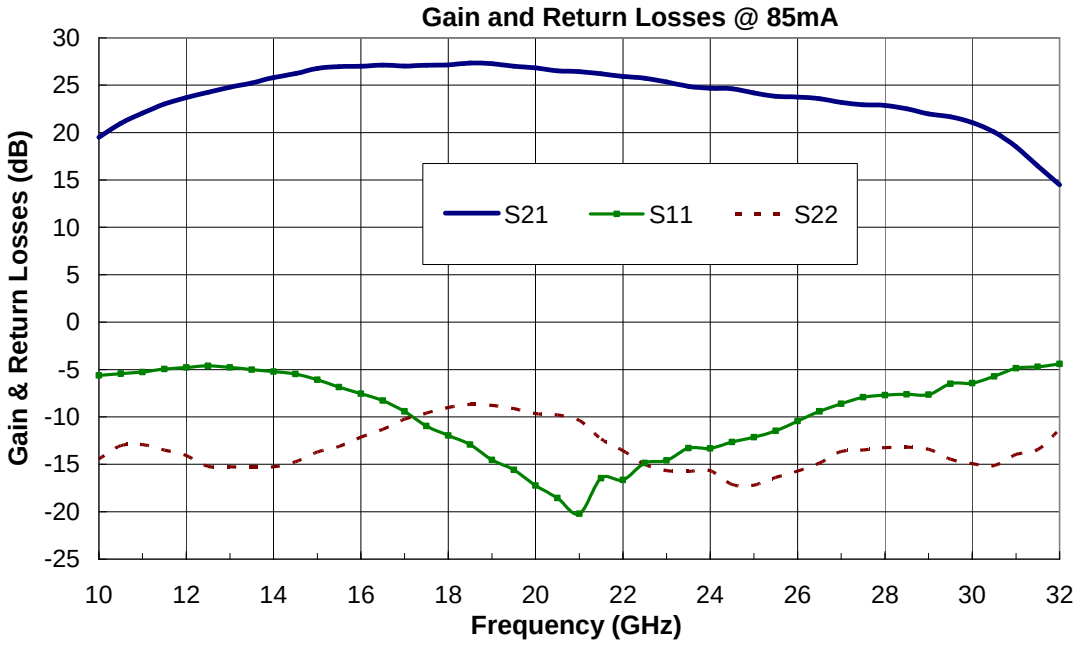
Typical Measured Performance

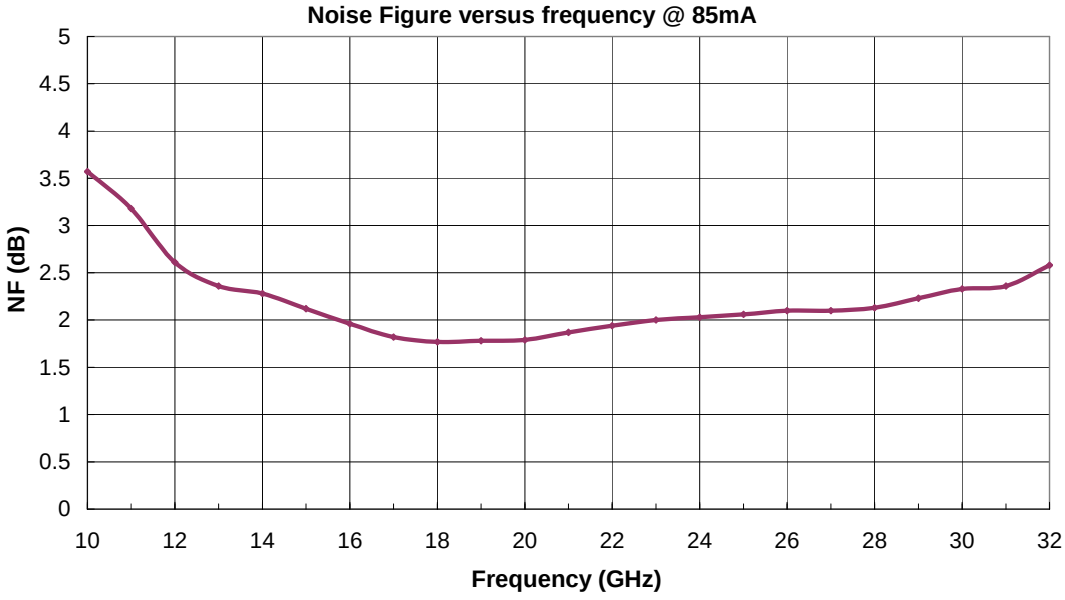
Tamb = +25°C, Vd1=Vd2=Vd3= +4V

Id = 85mA for pads B, D not connected

Id = 115mA for pads B, D = GND

Measurements in the package access planes, using the proposed land pattern & board 96270.





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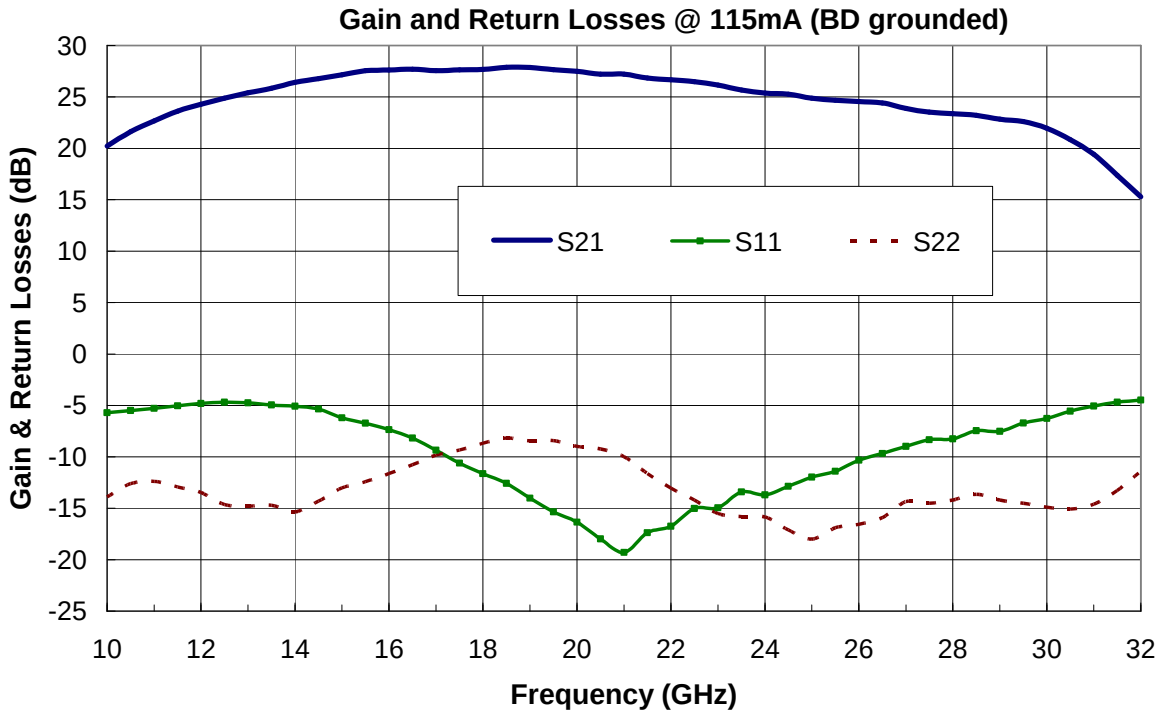

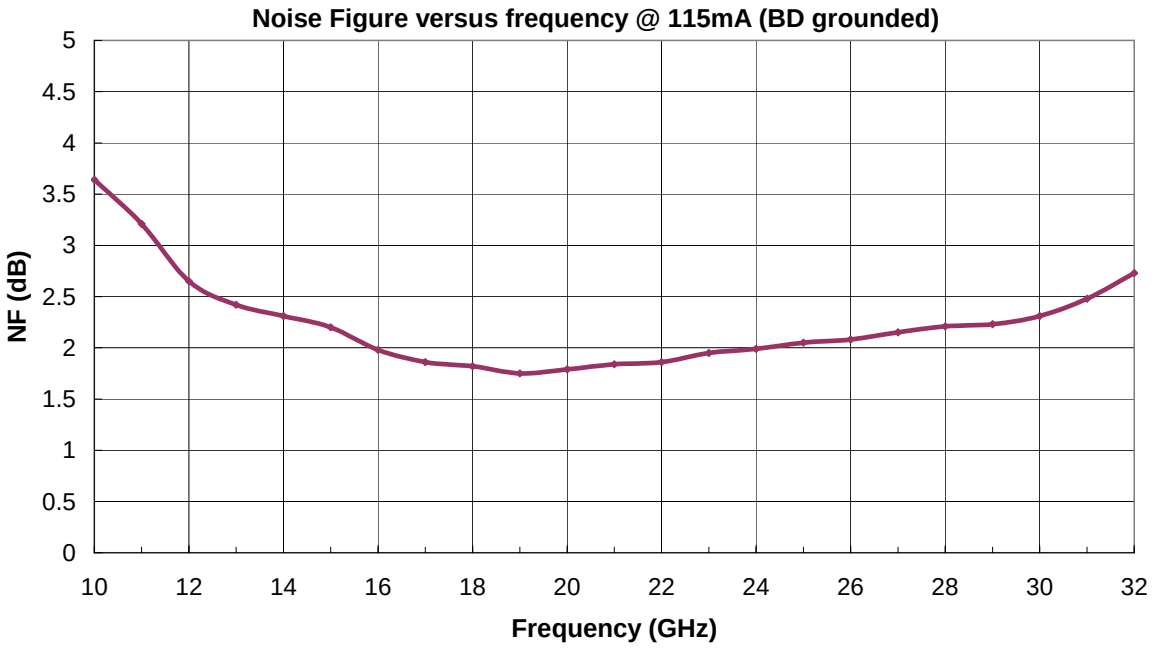

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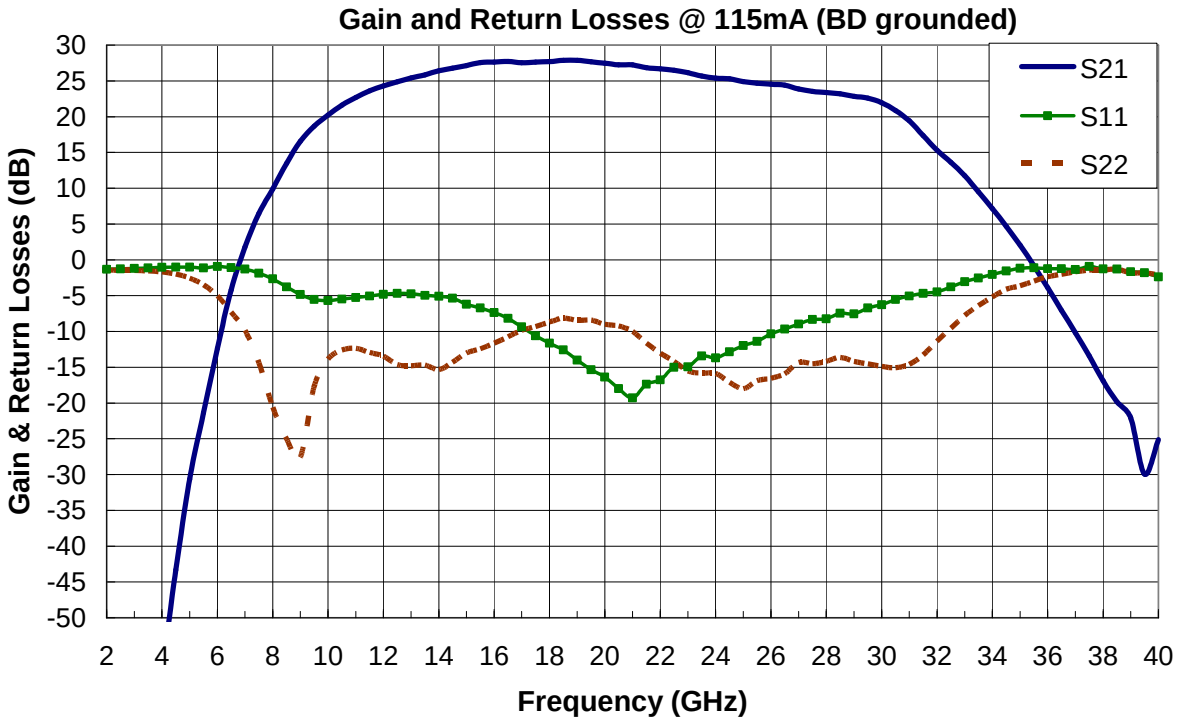

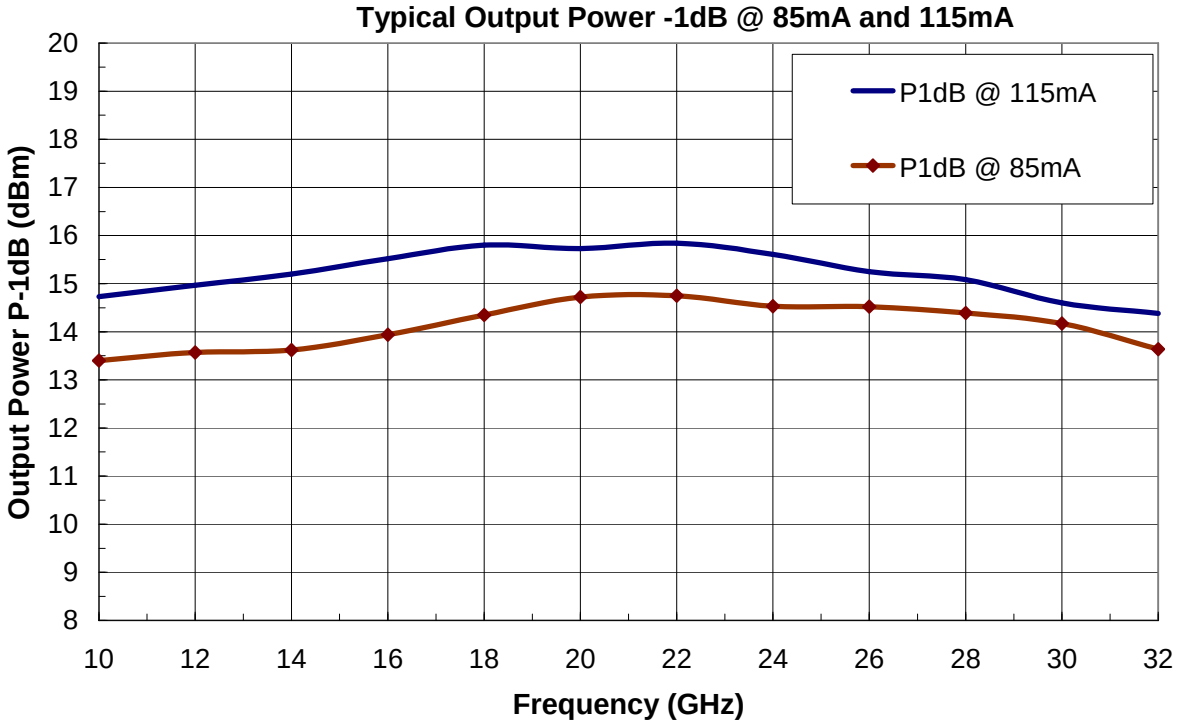

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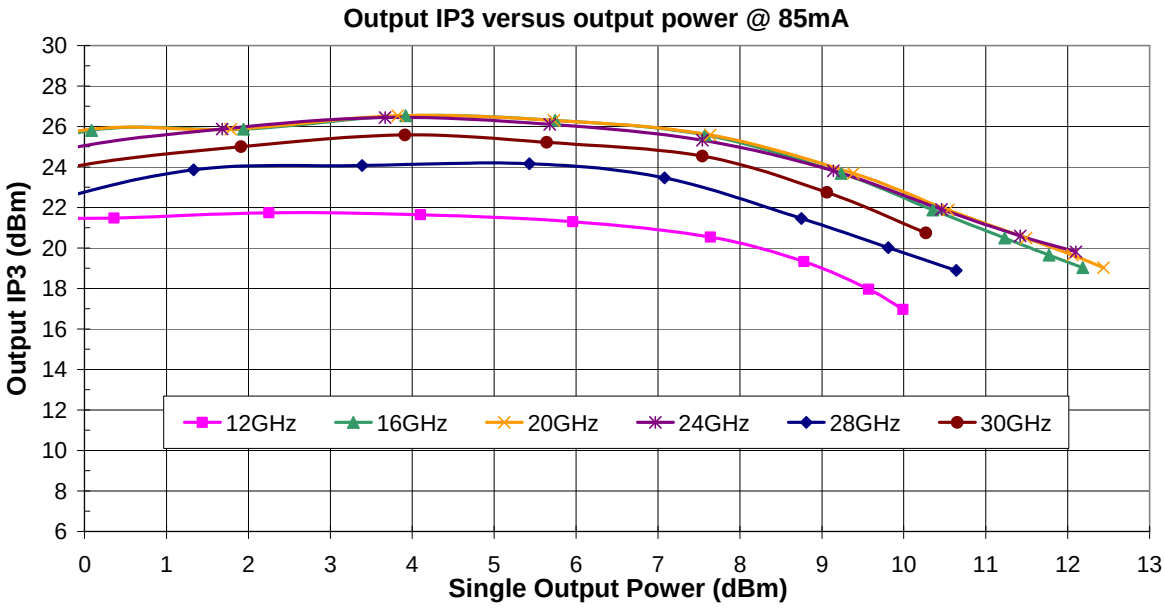

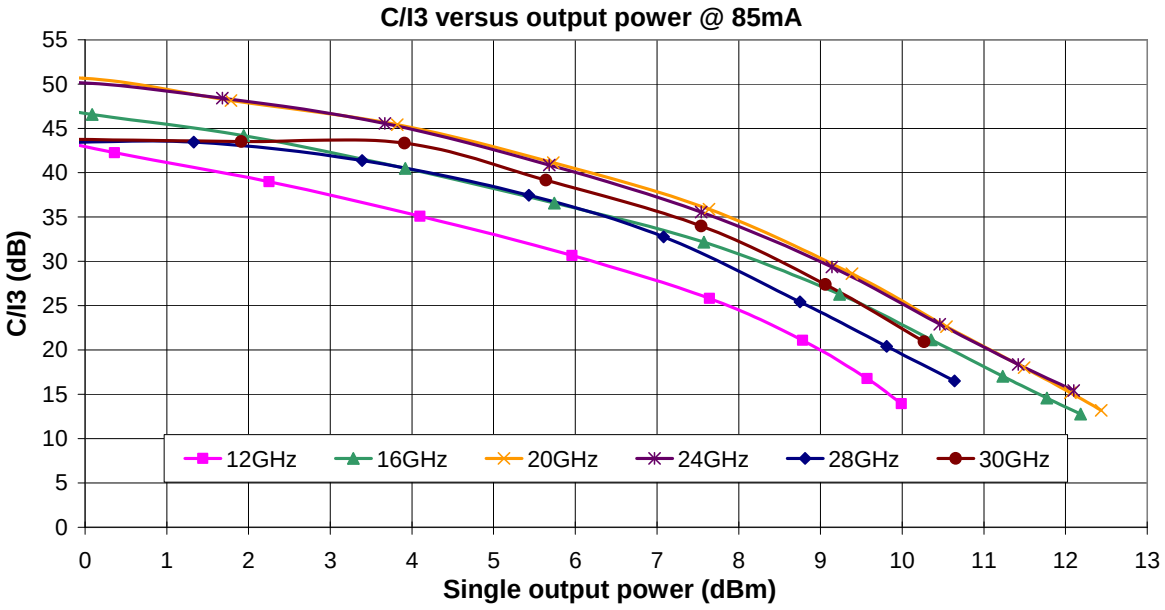

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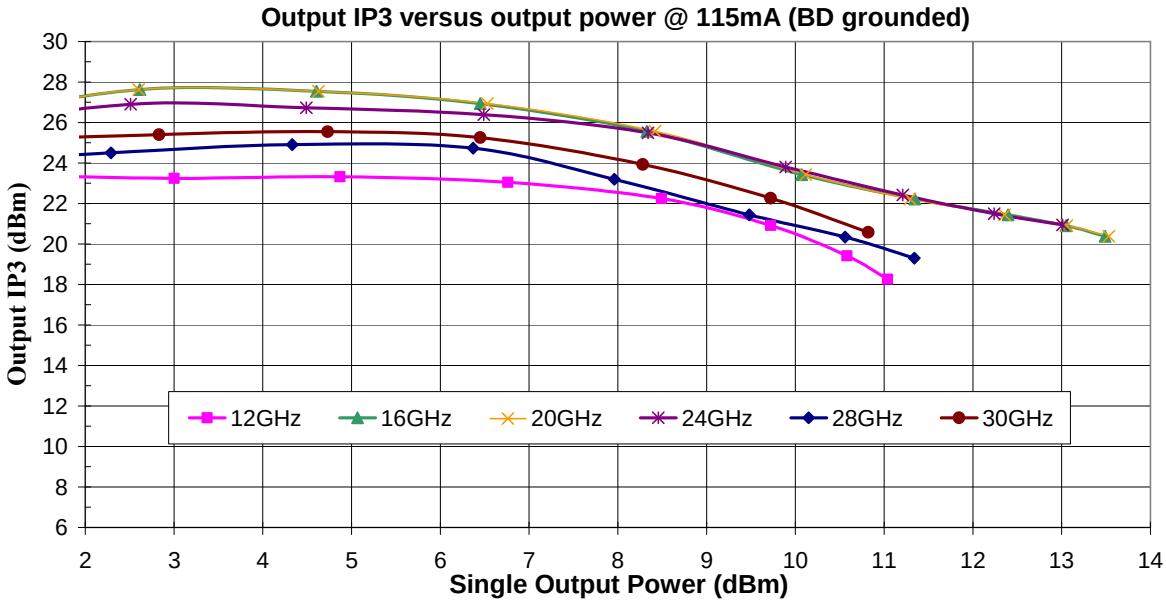

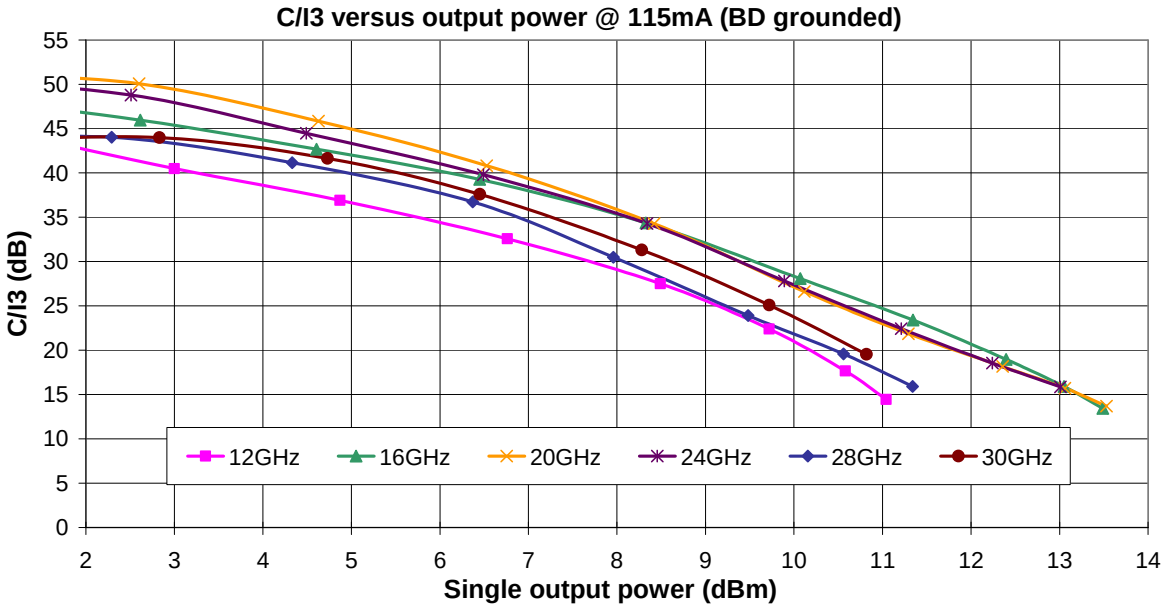

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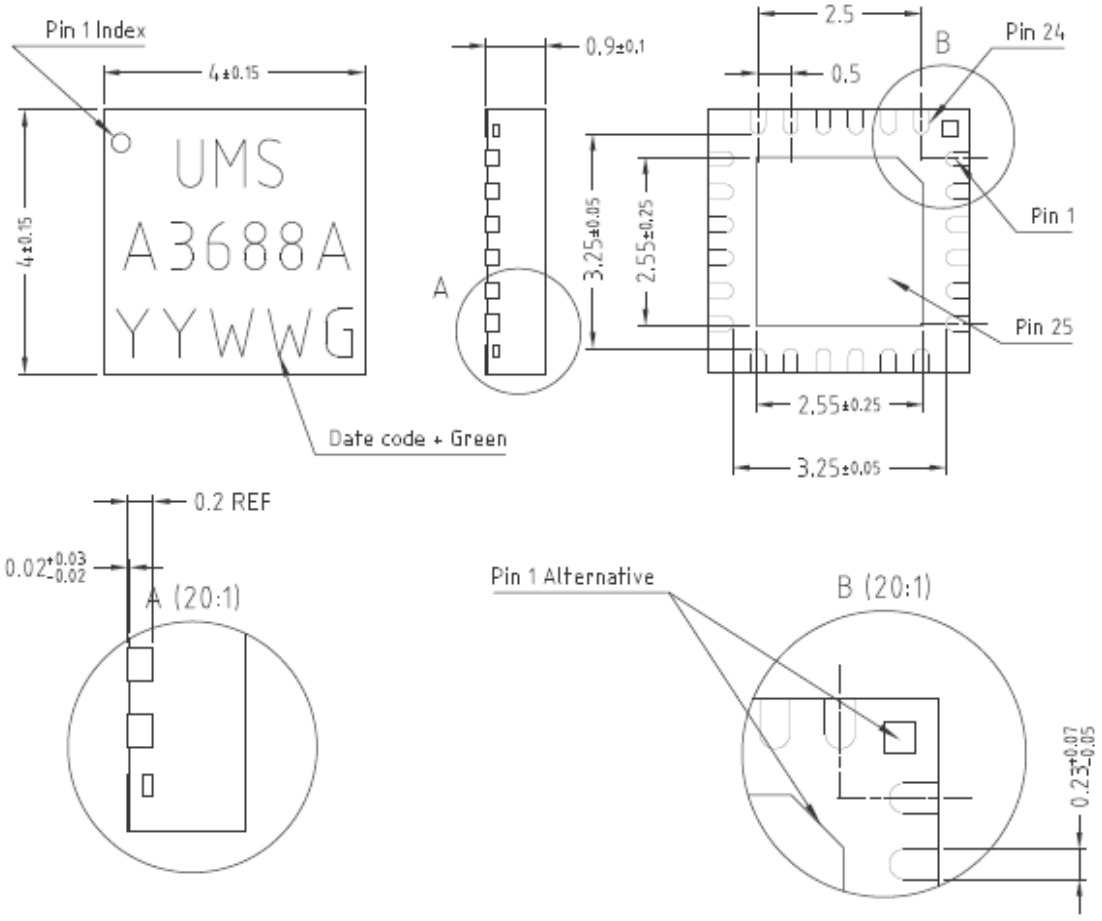
Package outline:



Matt tin, Lead Free	(Green)	1-	NC	13-	GND
Units	mm	2-	GND	14-	GND
From the standard	JEDEC MO-220	3-	GND	15-	RF OUT
	(VGGD-6 / VGGD-8)	4-	RF IN	16-	GND
25- GND		5-	GND	17-	GND
		6-	GND	18-	NC
		7-	NC	19-	Vd3
		8-	NC	20-	NC
		9-	B	21-	Vd2
		10-	NC	22-	NC
		11-	D	23-	Vd1
		12-	NC	24-	NC

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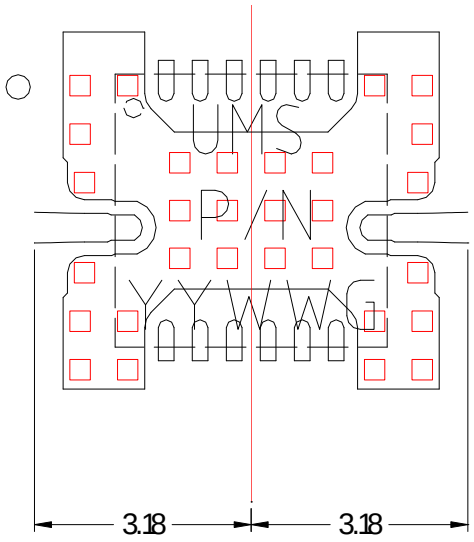
Definition of the Sij reference planes

The reference planes are defined from the footprint of the recommended characterization board 96270 shown below.
The reference is the symmetrical axis of the package. The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij incorporates this land pattern.



SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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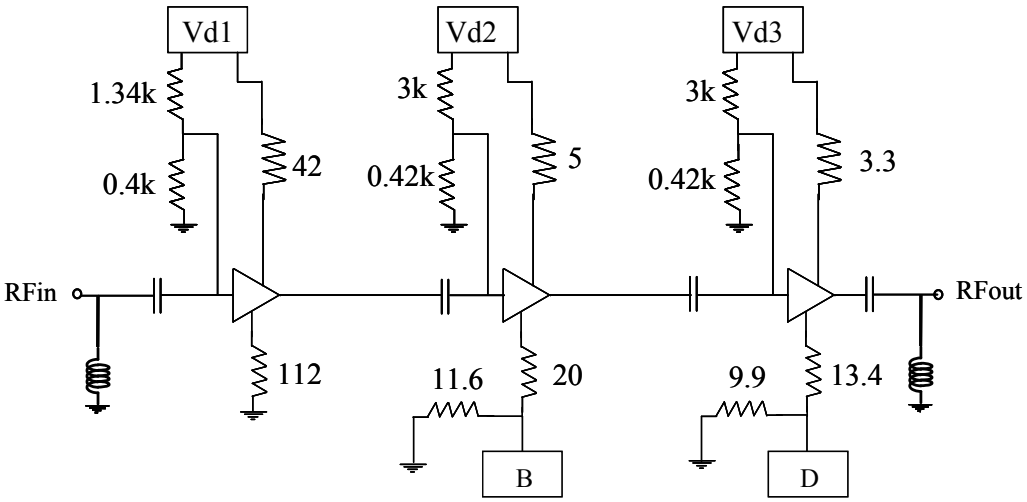
Package biasing options

This chip is self-biased, and flexibility is provided by the access to number of leads. The internal DC electrical schematic is given in order to use these leads in a safe way.



We propose two standard biasing:

Low Noise and low consumption: Vd = 4V and B & D leads non connected (NC).
Idd = 85mA & Pout-1dB = 14dBm Typical.

Low Noise and higher output power: Vd = 4V and B, D grounded.
Idd = 115mA & Pout-1dB = 15dBm Typical.

Note

Due to ESD protection circuits, RFin and RFout are DC grounded and an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

The DC connections (Vd1, Vd2 and Vd3) do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (typically 10nF) on the PC board, as close as possible to the package.

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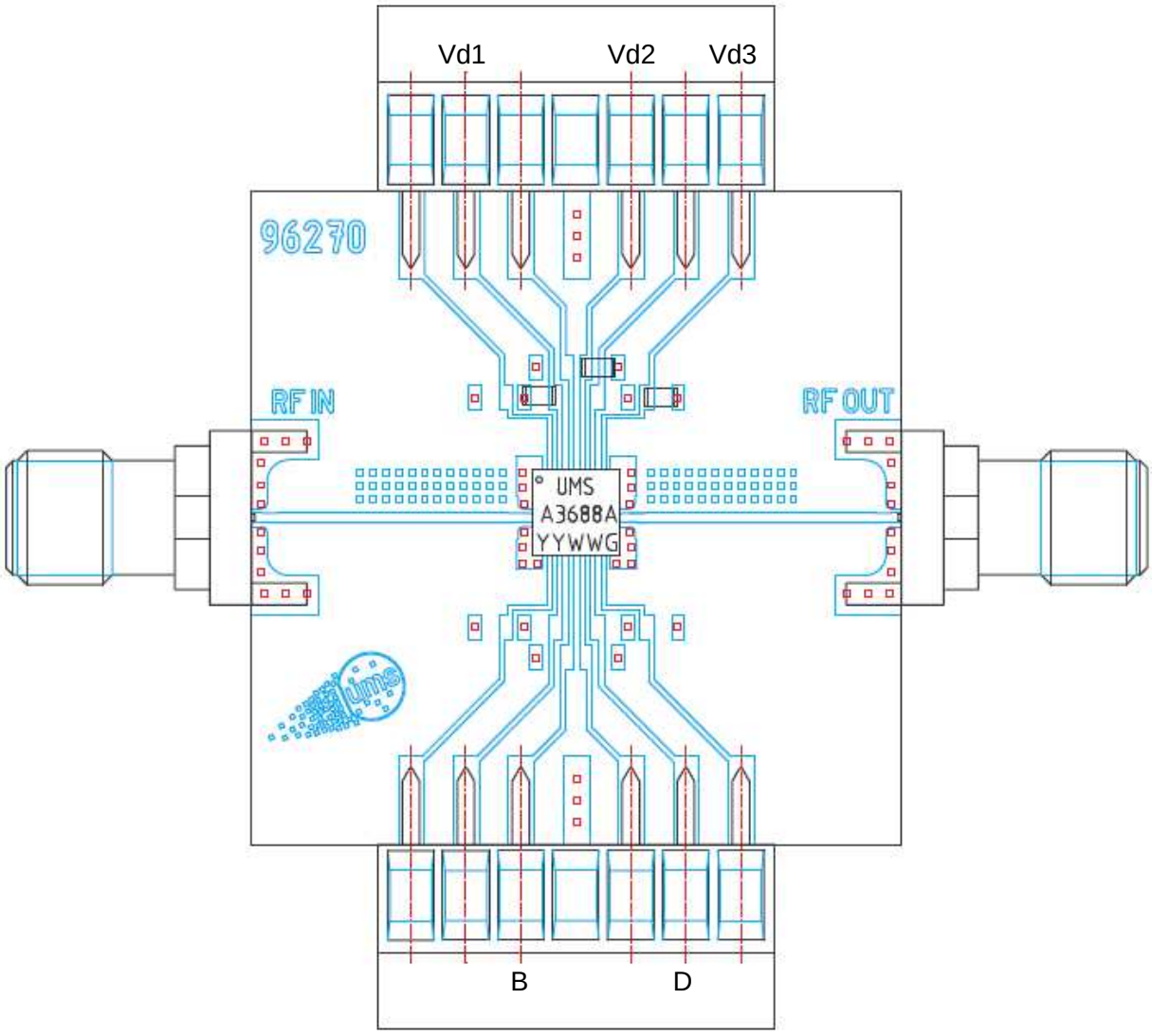
Proposed Assembly board “96270” for the 24L-QFN4x4 products characterization.

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.

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Ordering Information

QFN 4x4 RoHS compliant package: CHA3688aQDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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