12.5-30GHz Low Noise Amplifier

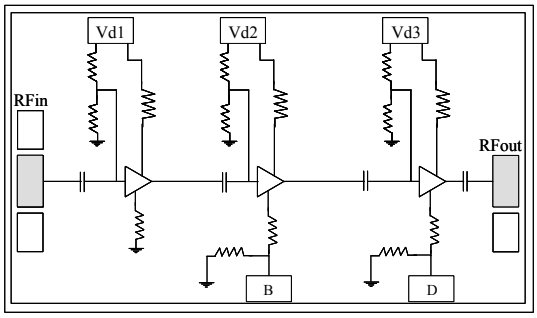
GaAs Monolithic Microwave IC

Description

The CHA3689 is a three-stage self biased wide band monolithic low noise amplifier.

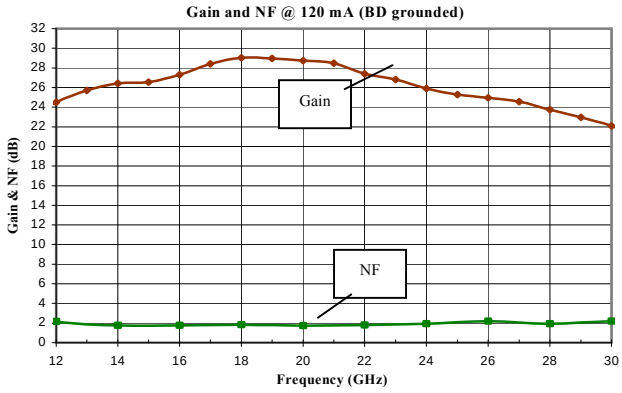
The circuit is manufactured with a standard P-HEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in chip form.



Main Features

- Broadband performance 12.5-30GHz
- 2.0dB noise figure
- 26dB gain (12.5-26GHz)
- 26dBm output IP3 (18-30GHz)
- Low DC power consumption
- Chip size: 2,45 x 1,21 x 0,1 mm



On wafer typical measurements

Main Characteristics

Tamb = +25°C, Vd1=Vd2=Vd3 = +4V Pads B, D = GND (High current configuration)

Symbol	Parameter	Min	Typ	Max	Unit
NF	Noise figure		2.0	2.5	dB
G	Gain	23	26		dB
P1dB	Output power at 1dB gain compression	14	15		dBm

ESD Protections : Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics (low current configuration)

These values are representative on wafer measurements that are made without bonding wires at the RF ports.

Tamb = +25°C, Vd1=Vd2=Vd3= +4V **Pads B, D = not connected**

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	12.5		30	GHz
G	Gain (12.5 - 24GHz)	23	26		dB
	Gain (24.5 - 30GHz)	20	22		dB
ΔG	Gain flatness (12.5 - 24GHz)		±2.5		dB
	Gain flatness (24.5 - 30GHz)		±2		dB
NF	Noise figure (12.5 - 24GHz)		1.8	2.3	dB
	Noise figure (24.5 - 30GHz)		2.0	2.5	dB
S11	Input return loss (12.5 - 16GHz) (27 - 30GHz)		3.0:1	3.5:1	
	Input return loss (16 - 27GHz)		2.0:1	2.5:1	
S22	Output return loss		2.5:1	3.0:1	
OIP3	3rd order intercept point (18 – 30GHz)	23	24		dBm
P1dB	Output power at 1dB gain compression	13	14		dBm
Id	Drain bias current		90	120	mA
Vd	Drain bias voltage		4		V

Electrical Characteristics (high current configuration)

Tamb = +25°C, Vd1=Vd2=Vd3 = +4V **Pads B, D = GND**

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	12.5		30	GHz
G	Gain (12.5 - 24GHz)	24	27		dB
	Gain (24.5 - 30GHz)	21	23		dB
ΔG	Gain flatness (12.5 - 24GHz)		±2.5		dB
	Gain flatness (24.5 - 30GHz)		±2		dB
NF	Noise figure (12.5 - 24GHz)		1.9	2.4	dB
	Noise figure (24.5 - 30GHz)		2.1	2.6	dB
S11	Input return loss (12.5 - 16GHz) (27 - 30GHz)		3.0:1	3.5:1	
	Input return loss (16 - 27GHz)		2.0:1	2.5:1	
S22	Output return loss		2.5:1	3.0:1	
OIP3	3rd order intercept point (18 – 30GHz)	25	26		dBm
P1dB	Output power at 1dB gain compression	14	15		dBm
Id	Drain bias current		120	150	mA
Vd	Drain bias voltage		4		V

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Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Pin	RF input power	10	dBm
Top	Operating temperature range	-40 to +85	℃
Tj	Junction temperature	175	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

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Typical Chip on wafer Sij parameters for low current configuration

Tamb = +25°C, Vd1=Vd2=Vd3= +4V, Id = 90 mA **Pads B, D = not connected**

Freq (GHz)	dB(S11)	P(S11) (°)	dB(S12)	P(S12) (°)	dB(S21)	P (S21) (°)	dB(S22)	P(S22) (°)
2	-0,1	-23	-67,3	-16	-65,4	67	-0,2	-30
3	-0,1	-35	-61,6	-160	-70,6	-166	-0,3	-47
4	-0,2	-48	-81,4	132	-56,0	10	-0,5	-66
5	-0,2	-64	-60,5	-176	-33,7	-32	-1,3	-90
6	-0,3	-81	-63,3	-15	-16,5	-89	-3,3	-118
7	-0,5	-106	-59,5	-2	-1,4	-160	-8,0	-147
8	-1,5	-141	-61,4	73	7,4	123	-14,9	-143
9	-3,9	170	-55,2	-83	15,1	54	-19,6	-142
10	-6,7	110	-59,4	-68	19,5	-20	-14,6	-73
11	-6,5	53	-61,7	-76	22,2	-81	-11,6	-108
12	-5,0	7	-51,4	-156	23,9	-137	-12,2	-134
13	-4,5	-26	-51,6	176	25,1	173	-12,5	-153
14	-5,1	-53	-49,3	-136	25,8	126	-13,1	-178
15	-5,9	-67	-61,1	-1	26,2	85	-15,0	155
16	-5,9	-81	-44,5	67	27,3	49	-12,3	147
17	-8,0	-102	-47,5	60	27,7	7	-12,3	121
18	-8,9	-118	-47,7	20	28,7	-30	-9,9	101
19	-12,8	-137	-52,1	7	28,5	-72	-8,1	78
20	-15,3	-150	-49,2	10	28,4	-108	-7,8	56
21	-20,3	-172	-59,8	-56	27,9	-147	-7,3	36
22	-25,7	170	-72,9	24	26,9	180	-8,2	19
23	-26,6	105	-55,4	71	26,2	147	-8,8	9
24	-24,2	47	-54,5	41	25,1	116	-9,3	1
25	-22,4	43	-54,8	13	24,4	88	-10,2	-8
26	-18,9	57	-61,9	-85	24,1	60	-12,2	3
27	-12,0	62	-47,8	177	24,0	26	-10,1	8
28	-9,2	45	-63,2	-179	23,0	-4	-9,9	-1
29	-7,1	27	-48,4	99	22,2	-35	-9,6	-1
30	-5,4	15	-49,5	-2	21,2	-67	-9,0	-2
31	-3,5	0	-47,3	-75	19,8	-100	-7,9	-1
32	-2,7	-15	-47,6	-133	17,9	-133	-6,7	-9
33	-2,6	-29	-45,0	-160	15,5	-162	-6,1	-14
34	-2,6	-38	-49,3	40	12,9	172	-5,4	-22
35	-2,4	-46	-38,8	98	10,7	149	-4,9	-26
36	-2,4	-57	-45,5	124	8,2	129	-4,4	-34
37	-2,3	-64	-51,5	114	6,2	109	-4,0	-40
38	-2,7	-73	-46,1	-96	4,1	92	-4,0	-48
39	-3,2	-76	-56,0	142	2,4	75	-4,0	-54
40	-3,6	-87	-47,4	153	1,1	56	-4,1	-62

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Typical Chip on wafer Sij parameters for high current configuration

Tamb = +25°C, Vd1=Vd2=Vd3= +4V, Id = 120 mA **Pads B, D = GND**

Freq (GHz)	dB(S11)	P(S11) (°)	dB(S12)	P(S12) (°)	dB(S21)	P(S21) (°)	dB(S22)	P(S22) (°)
2	-0,1	-23	-62,8	-51	-59,9	-140	-0,2	-30
3	-0,1	-35	-60,7	9	-58,1	-121	-0,3	-46
4	-0,1	-48	-63,5	-105	-54,9	31	-0,5	-65
5	-0,2	-63	-72,0	63	-33,8	-31	-1,2	-88
6	-0,3	-80	-74,5	-171	-15,8	-87	-3,2	-115
7	-0,5	-105	-66,5	137	-0,7	-159	-8,0	-142
8	-1,5	-140	-57,0	-133	8,1	124	-14,6	-133
9	-3,8	171	-65,6	-97	15,7	55	-17,5	-128
10	-6,6	112	-53,8	-100	20,1	-18	-13,4	-77
11	-6,5	55	-53,3	-131	22,7	-80	-10,7	-109
12	-5,0	9	-52,2	-152	24,5	-136	-11,4	-134
13	-4,6	-25	-59,8	165	25,7	174	-11,7	-152
14	-5,2	-51	-49,6	84	26,4	127	-13,3	-179
15	-6,7	-67	-45,7	147	26,6	86	-14,6	161
16	-6,6	-76	-44,7	79	27,3	51	-13,2	148
17	-7,1	-100	-48,0	85	28,4	11	-12,3	125
18	-9,1	-115	-60,5	63	29,0	-27	-10,2	107
19	-12,0	-134	-59,0	-25	29,0	-68	-8,4	78
20	-14,8	-142	-61,1	131	28,8	-104	-8,1	56
21	-18,5	-171	-56,6	-81	28,5	-142	-7,5	36
22	-23,6	150	-62,0	18	27,4	-176	-8,0	18
23	-26,6	101	-57,1	174	26,8	152	-8,7	6
24	-23,6	58	-59,9	150	25,9	121	-9,3	-1
25	-21,8	48	-56,2	22	25,3	93	-10,2	-10
26	-17,3	54	-56,5	-113	24,9	64	-11,9	-1
27	-12,9	54	-51,9	139	24,6	32	-10,8	1
28	-10,1	42	-49,9	-2	23,7	1	-10,1	-6
29	-7,3	27	-49,0	33	23,0	-30	-10,2	-3
30	-5,6	12	-44,7	120	22,1	-61	-9,4	-4
31	-4,0	1	-53,1	29	20,8	-95	-8,4	-3
32	-3,1	-14	-53,6	128	19,1	-129	-7,2	-8
33	-2,8	-27	-59,1	-80	16,6	-159	-6,2	-12
34	-2,8	-37	-48,0	99	14,0	174	-5,6	-20
35	-2,3	-46	-47,2	-155	11,6	151	-4,8	-24
36	-2,5	-55	-43,6	141	9,1	130	-4,3	-32
37	-2,3	-65	-63,3	109	6,8	110	-4,0	-39
38	-3,1	-75	-45,0	179	4,5	91	-3,9	-43
39	-3,3	-77	-46,0	101	2,4	75	-3,9	-50
40	-3,9	-85	-31,5	144	0,7	57	-3,5	-54

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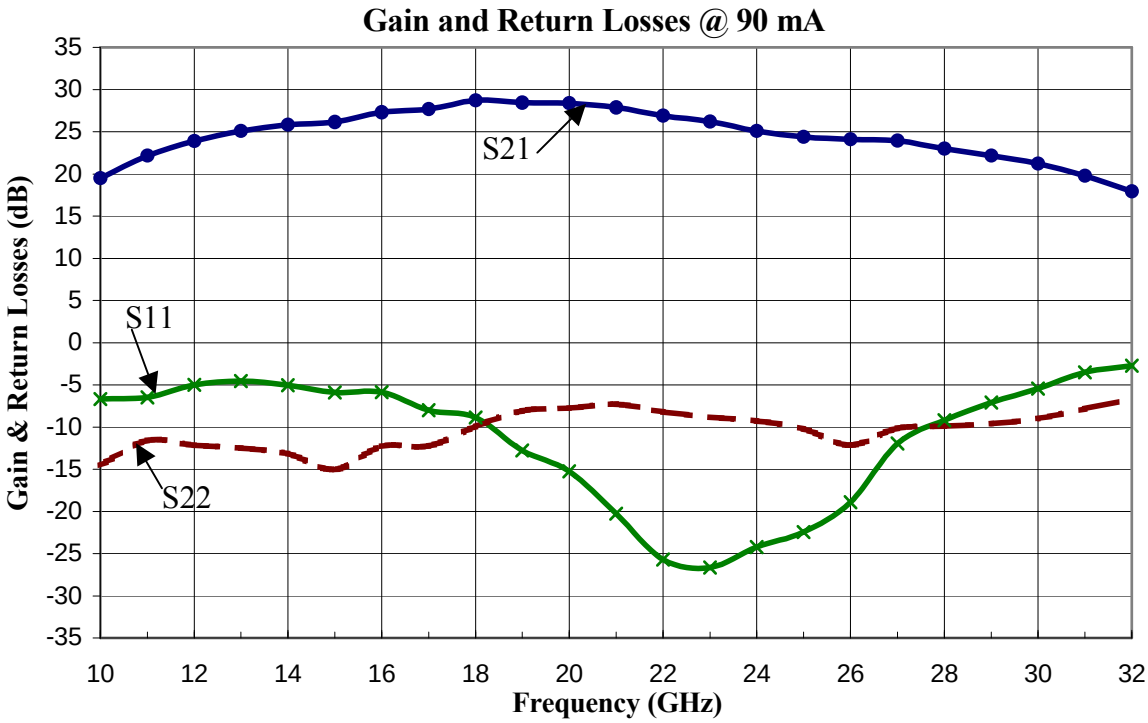
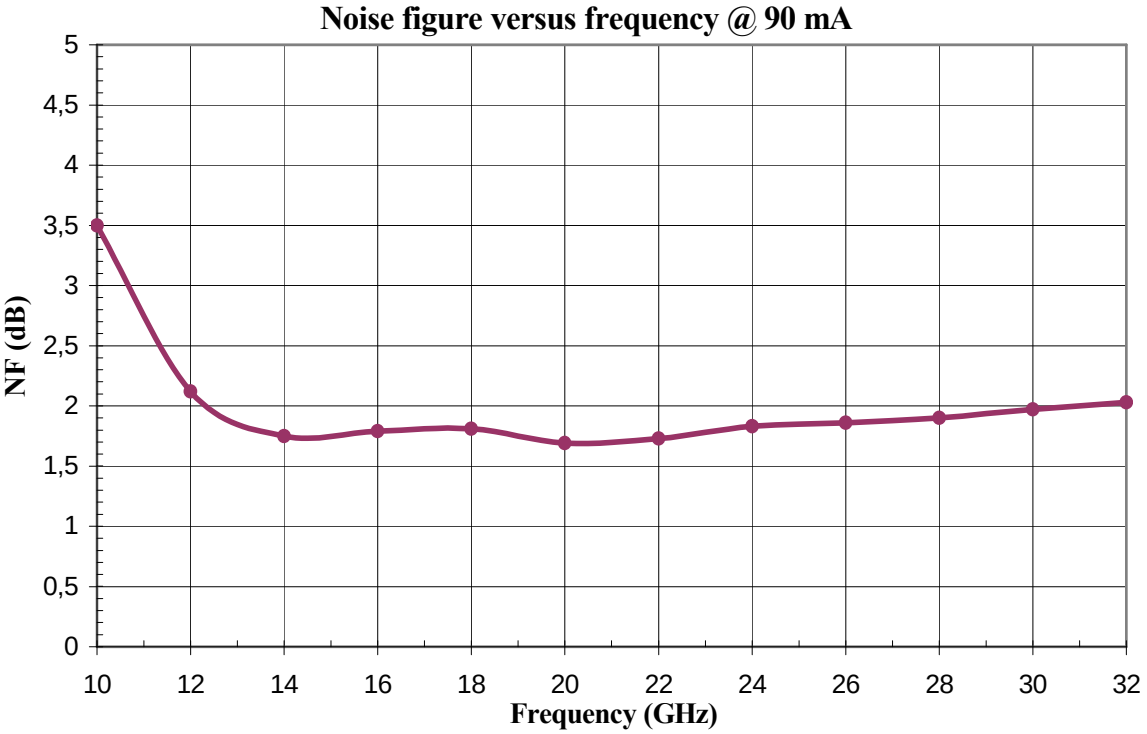
Typical Measured Performance

Tamb = +25°C, Vd1=Vd2=Vd3= +4V

Id = 90 mA / Id = 120 mA for pads B, D = GND

Measurements on wafer (without bonding wires at the RF ports)





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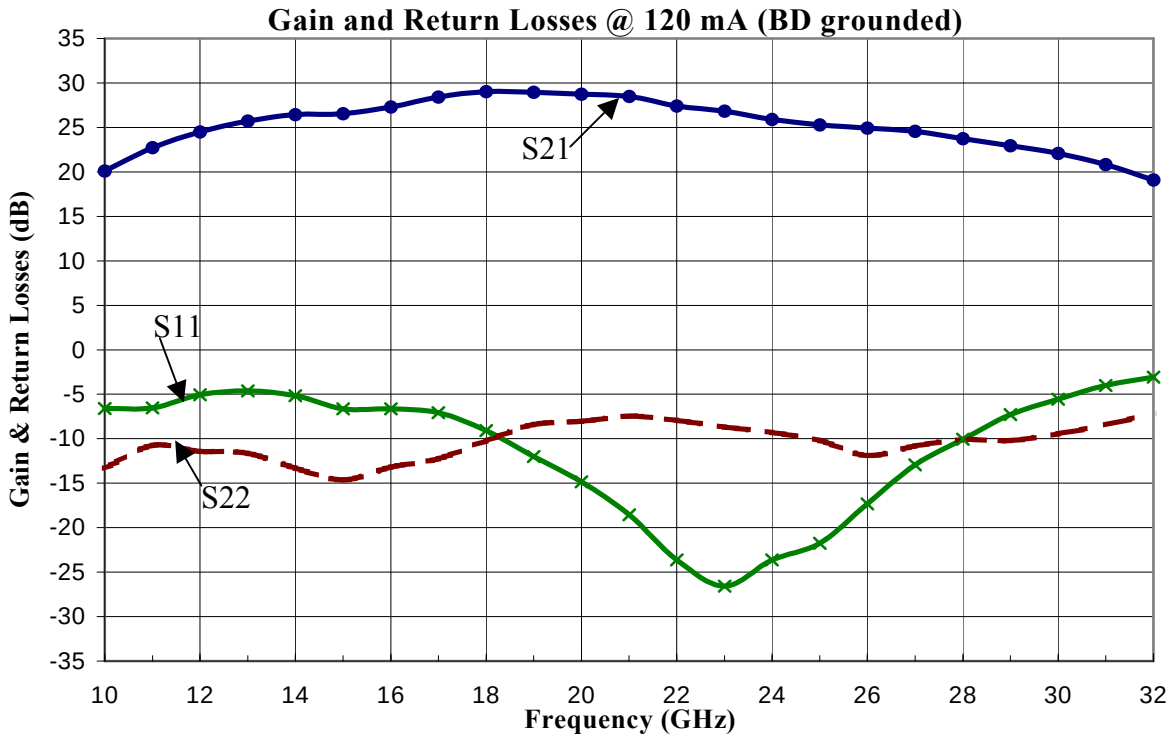

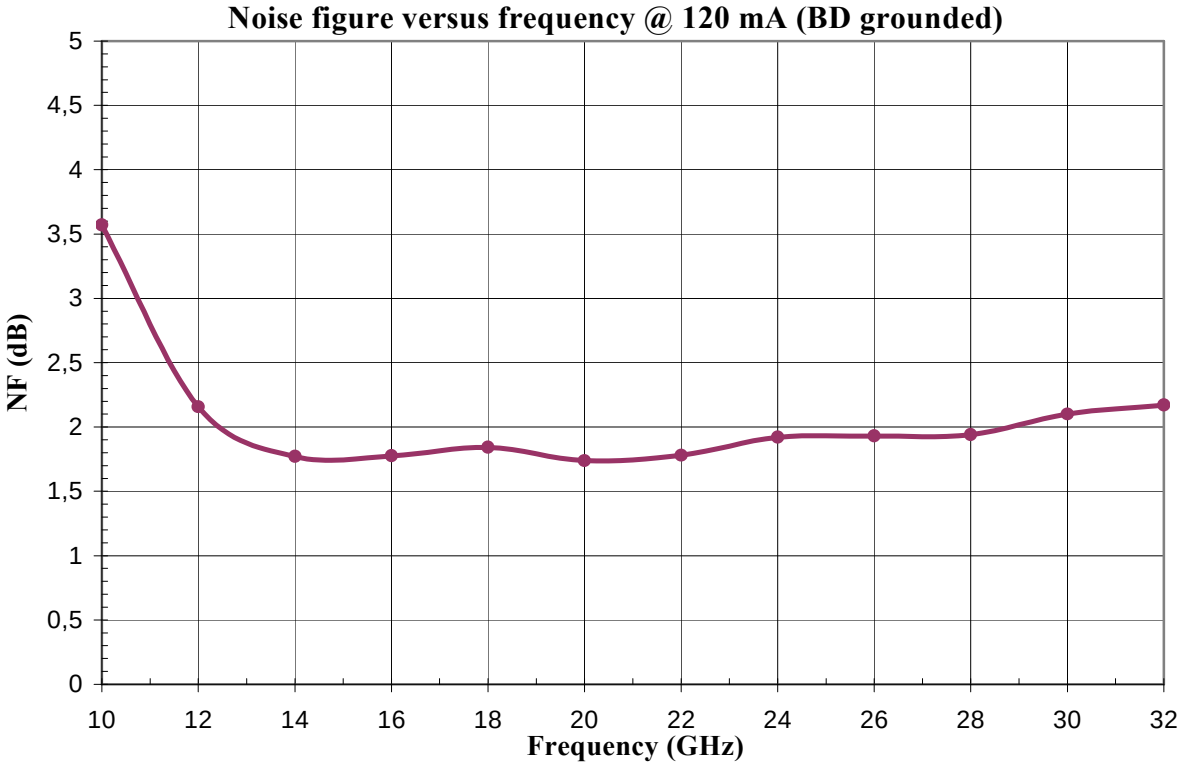

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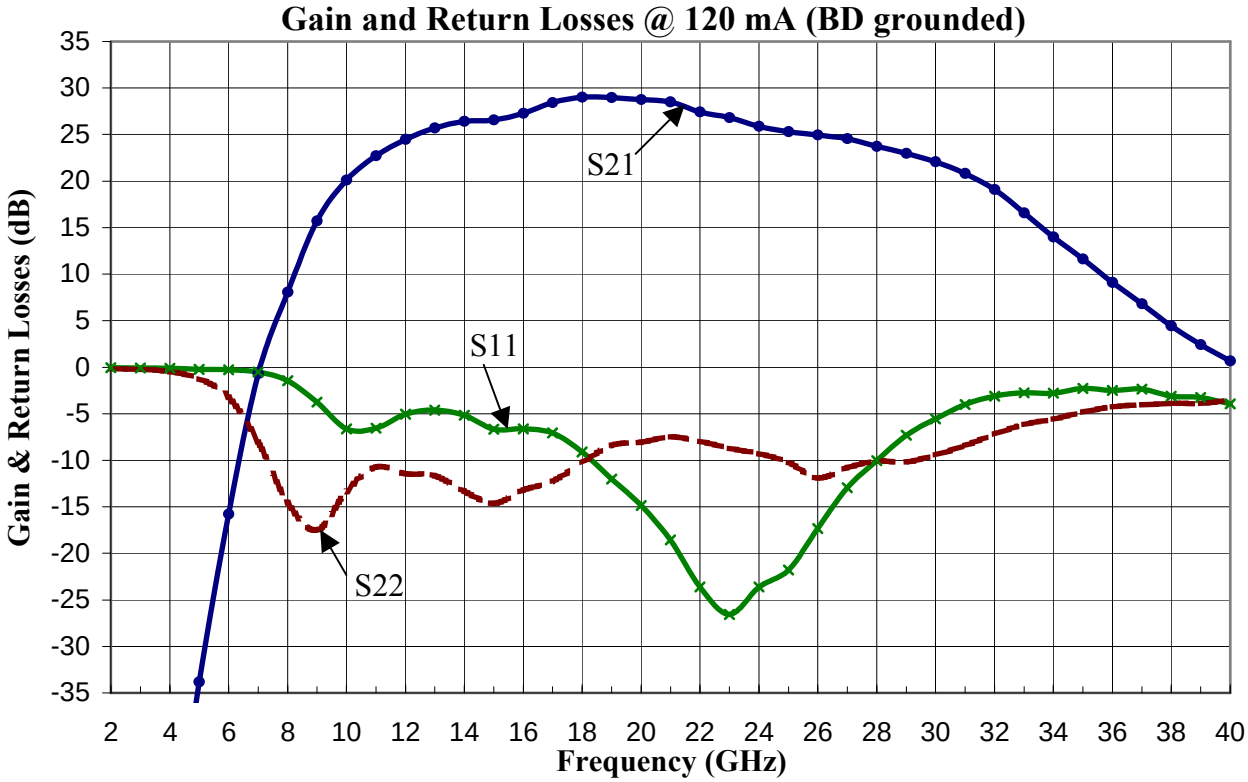

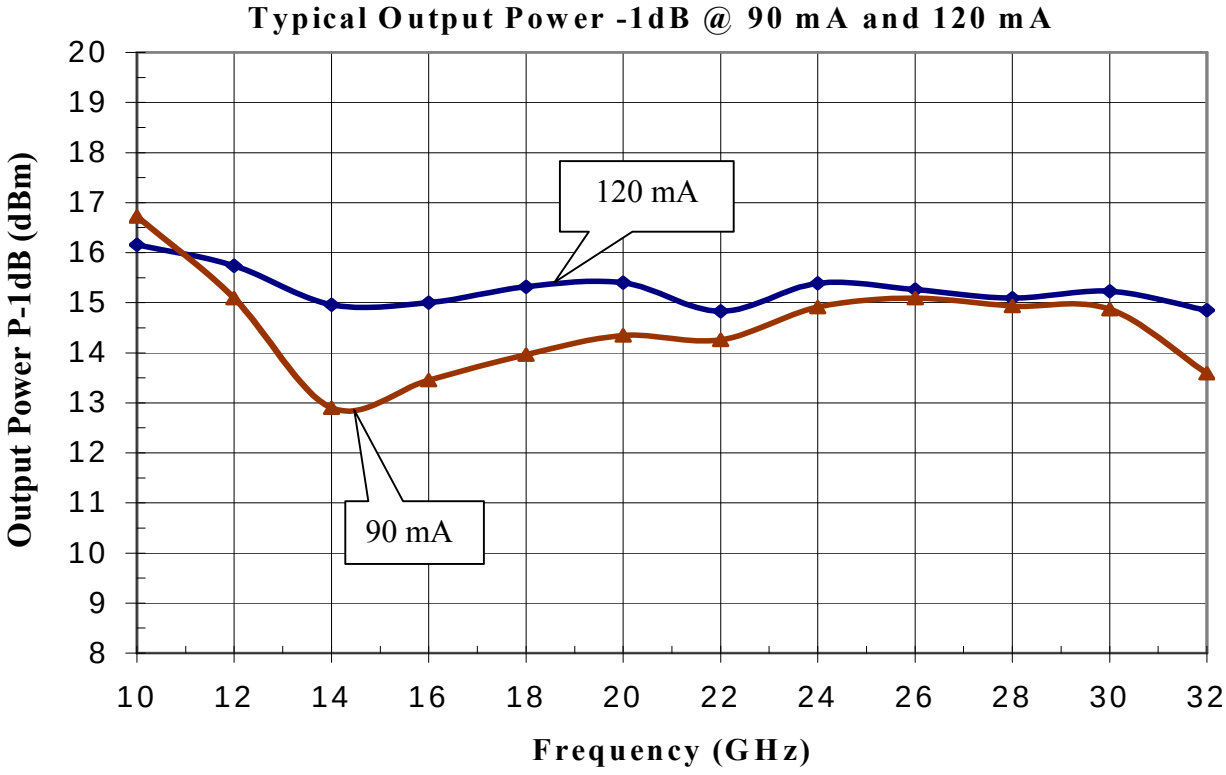

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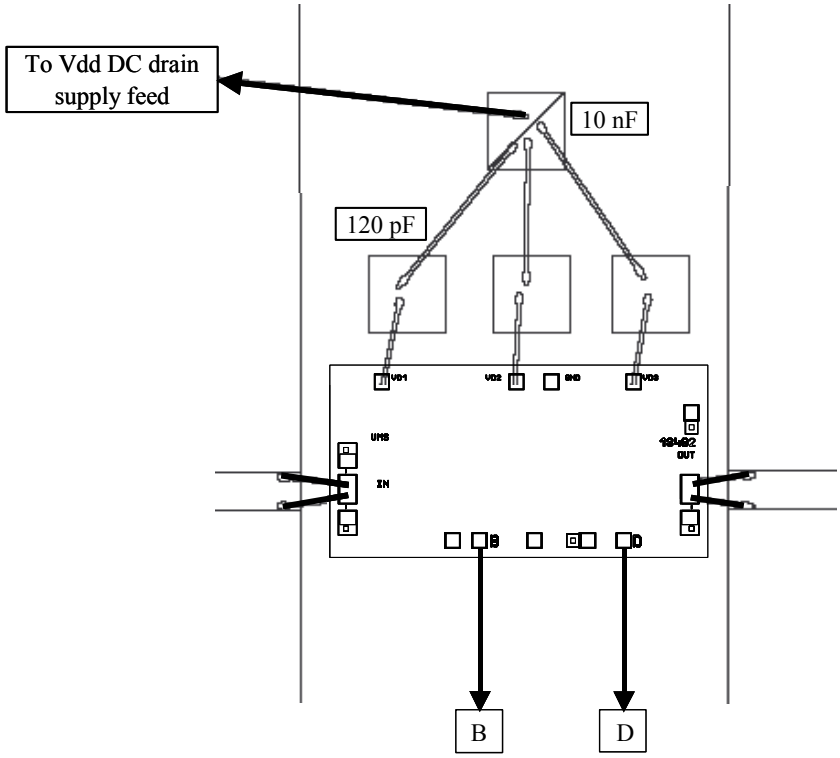
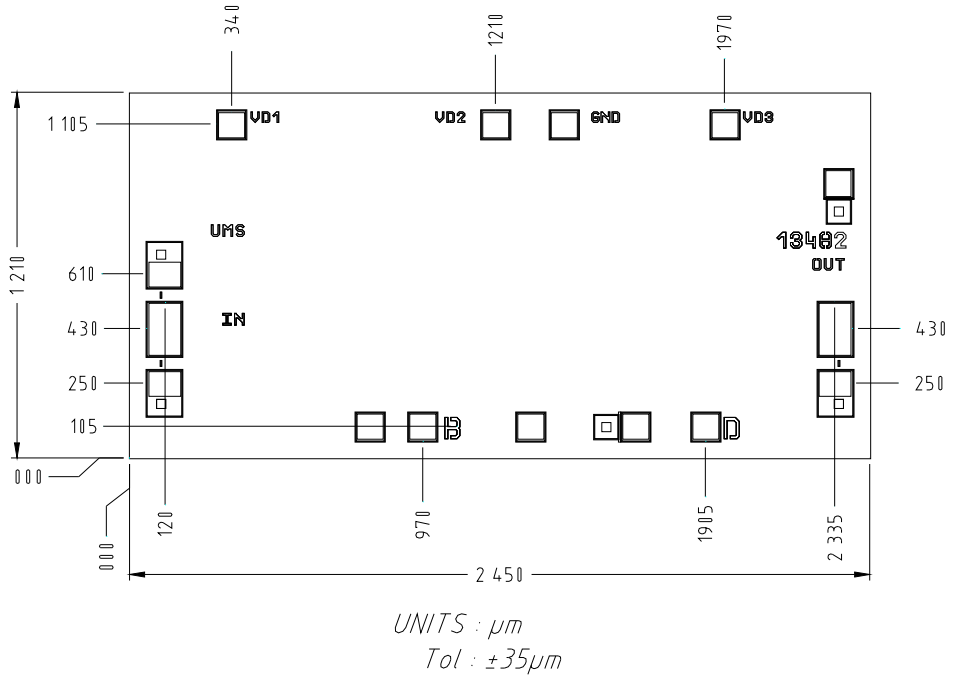
Chip Assembly and Mechanical Data



Note: Supply feed might be capacitively bypassed. 25µm diameter gold wire is to be prefered.



DC Pads Size: 100/100 µm, Chip thickness : 100 µm

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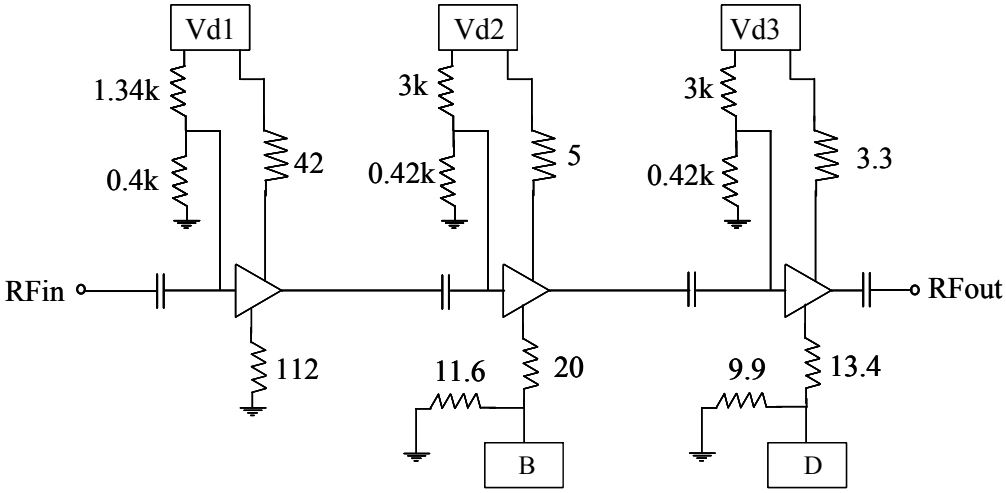
Chip Biasing options

This chip is self-biased, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



The requirement is not to exceed Vds = 3.5Volt (internal Drain to Source voltage).

We propose two standard biasing:

- Low Noise and low consumption: Vd = 4V and B, D not connected (NC).
  Idd = 90mA & Pout-1dB = 14dBm Typical.

- Low Noise and higher output power: Vd = 4V and B, D grounded.
  Idd = 120mA & Pout-1dB = 15dBm Typical.

Ordering Information

Chip form : CHA3689-99F/00

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