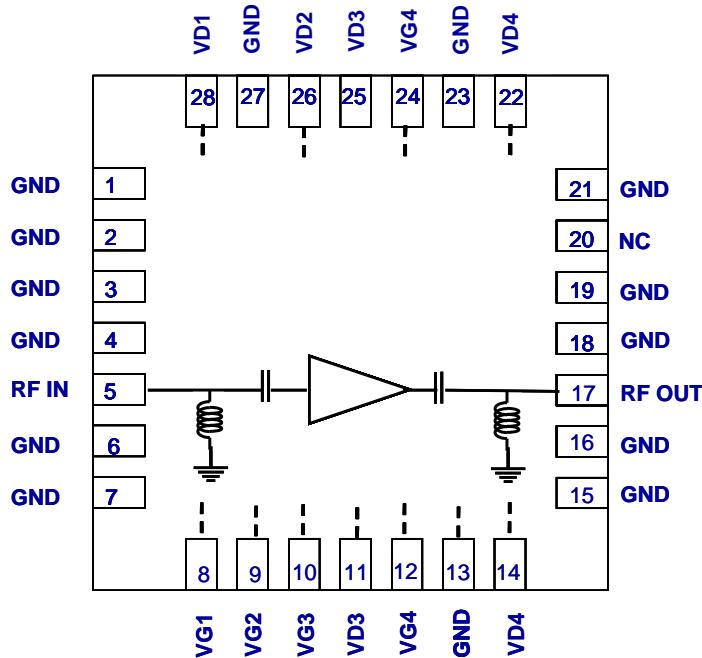


## Advance Information: AI1007

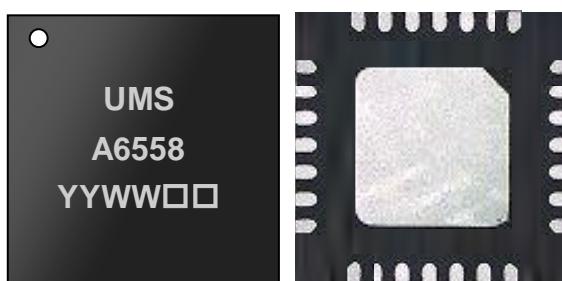
### QFN packaged 29-31.5GHz HPA 2W GaAs Monolithic Microwave IC



UMS is developing a Ka-Band packaged monolithic high power amplifier delivering 32.5dBm output power at 1dB compression point, associated with 22dB of linear gain from 29 to 31.5GHz for an overall power supply of 6V/ 1.9A in saturation.

The circuit is dedicated to telecommunication and VSAT, and also well suited for a wide range of microwave applications and systems.

It is developed on a robust 0.15µm gate length pHEMT process, and will be available in a standard surface mount 28 leads QFN5x5, compliant with the RoHS N° 2011/65 and the regulation REAch N° 1907/2006



## Main Characteristics

Tamb.= +25°C, Vd = +6V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	29.0		31.5	GHz
G	Small signal gain		22		dB
P1dB	Output power @ 1dB compression		32.5		dBm
Psat	Saturated output power		32.7		dBm
Rlin	Input return loss		-10		dB
Id	Supply quiescent drain current		1.4		A
Id_sat	Drain current @ saturation		1.9		A
Vg	Negative gate voltage (8, 9, 10, 12 pads)		-0.55		V

These values are representative of on-board measurements.

## Absolute Maximum Ratings <sup>(1)</sup>

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Cmp	Gain compression level	5	dB
Vd	Drain bias voltage	7	V
Id	Supply quiescent current	1.6	A
Vg	Gate bias voltage	-2 to -0.2	V
Pin	Maximum peak input power overdrive <sup>(2)</sup>	+18	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration &lt; 1s.

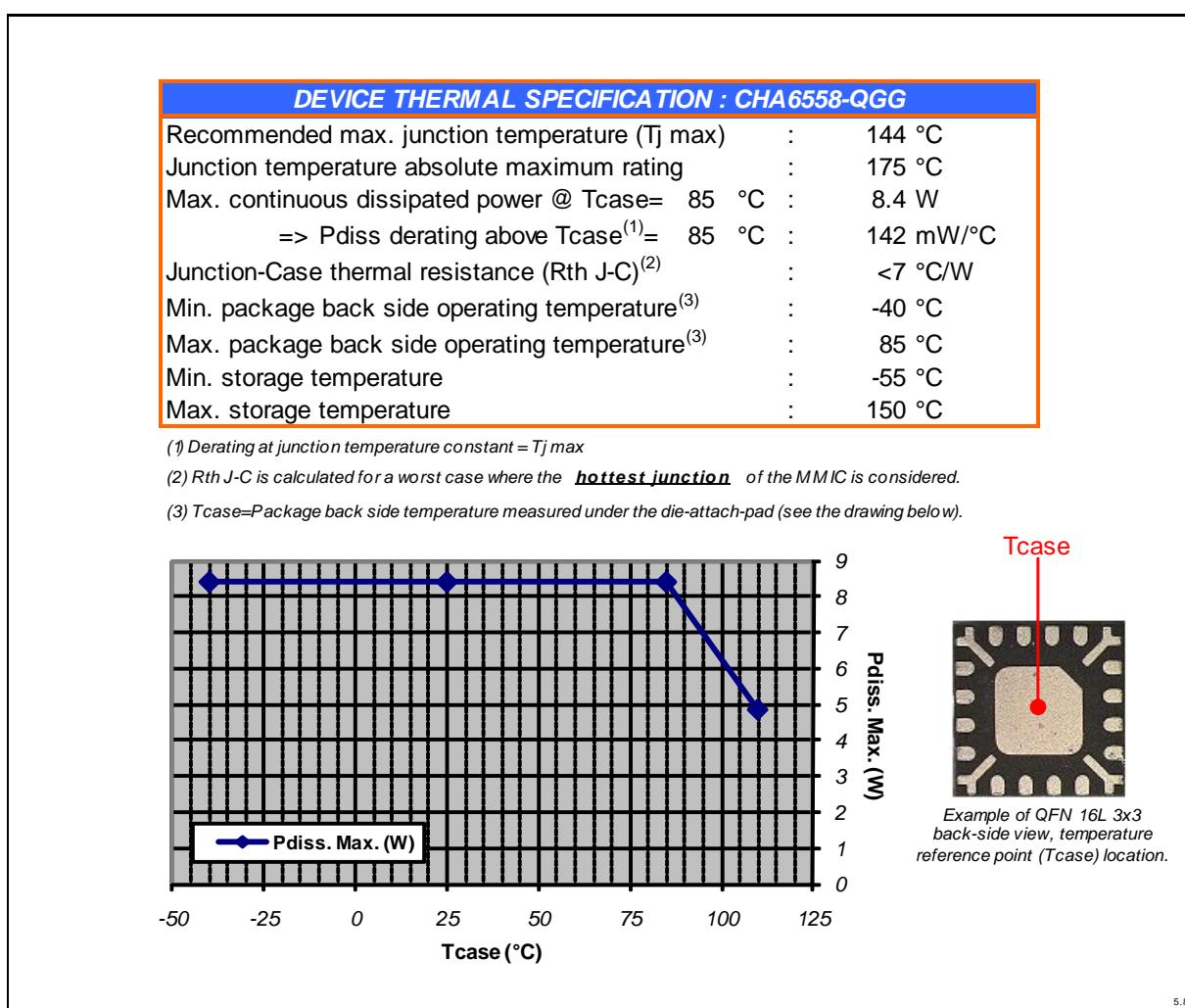
## Advanced Information

## Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package back-side interface ( $T_{case}$ ) as shown below. The system maximum temperature must be adjusted in order to guarantee that  $T_{case}$  remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the  $T_{case}$  temperature can not be maintained below than the maximum temperature specified (see the curve  $P_{diss. Max.}$ ) in order to guarantee the nominal device life time (MTTF).



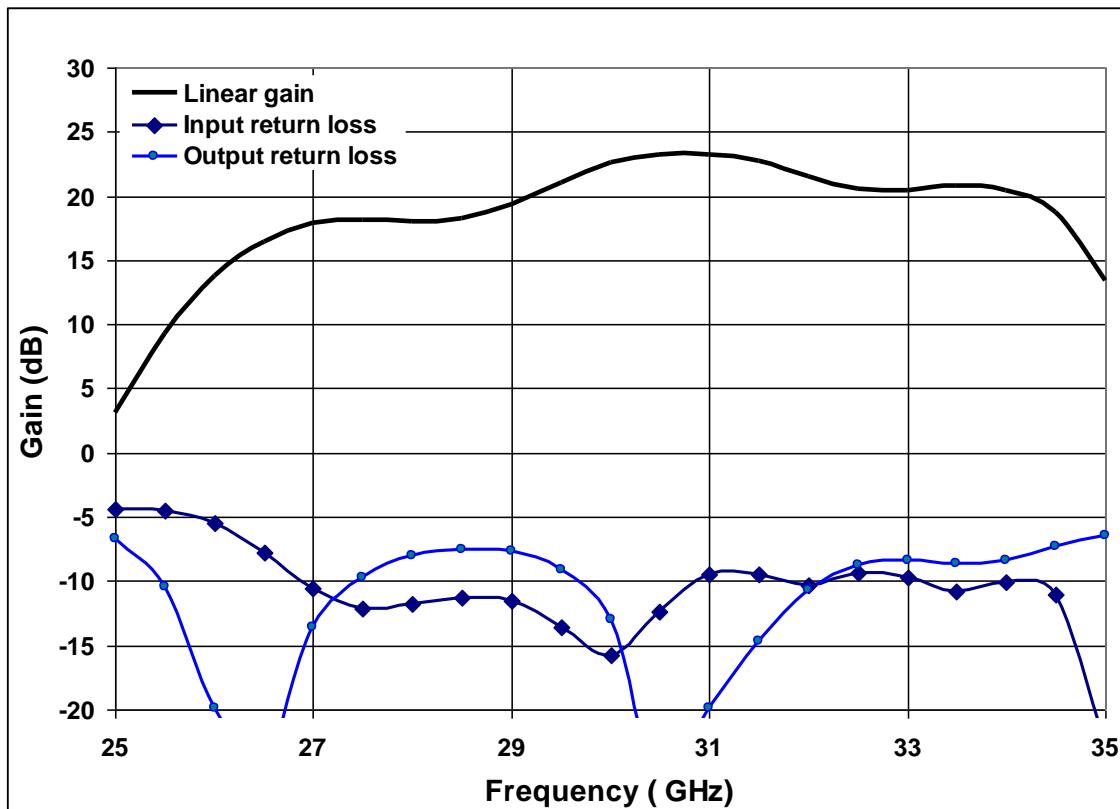
### Advanced Information

## Typical Board Measurements

Tamb.= +25°C, Vd = 6V, Id (Quiescent current) = 1.4A

Measurements in the plan of the connectors, using the proposed land pattern & board, as defined in paragraph "Evaluation mother board".

Linear gain & RLosses versus Frequency



### Advanced Information

Ref. : AI10071293 - 20 Oct 11

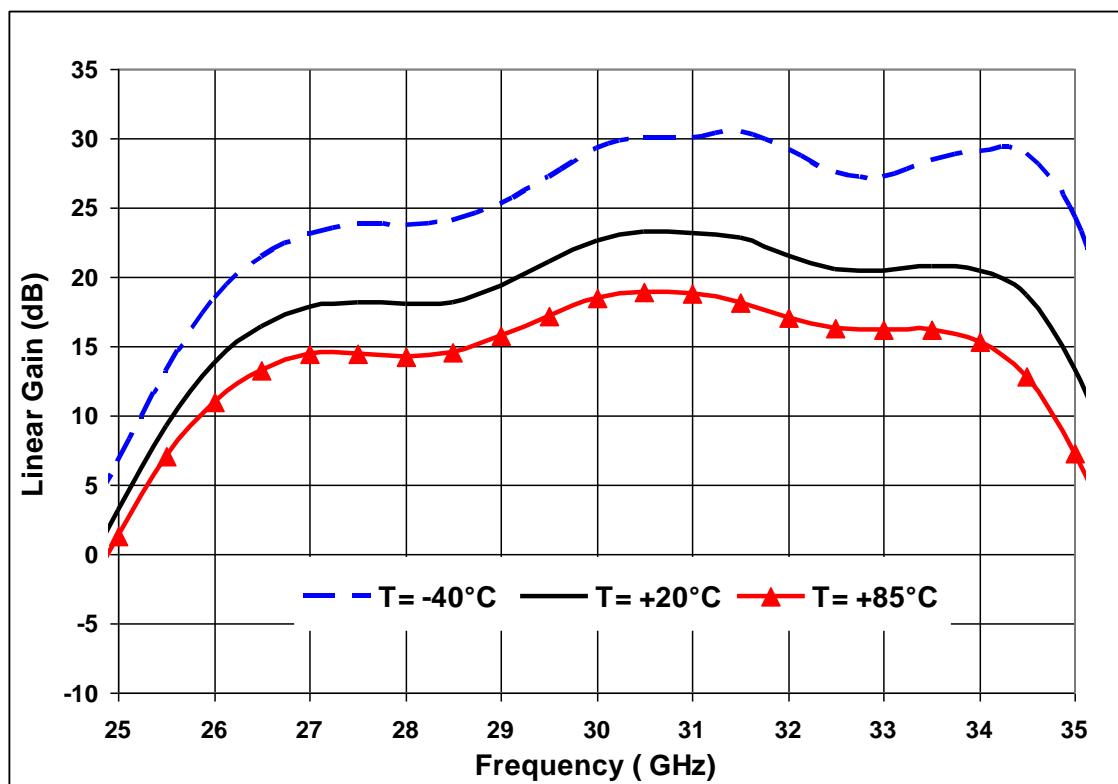
4/12

Subject to change without notice

## Typical Board Measurements

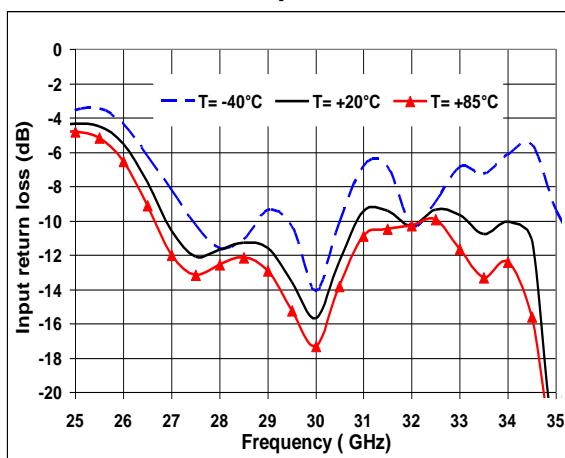
Tamb.= +25°C, Vd = 6V, Id (Quiescent current) = 1.4A

Linear gain versus frequency & temperature

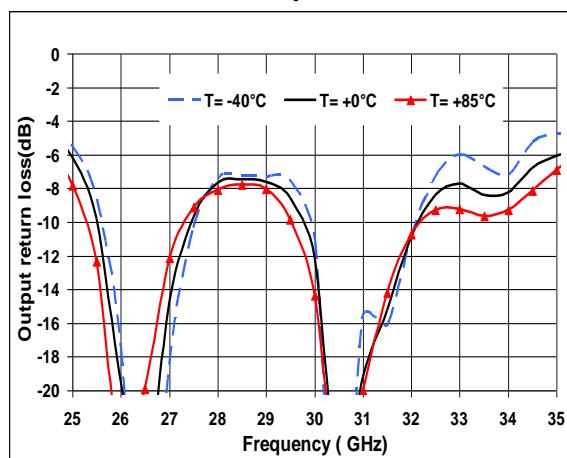


Return Losses versus frequency & temperature

Input



Output



## Advanced Information

Ref. : AI10071293 - 20 Oct 11

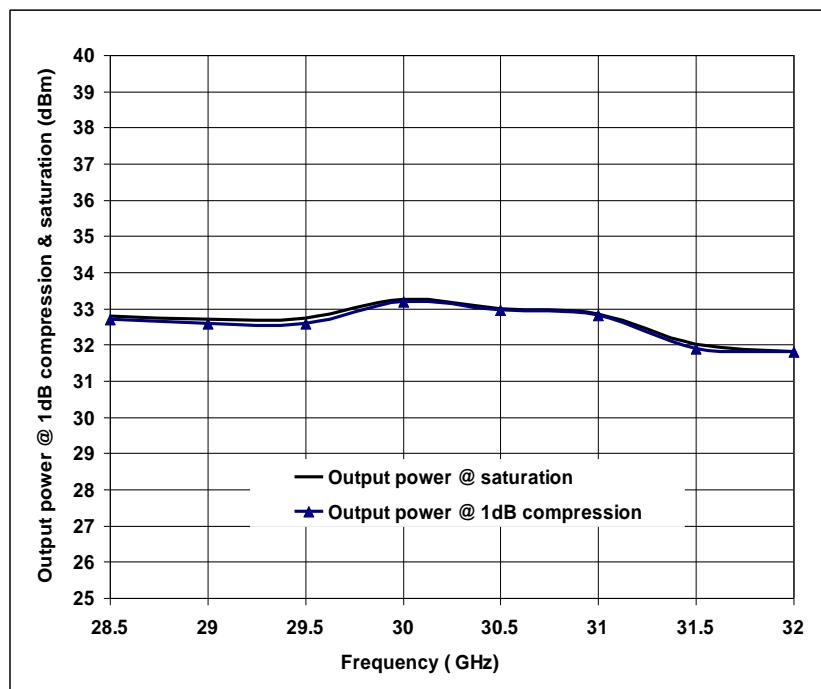
5/12

Subject to change without notice

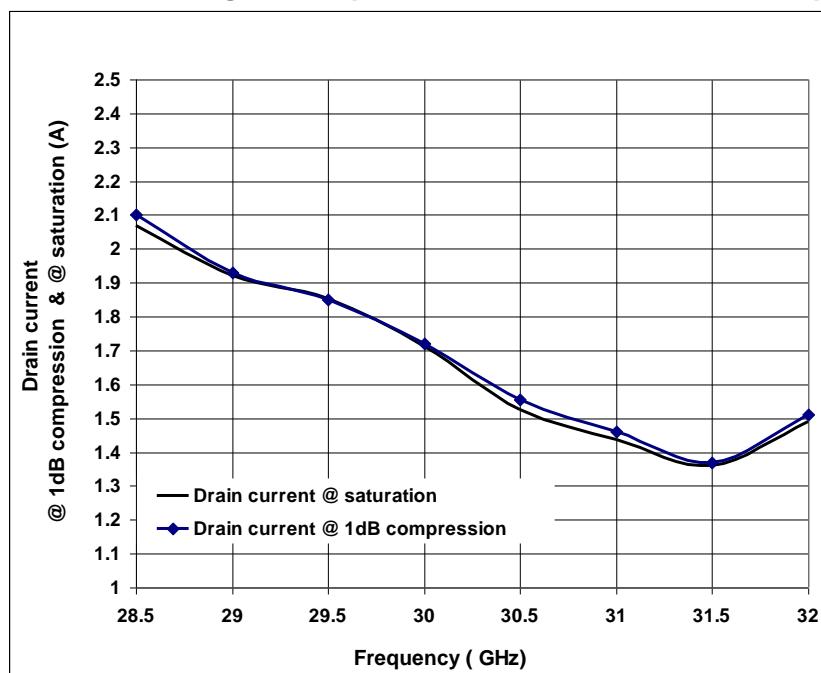
## Typical Board Measurements

Tamb.= +25°C, Vd = 6V, Id (Quiescent current) = 1.4A

**Output Power @1dB gain compression & saturation versus frequency**



**Drain current @1dB gain compression & saturation versus frequency**

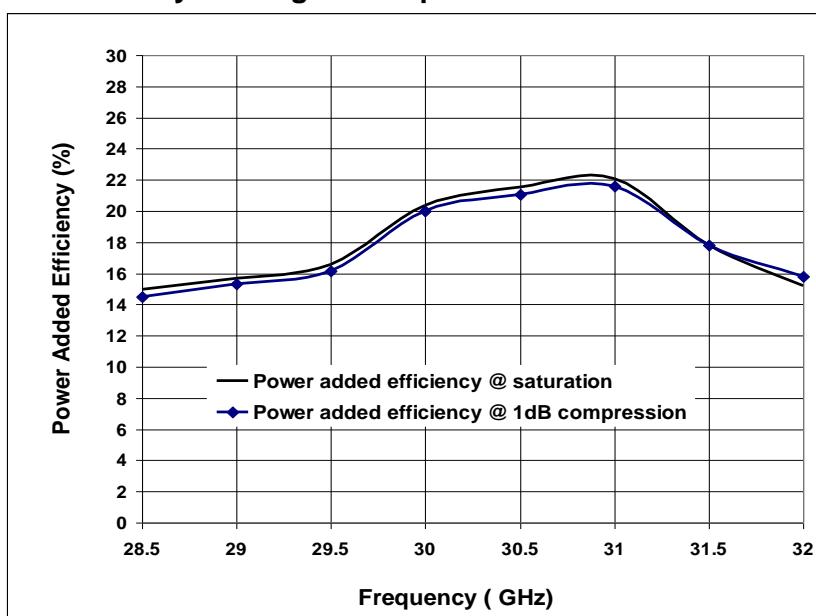


## Advanced Information

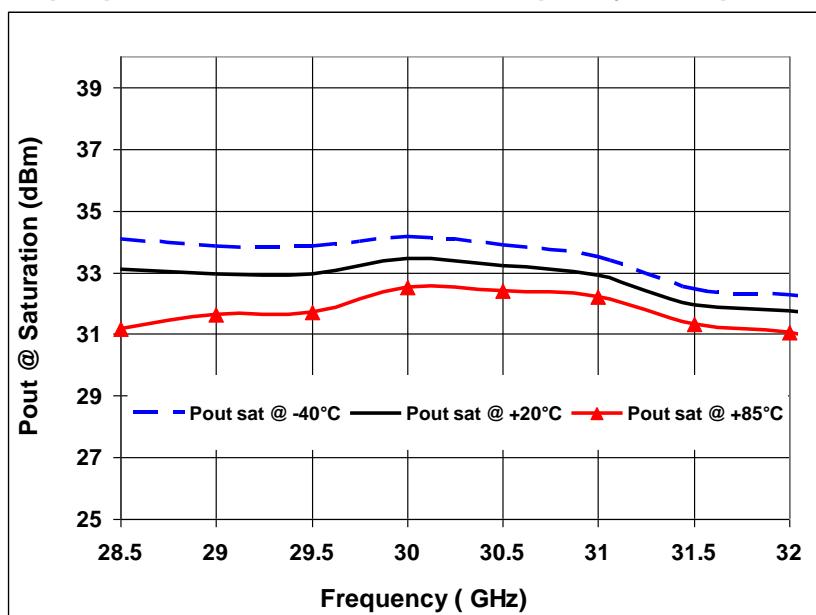
## Typical Board Measurements

Tamb.= +25°C, Vd = 6V, Id (Quiescent current) = 1.4A

**Power added efficiency @1dB gain compression & saturation versus frequency**



**Output power @ saturation versus frequency & temperature**

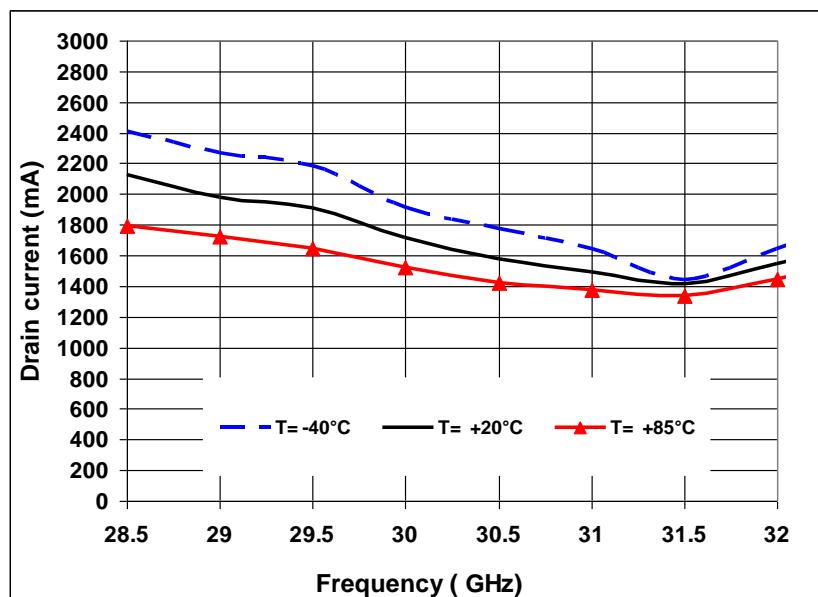


## Advanced Information

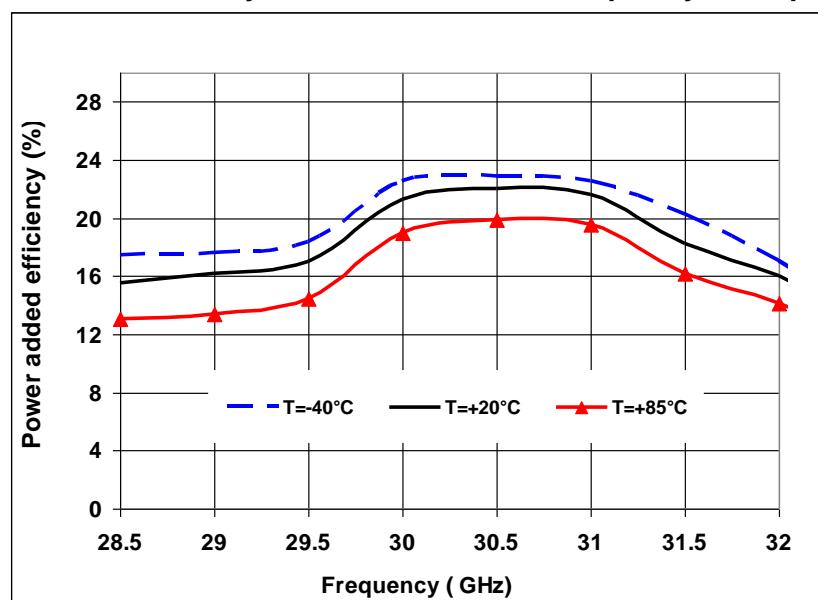
## Typical Board Measurements

Tamb.= +25°C, Vd = 6V, Id (Quiescent current) = 1.4A

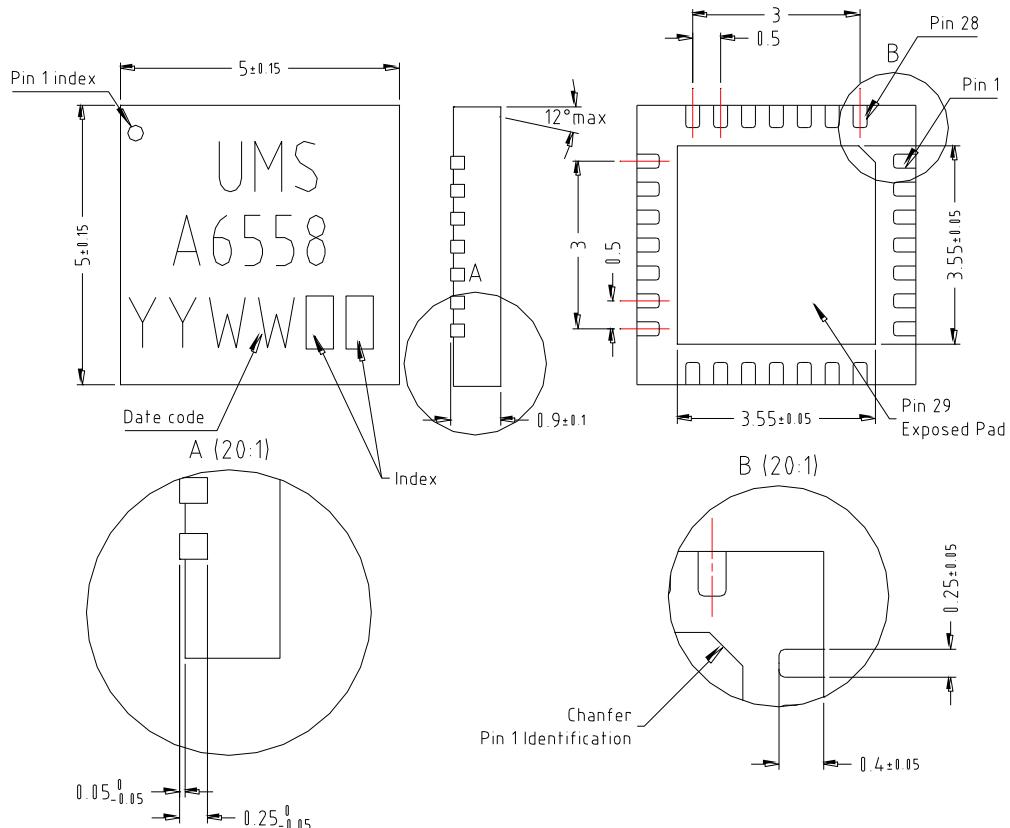
**Drain current @ saturation versus frequency & temperature**



**Power added efficiency @ saturation versus frequency & temperature**



## Package outline <sup>(1)</sup>



Matt tin, Lead Free	(Green)	1-	Gnd <sup>(2)</sup>	11-	VD3	21-	Gnd <sup>(2)</sup>
Units :	mm	2-	Gnd <sup>(2)</sup>	12-	VG4	22-	VD4
From the standard :	JEDEC MO-220 (VGGD)	3-	Gnd <sup>(2)</sup>	13-	Gnd <sup>(2)</sup>	23-	Gnd <sup>(2)</sup>
		4-	Gnd <sup>(2)</sup>	14-	VD4 <sup>(1)</sup>	24-	VG4
29-	GND Exposed pad	5-	RF_in	15-	Gnd <sup>(2)</sup>	25-	VD3
		6-	Gnd <sup>(2)</sup>	16-	Gnd <sup>(2)</sup>	26-	VD2
		7-	Gnd <sup>(2)</sup>	17-	RF_out <sup>(1)</sup>	27-	Gnd <sup>(2)</sup>
		8-	VG1	18-	Gnd <sup>(2)</sup>	28-	VD1
		9-	VG2	19-	Gnd <sup>(2)</sup>		
		10-	VG3	20-	Nc		

<sup>(1)</sup> The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

<sup>(2)</sup> It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

### Advanced Information

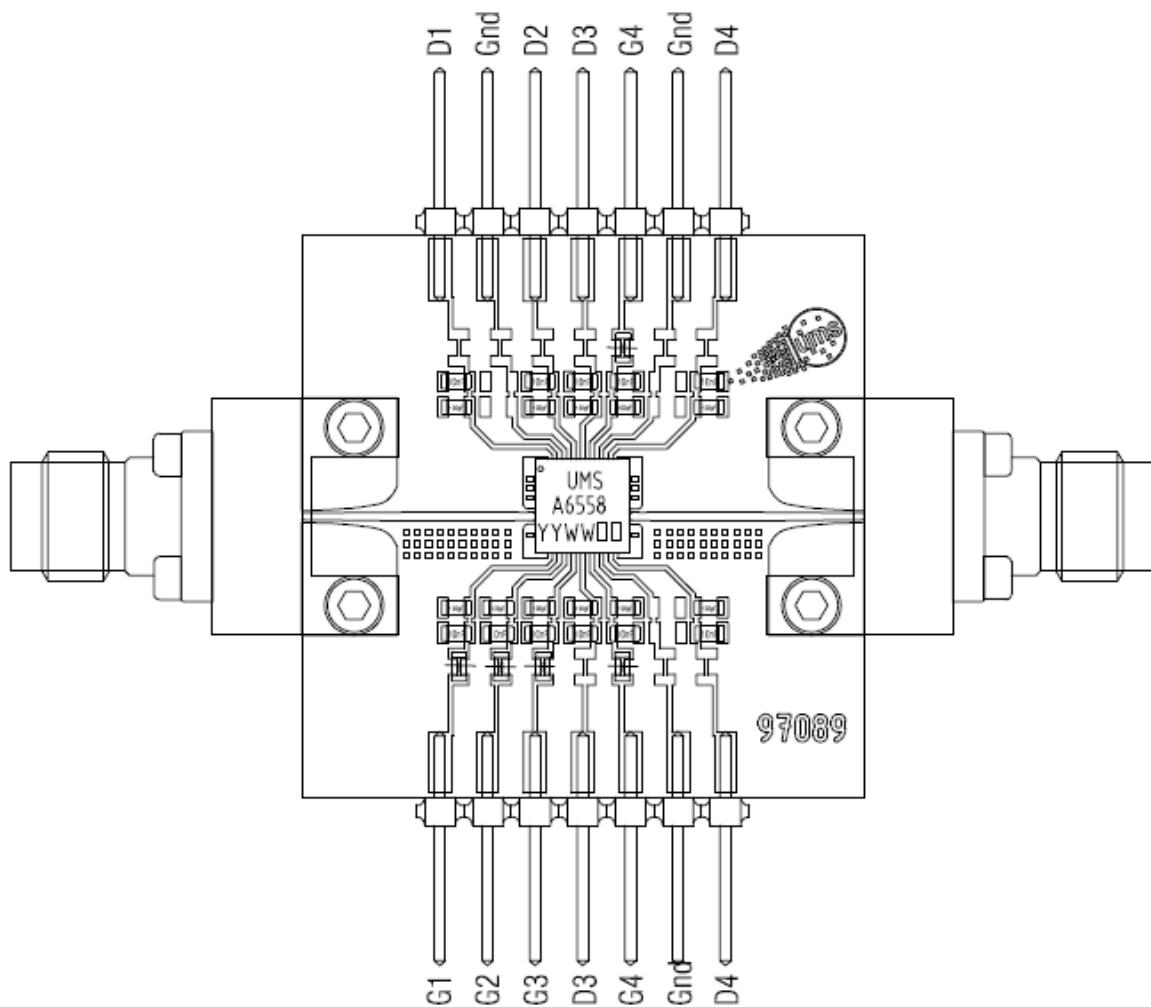
Ref. : AI10071293 - 20 Oct 11

9/12

Subject to change without notice

## Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of  $100\text{pF}\pm5\%$  and  $10\text{nF}\pm10\%$  are necessary for each DC access.



### Advanced Information

Ref. : AI10071293 - 20 Oct 11

10/12

Subject to change without notice

## Notes

### Advanced Information

Ref. : AI10071293 - 20 Oct 11

11/12

Subject to change without notice

Route Départementale 128, B.P.46 - 91401 ORSAY Cedex - FRANCE  
Tel.: +33 (0)1 69 33 03 08 - Fax: +33 (0)1 69 33 03 09

united  
monolithic  
semiconductors



## **Recommended package footprint**

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations and exact package dimensions.

## **SMD mounting procedure**

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at <http://www.ums-gaas.com>.

## **Recommended environmental management**

Refer to the application note AN0019 available at <http://www.ums-gaas.com> for environmental data on UMS package products.

## **Recommended ESD management**

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

## **Sampling request reference**

Die:

Package: ES-CHA6558-QGG

Contact us

Web site: [www.ums-gaas.com](http://www.ums-gaas.com)

e.mail: [mktsales@ums-gaas.com](mailto:mktsales@ums-gaas.com)

Phone: 33 (1) 6933 0226 (France)  
1 978 905 3165 (USA)  
86 21 6103 1703 (China)

### Advanced Information