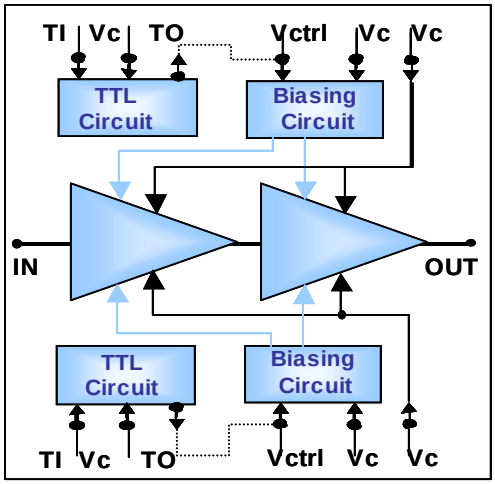
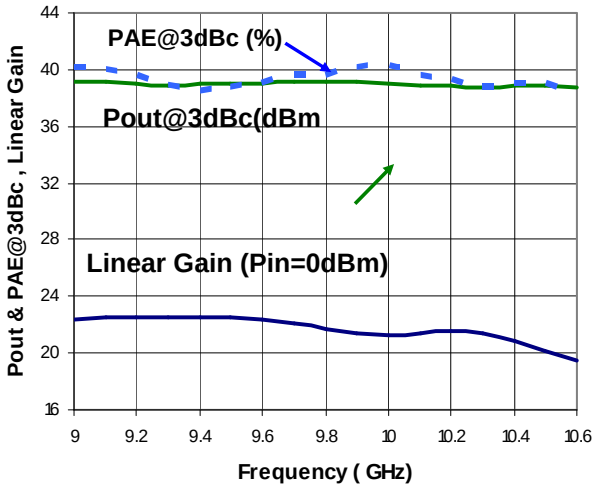
X-band HBT High Power Amplifier

GaAs Monolithic Microwave IC

Description

The **CHA7012** chip is a monolithic two-stage GaAs high power amplifier designed for X band applications.
This device is manufactured using a GaInP HBT process, including, via holes through the substrate and air bridge. A nitride layer protects the transistors and the passive components. Special heat removal techniques are implemented to guarantee high reliability.
To simplify the assembly process:
-the backside of the chip is both RF and DC grounded
-bond pads and back side are gold plated for compatibility with eutectic die attach method and thermosonic or thermo compression bonding process.





Pout & PAE @3dBc and Linear Gain @ 25°C

Main Features

- Frequency band: 9.2 -10.4GHz
- Output power (P3dB): 38.5dBm
- High linear gain: > 20dB
- High PAE: > 38%
- Two biasing modes:
  -VDigital control thanks to TTL interface
  -VAnalog control thanks to biasing circuit
- Chip size: 5.00 x 3.68 x 0.1mm

Main Characteristics

Vc=7.5V, Ic (Quiescent) = 1.9A, Pulse width=100µs, Duty cycle = 20%

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	9.2		10.4	GHz
Psat	Saturated output power @ 25°C		9		W
P_3dBc	Output power @ 3dBc @ 25°C		7		W
G	Small signal gain @ 25°C		20		dB
Top	Operating temperature range	-40		+80	°C

ESD Protections: Electrostatic discharge sensitive device. Observe handling precautions!

United Monolithic Semiconductors S.A.S.
Route Départementale 128 - B.P.46 - 91401 Orsay Cedex France
Tel. : +33 (0)1 69 33 03 08 - Fax : +33 (0)1 69 33 03 09

Electrical Characteristics

Tamb = 20℃, Vc=7.5V, Ic (Quiescent) = 1.9A, Pulse width=100µs, Duty cycle = 20%

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency	9.2		10.4	GHz
G	Small signal gain	17.5	20	23	dB
G_T	Small signal gain variation versus temperature		-0.025		dB/℃
RLin	Input Return Loss	8	10		dB
RLout	Output Return Loss	8	12		dB
Psat	Saturated output power		39.5		dBm
Psat_T	Saturated output power variation versus temperature		-0.01		dB/℃
P_3dBc	Output power @ 3dBc (3)	38	38.5		dBm
PAE_3dBc	Power Added Efficiency @ 3dBc	34	38		%
Vc	Power supply voltage (3)		7.5	8	V
Ic	Power supply quiescent current (1)		1.9		A
TI	TTL input voltage	0		5	V
I_TI	TTL input current		1		mA
Vctrl	Collector control voltage		5		V
Zctr	Vctrl input port impedance (2)		350		Ohm
Top	Operating temperature range	-40		+80	℃

(1) Parameter tunable by Vctrl when control biasing circuit used.
(2) This value corresponds to the 4 ports in parallel (Pin 4, 8, 14, 18)
(3) 0.5V variation on Vc leads to around 0.4dB variation of the output power (impact on robustness see Maximum ratings)

Absolute Maximum Ratings (1)

Tamb = 20℃

Symbol	Parameter	Values	Unit
Cmp	Compression level (2)	6	dBc
Vc	Power supply voltage with RF	8	V
Ic	Power supply quiescent current	2.8	A
Ic_sat	Power supply current in saturation	3.5	A
Vctrl	Collector current control voltage	6.5	V
Tj	Maximum junction temperature	175	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) For higher compression the level limit can be increased by decreasing the voltage Vc using the rate 0.5 V / dBc
Equivalent Thermal resistance to Backside: 6℃/W

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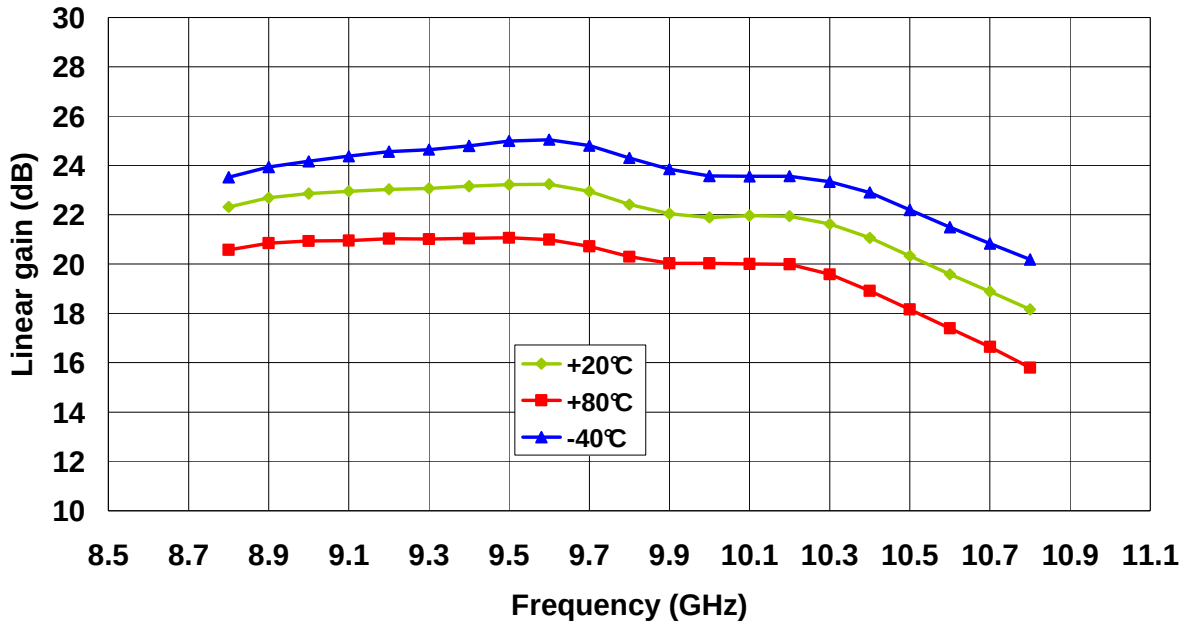
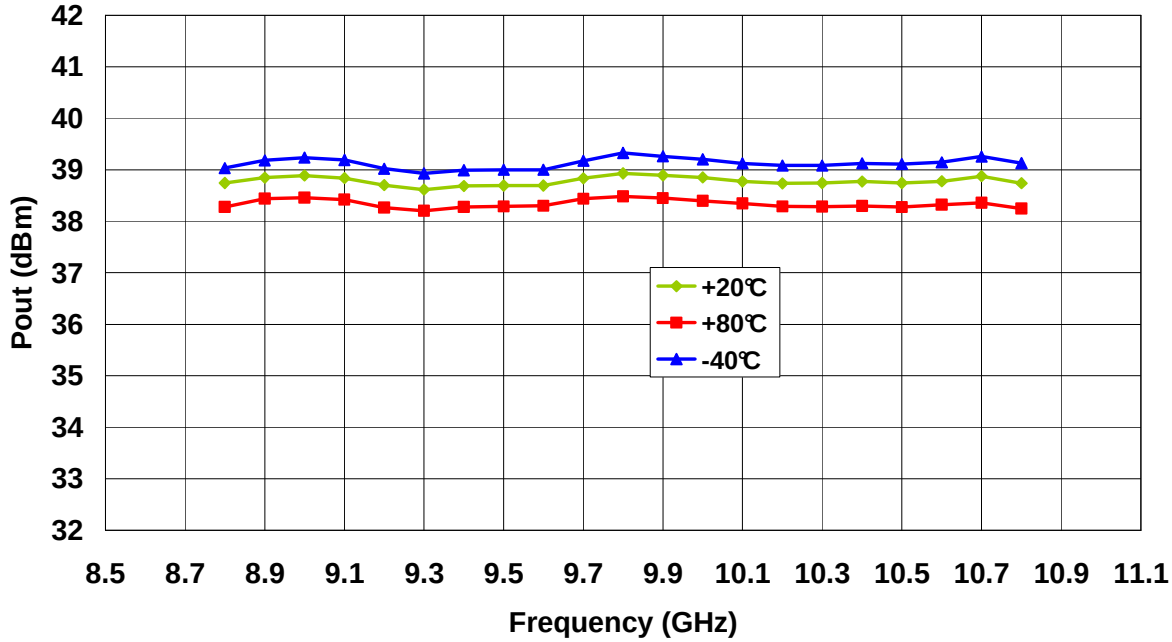
Typical measured characteristics

Measurements on Jig

Vc=7.5V, VTTL=5V, Ic (Quiescent) = 1.9A, Pulse width=100µs, Duty cycle = 20%



Linear gain versus frequency and temperature



Output Power @ 3dBc versus frequency and temperature

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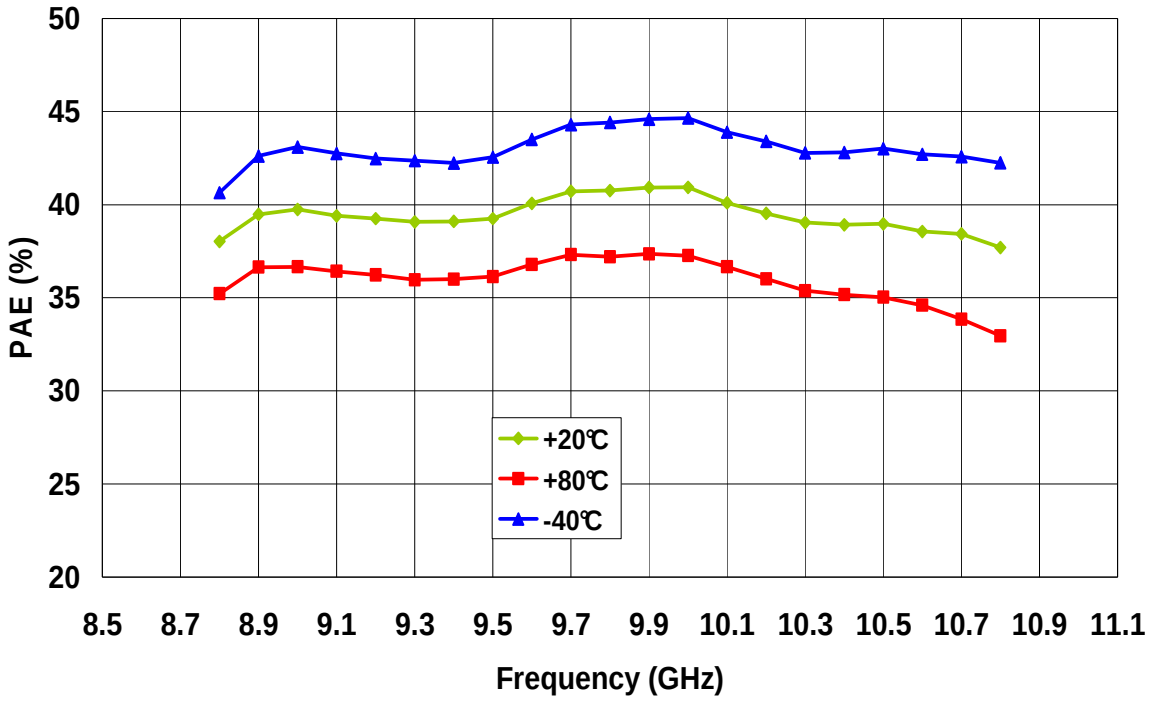
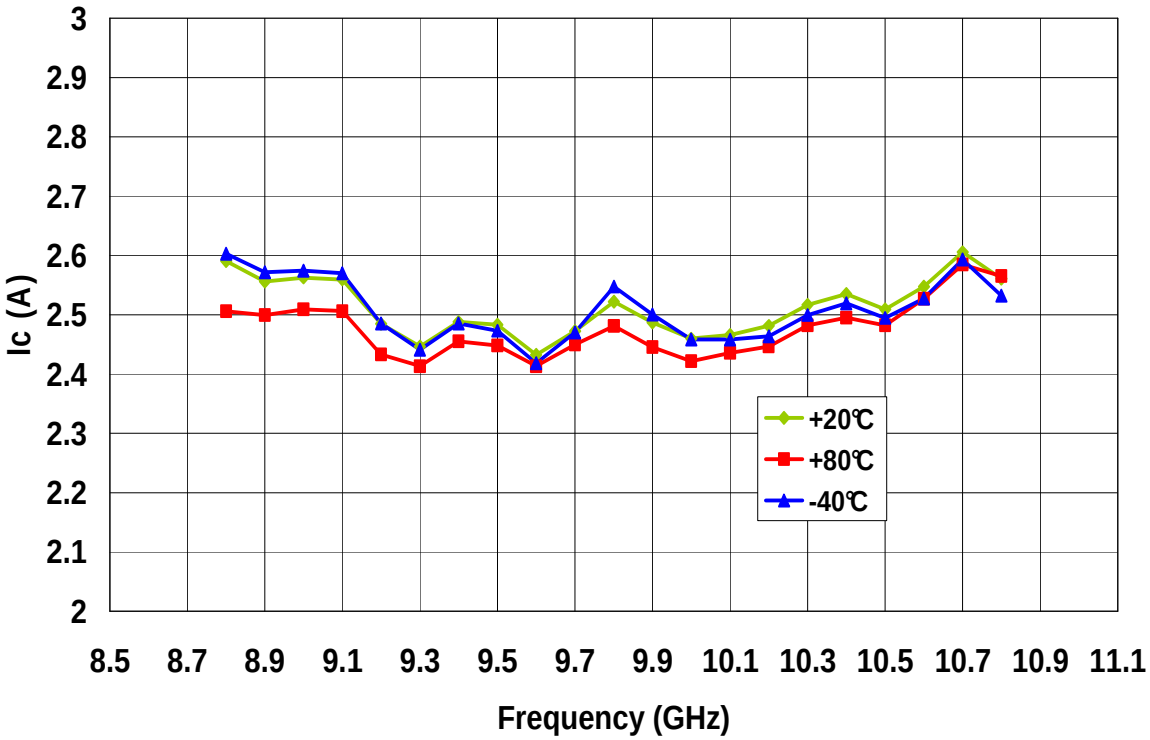


PAE @ 3dBc versus frequency and temperature



Ic @ 3dBc versus frequency and temperature

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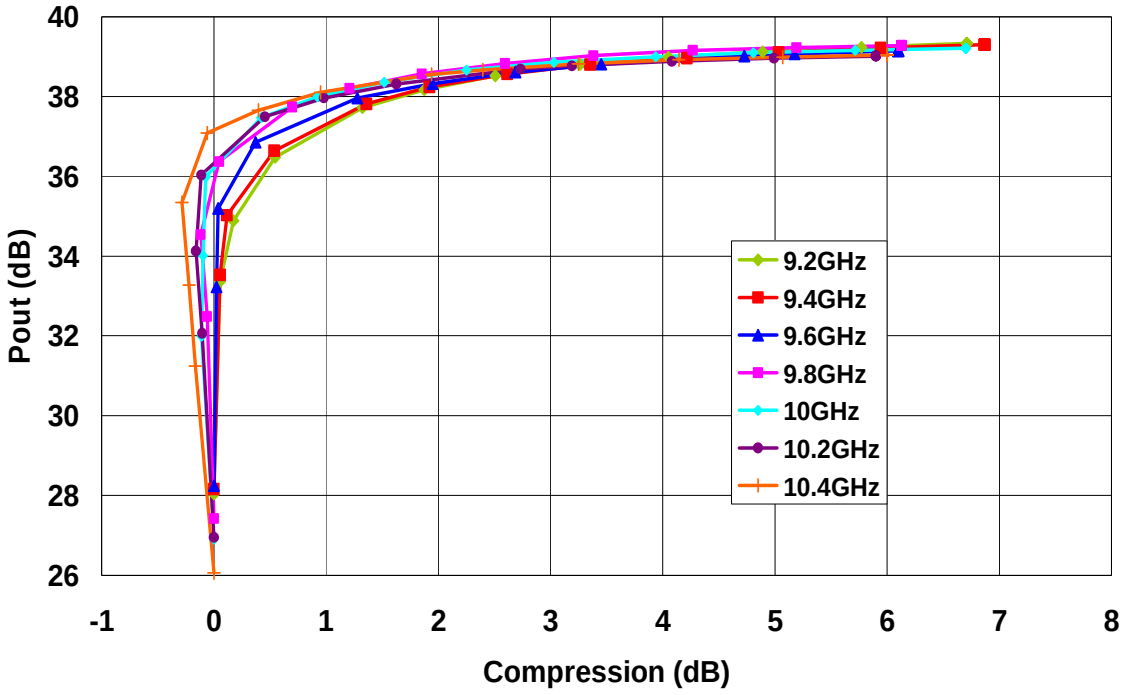
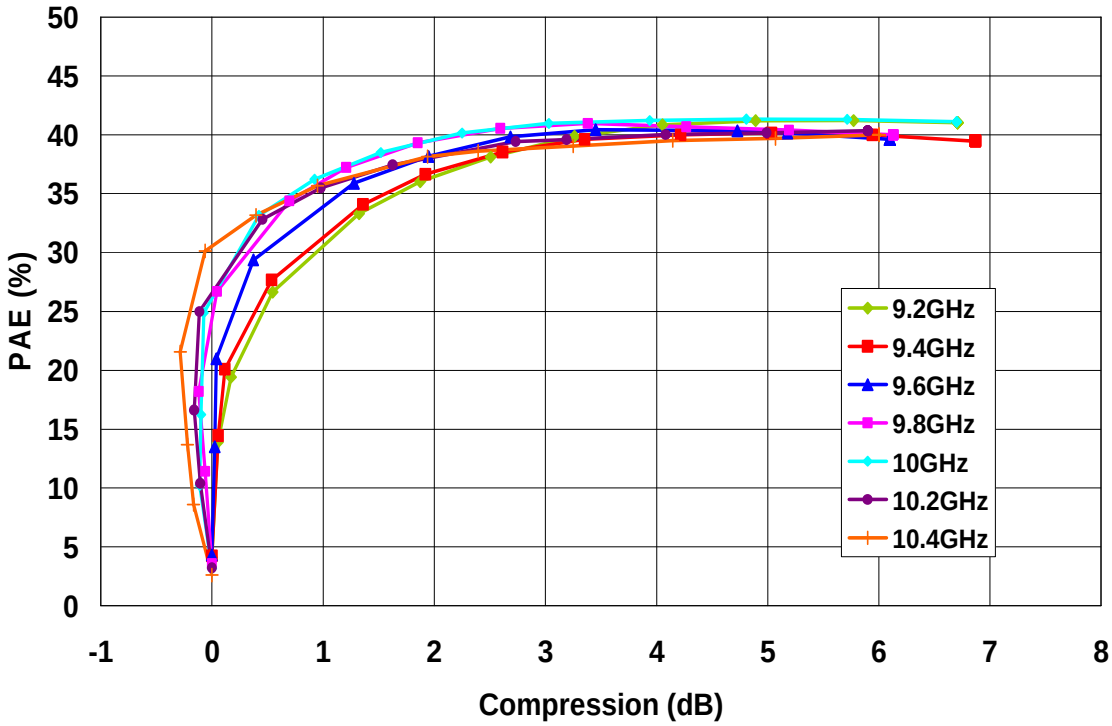


Output Power @ 25℃ versus compression and frequenc y



PAE @ 25℃ versus compression and frequency

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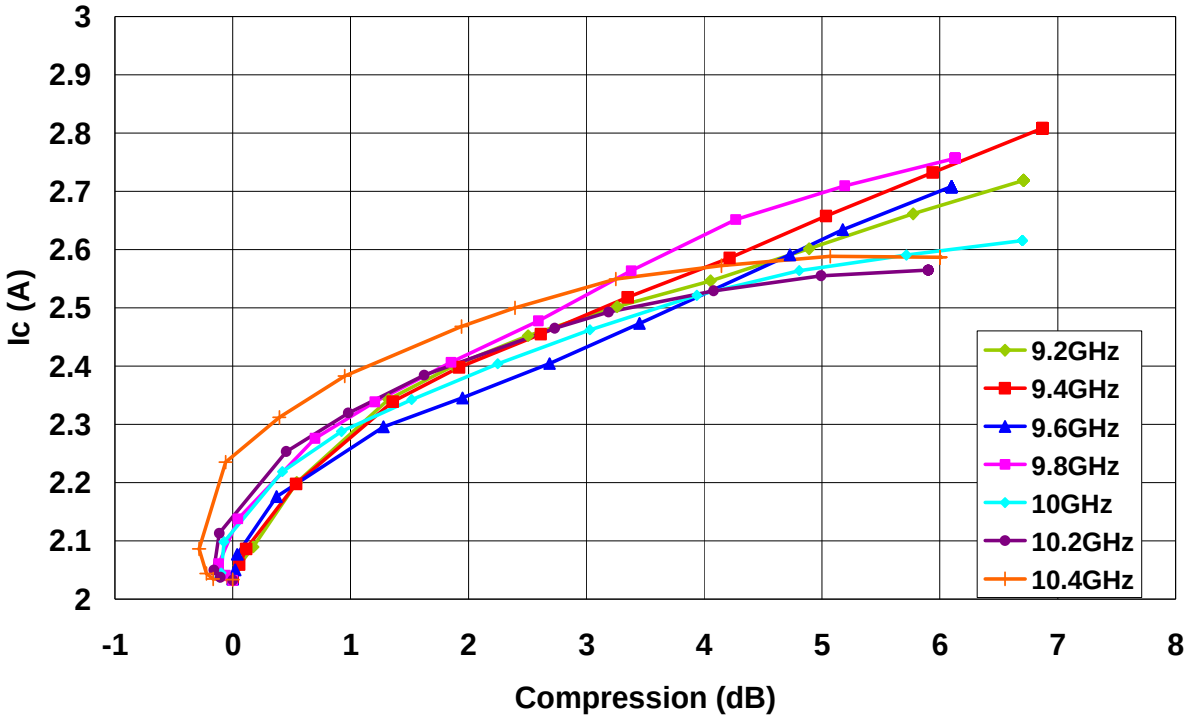
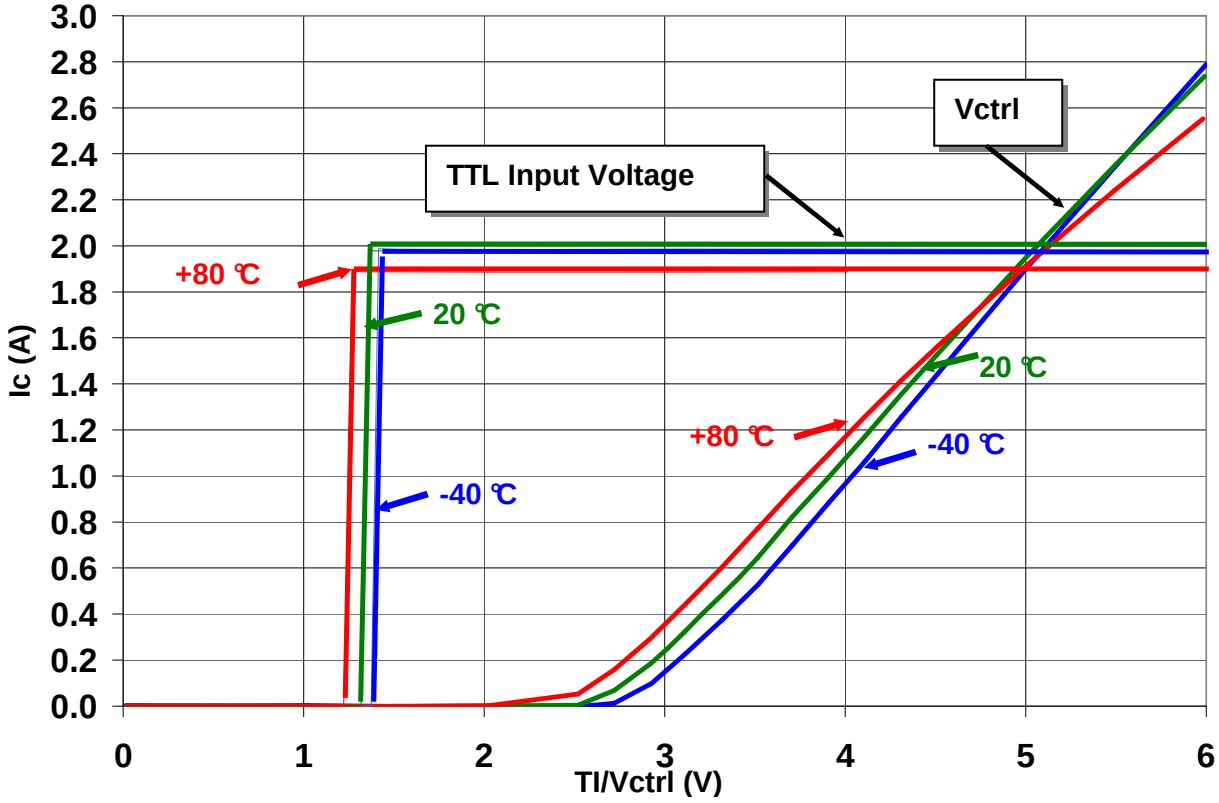


Collector current @ 25℃ versus compression and fr equency

Temperatures: -40℃; 20℃; +80℃ Vc=7.5V Pul se= 100µs, Duty cycle 20%



Collector quiescent current versus Tl & Vctrl and temperature

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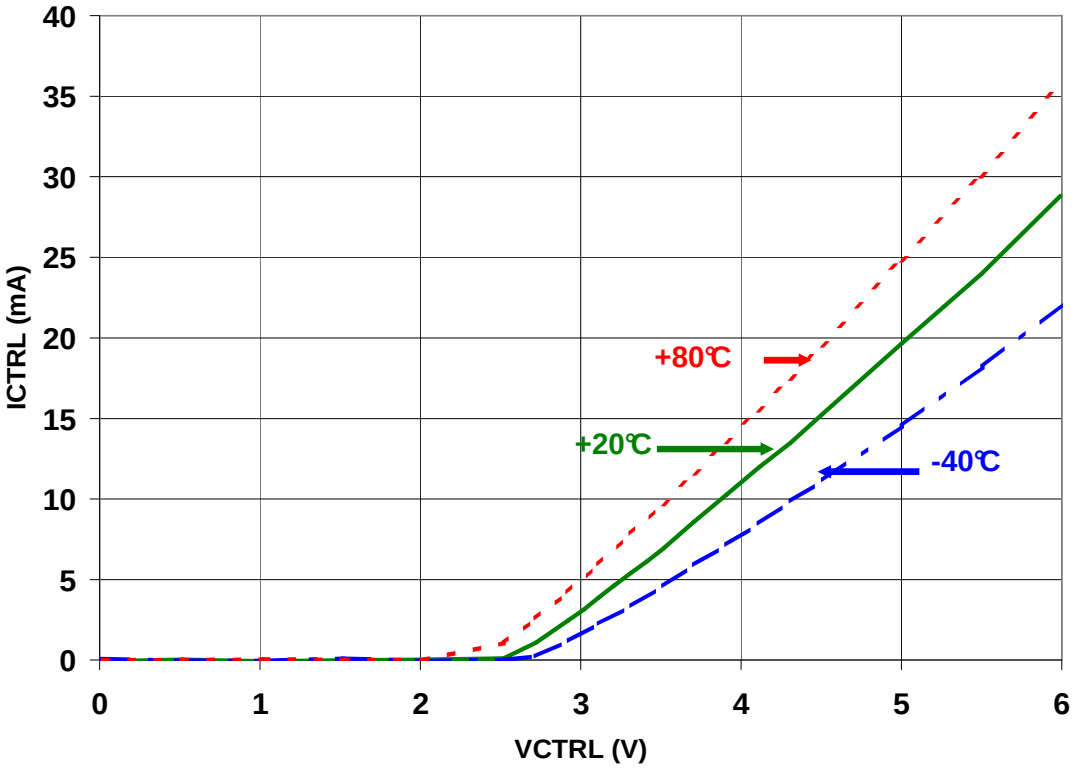
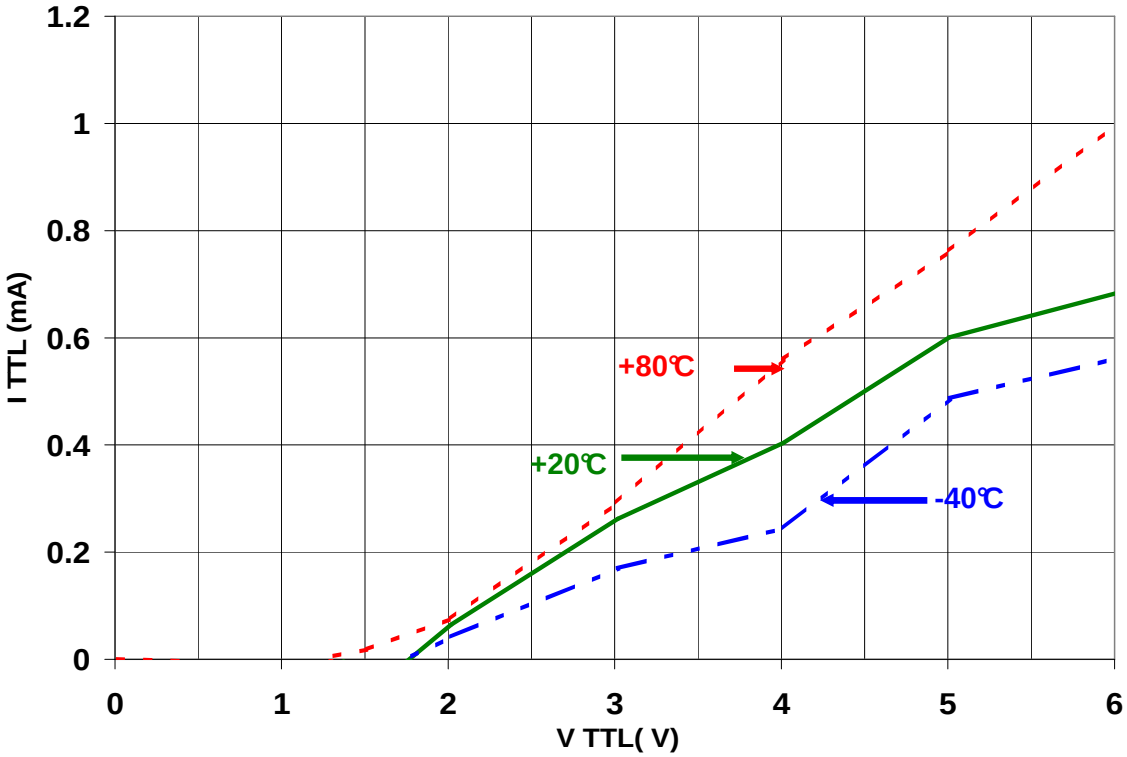
Temperatures: -40℃; 20℃;+80℃ Vc=7.5V Pulse= 100µs, Duty cycle 20%



Collector current control versus control voltage and temperature

Temperatures: -40℃; 20℃; +80℃ Vc=7.5V Pulse= 100µs, Duty cycle20%



TTL input current versus TTL voltage and temperature

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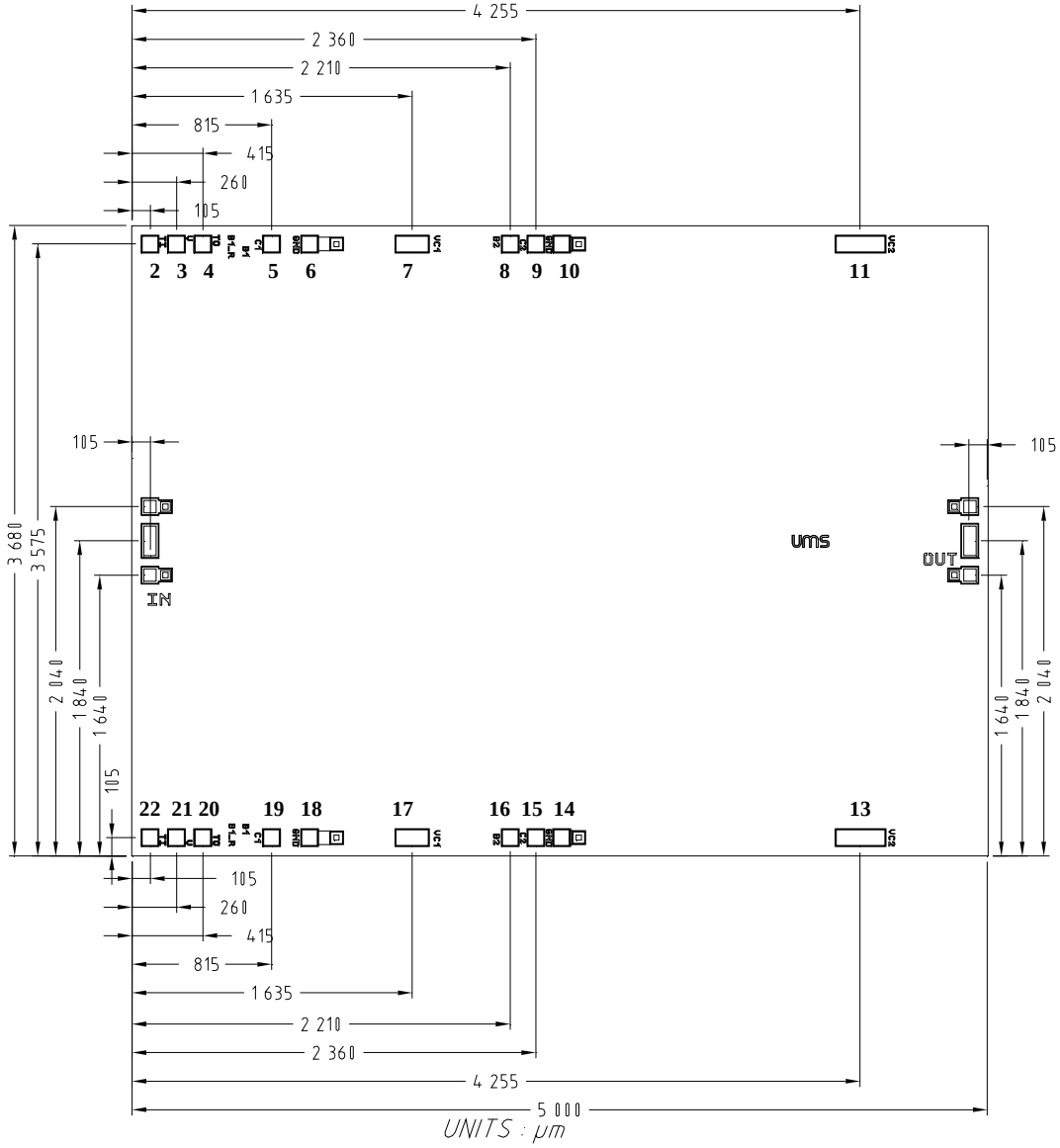
Chip Mechanical Data and Pin references



Chip thickness = 100µm +/- 10 µm
RF pads (1, 12) = 96 x 196µm²
DC pads (2, 3, 4, 5, 9,15, 19, 20, 21, 22) = 96 x 96µm²
DC pads (7, 17) = 192 x 96µm²
DC pads (11, 13) = 288 x 96µm²

Pin number	Pin name	Description
1	IN	Input RF
8, 16		NC
5, 9, 15, 19	Vctrl	Collector current control voltage
2, 22	TI	TTL input
4, 20	TO	TTL output
6, 10, 14, 18	GND	Ground (NC)
3, 7, 11, 13, 17, 21	V,Vc1,Vc2	Power supply voltage
12	OUT	Output RF

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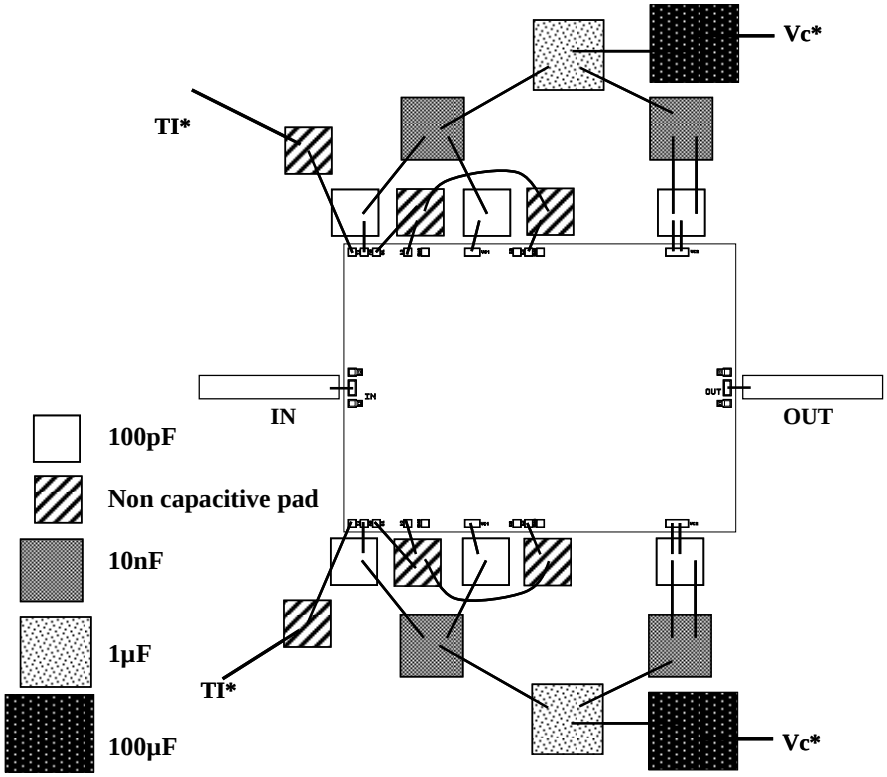
Bonding recommendations

For thermal and electrical considerations, the chip should be brazed on a metal base plate.
The RF, DC and modulation port inter-connections should be done according to the following table:

Port	Connection
IN (1)	Inductance (Lbonding) = 0.3nH 400µm length with wire diameter of 25 µm
OUT (12)	Inductance (Lbonding) = 0.3nH 400µm length with wire diameter of 25 µm
DC pads to 1st decoupling level for double bonding	Inductance (Lbonding) =0.7nH Two 1.2mm length wires with a diameter of 25 µm
DC pads to 1st decoupling level for single bonding	Inductance (Lbonding) =1nH One 1.2mm length wires with a diameter of 25 µm
1st decoupling level to 2nd decoupling level for double bonding	Inductance (Lbonding) =0.7nH Two 1.2mm length wires with a diameter of 25 µm
1st decoupling level to 2nd decoupling level for single bonding	Inductance (Lbonding) =1nH One 1.2mm length wires with a diameter of 25 µm

Assembly recommendations in test fixture (using TTL circuits)



* Performances obtained with the same accesses connected to the same supply
Note: Supply feed should be capacitively by-passed. 25µm diameter gold wire is to be preferred.

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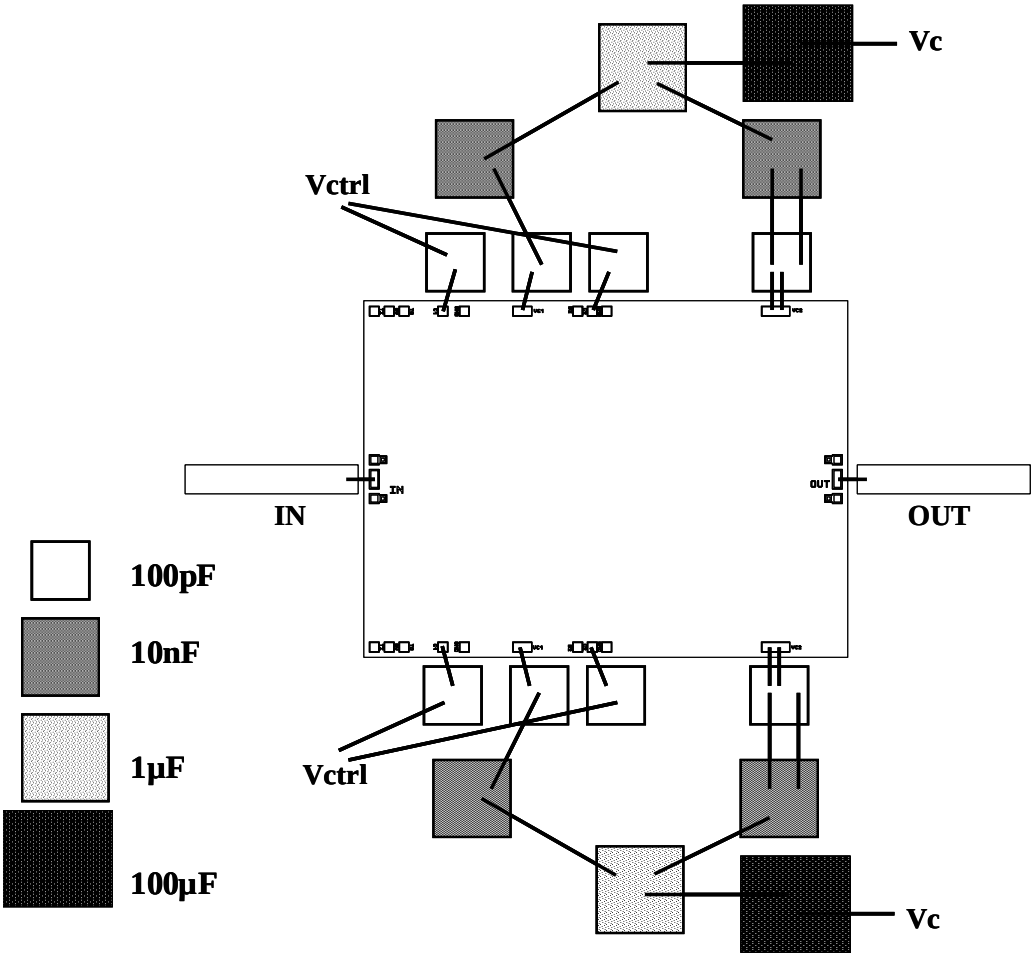
Assembly recommendations in test fixture
(using analog biasing circuits)



Note: Supply feed should be capacitively by-passed. 25µm diameter gold wire is to be preferred.

Ordering Information

Chip form : CHA7012-99F/00

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