SC1894: 225 to 3800 MHz RF Power Amplifier Linearizer (RFPAL)

General Description

The SC1894 is Scintera's 3rd generation of RF PA linearizers (RFPAL) providing improved correction and functionality over the previous generations. The SC1894 is a fully-adaptive, RFin / RFout predistortion linearization solution optimized for a wide range of amplifiers, power levels and communication protocols. The SC1894 uses the PA output and input signals to adaptively generate an optimized correction function in order to minimize the PA's self-generated distortion and impairments. Using RF-domain analog signal processing enables the SC1894 to operate over wide signal bandwidths and consume very low power.

The SC1894 goes beyond linearization and provides Advanced Features (AF) including PA control, monitor and measurement functionality. It integrates 4 general purpose analog inputs and 4 analog/digital outputs that may be configured for PA monitoring, gate bias control and temperature monitoring. It also provides accurate RF power measurement of RFIN and RFFB. Advanced features including spectral monitoring and ACLR alarm are also available. These optional features are accessed through the SC1894's serial peripheral interface (SPI) bus.

Applications

- Cellular infrastructure
  - Single/multi-carrier, multi-standard: CDMA/EVDO, TD-SCDMA, WiMAX, WCDMA/HSDPA, LTE & TD-LTE
  - BTS amplifiers, RRH, booster amplifiers, repeaters, small cells, microcells, picocells, DAS, AAS and MIMO systems
- Microwave Backhaul
  - BPSK, QPSK, up to 1024-QAM
  - IF-to-RF Outdoor Unit (ODU)
- Broadcast Infrastructure
  - UHF digital broadcast
  - DVB-T/H/T2, CMMB, ISDB-T and ATSC
  - Digital terrestrial UHF amplifiers, exciters, drivers and transmitters
- Other applications
  - Public safety and TV white space
  - Any application requiring PA linearization
- Wide range of PAs and output power
  - Amplifier: Class A/AB and Doherty
  - Average PA output power examples:
    - Cellular Infrastructure: Up to 49 dBm
    - Terrestrial Broadcast: Up to 60dBm
  - PA Process: LDMOS, GaN, GaAs and InGaP

Features

SC1894 (PC = 00): RFPAL

- RFin/RFout PA linearizer SoC in standard CMOS
  - Fully Adaptive Correction
  - Up to 28dB ACLR & 38dB IMD improvement(1)
- External reference clock support(3):
  - 10, 13, 15.36, 19.2, 20, 26 and 30.72 MHz
- Low Power Consumption:
  - Duty cycled (9 %) feedback: 600 mW
  - Full adaptation: 1200 mW
- Frequency Range: 225 MHz - 3800 MHz
- Input Signal Bandwidth: 1.2 MHz to 75 MHz
- Packaged in 9x9 mm QFN package
- Operating Case Temperature: -40 °C to +100 °C
- Fully RoHS compliant, Green Materials
- Backwards compatible with SC1887/69/89

SC1894 (PC = 13): RFPAL + AF (optional)(2),(3)

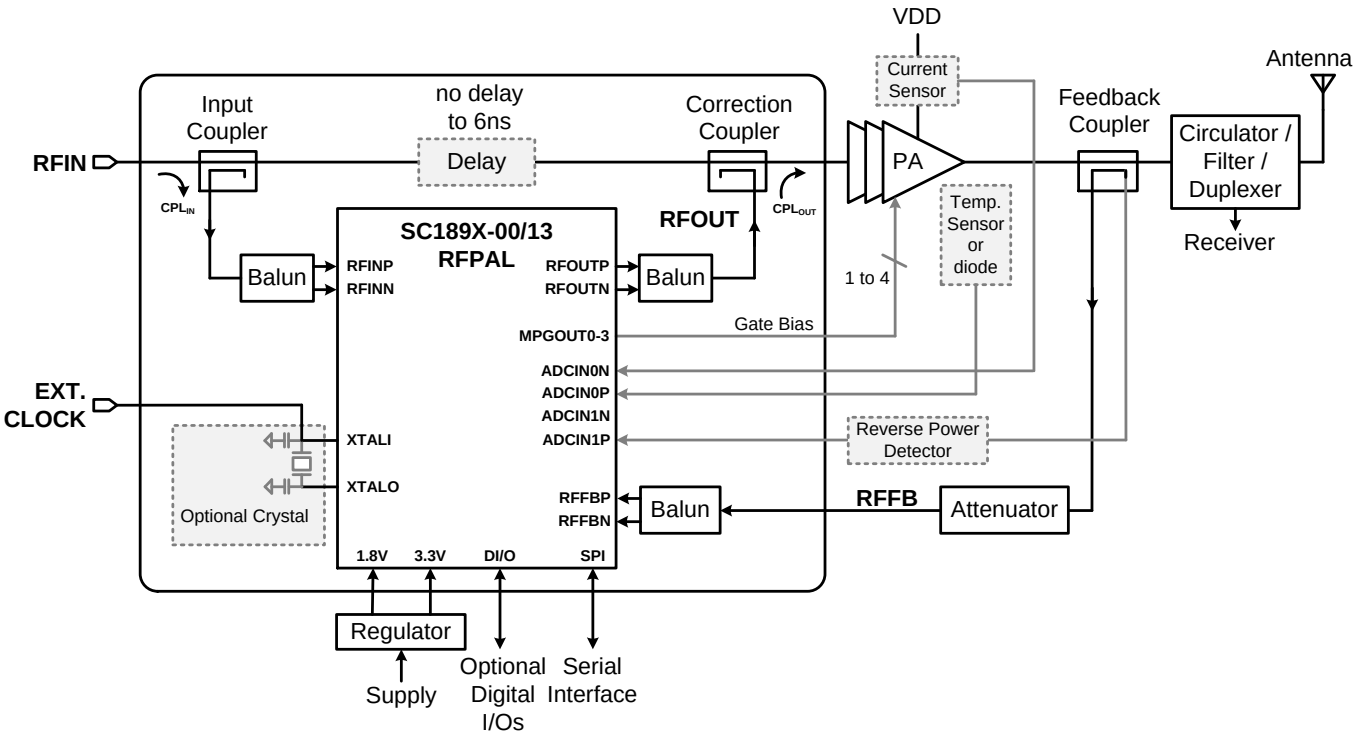
- RFPAL + **A**dvanced **F**eatures
- Dual-RF power measurement
- Internal die temperature monitoring
- PA gain monitoring
- SEM measurement and alarm
- PSD reporting
- PA gain alarm
- Quad ADC, Quad DAC/digital outputs:
  - External temperature monitoring
  - Measure drain current or reverse power
- Quad DAC / Digital Output: PA gate biasing

(1) Performance dependent on amplifier, bias & waveform
(2) Refer to SC1894-Advanced-Features13_Datasheet for specifications.
(3) Prototype Samples available now. Production available Q4'2013.

Benefits

- Ease of use
  - Integrated RFin/RFout solution
  - No FW development required
  - No training, lookup tables or complex calibration required
- Reduces system power consumption & OPEX
- Reduces BOM costs, area and total volume
  - Smaller power supply, heat sink & enclosure
  - Eliminates external bias chips, microcontroller and power detectors
  - Small implementation size (< 6.5 cm^2)
- Field-proven, carrier class reliability

Application Block Diagram



Lines and blocks shaded in grey refer to optional feature bundles, PC = 13. Use of the power measurement unit (RFIN and RFFB) in PC = 13 requires no changes to the application circuit and shares the same design as the baseline RFPAL design, PC = 00.

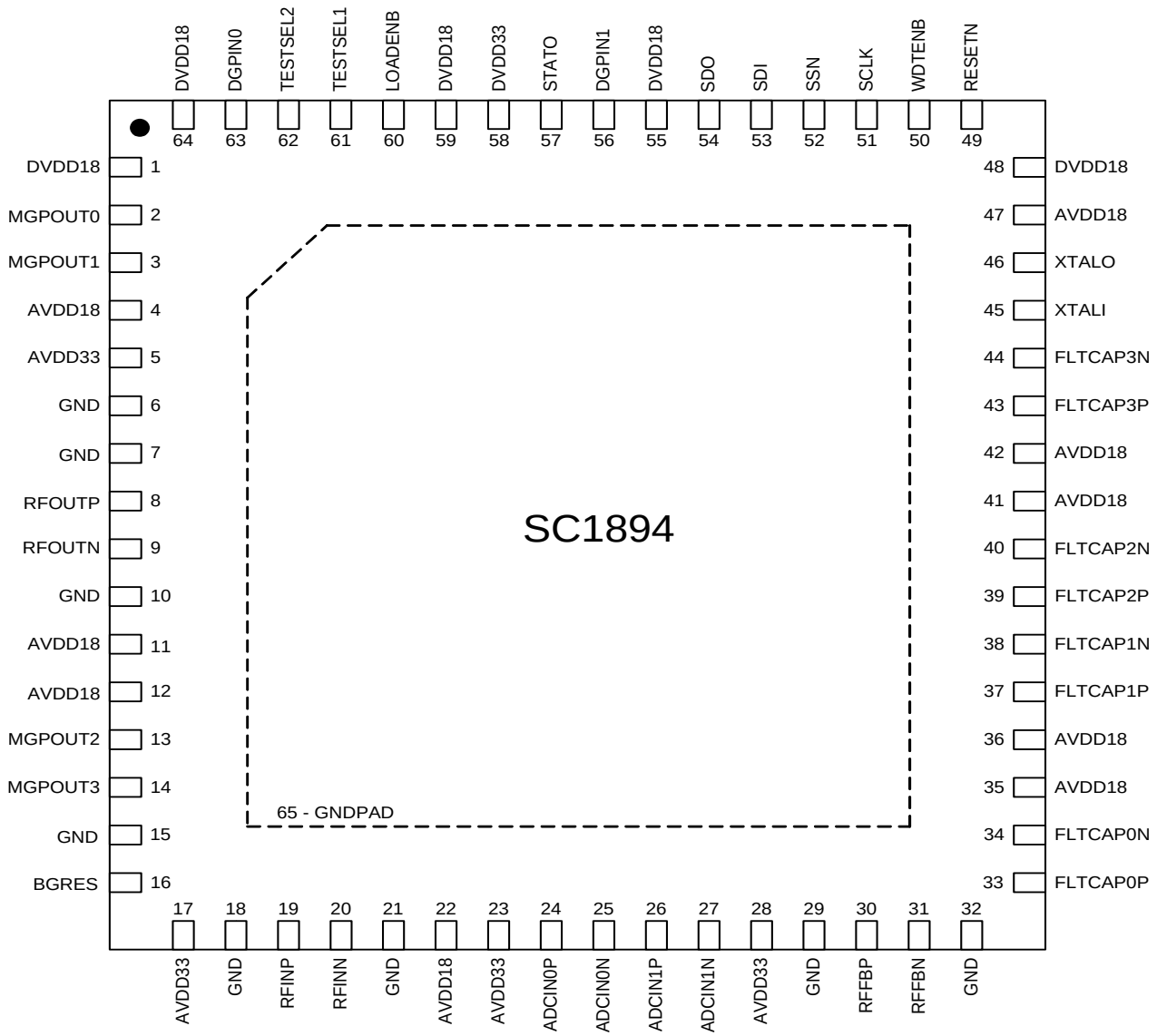
Introduction to Predistortion using the SC1894

Wideband signals in today's telecommunications systems have high peak-to-average ratios and stringent spectral regrowth specifications. These specifications place high linearity demands on power amplifiers. Linearity may be achieved by backing off output power at the price of reducing efficiency. However, this increases the component and operating costs of the power amplifier. Better linearity may be achieved through the use of digital pre-distortion and other linearization techniques, but many of these are time consuming and costly to implement.

Wireless service providers are deploying networks with wider coverage, greater subscriber density, and higher data rates. These networks require more efficient power amplifiers. Additionally, the emergence of distributed architectures and active antenna systems is driving the need for smaller and more efficient power amplifier implementations. Further, there continues to be a strong push toward reducing the total capital and operating costs of base stations.

With the SC1894, the complex signal processing is done in the RF domain. This results in a simple system-on-chip that offers wide signal bandwidth, broad frequency of operation, and very low power consumption. It is an elegant solution that reduces development costs and speeds time to market. Applicable across a broad range of signals — including 2G, 3G, 4G wireless, and other modulation types — the powerful analog signal processing engine is capable of linearizing the most efficient power amplifier topologies. The SC1894 is a true RFin and RFout solution, supporting modular power amplifier designs that are independent of the baseband and transceiver subsystems. The SC1894 delivers the required efficiency and performance demanded by today's wireless systems.

Pinout Configuration (Top View)



Pin Description

PIN	NAME	TYPE	FUNCTION
1	DVDD18	Supply	+1.8V DC Supply Voltage for digital circuits.
2	MGPOUT0	Analog Out	Mixed (Digital or Analog) General Purpose Output 0 Low frequency DAC#0 positive analog output (requires separate FW activation).
3	MGPOUT1	Analog Out	Mixed (Digital or Analog) General Purpose Output 1 Low frequency DAC#1 positive analog output (requires separate FW activation).
4	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
5	AVDD33	Supply	+3.3V DC Supply Voltage for analog circuits.
6	GND	Supply	Ground.
7	GND	RF Shield	Ground for shield of RF signal.
8	RFOUTP	Analog Out	RF Output Signal Positive, differential output. See S-parameters for complex impedance values.
9	RFOUTN	Analog Out	RF Output Signal Negative, differential output. See S-parameters for complex impedance values.
10	GND	RF Shield	Ground for shield of RF signal.
11	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
12	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
13	MGPOUT2	Analog Out	Mixed (Digital or Analog) General Purpose Output 3 Low frequency DAC#3 positive analog output (requires separate FW activation).
14	MGPOUT3	Analog Out	Mixed (Digital or Analog) General Purpose Output 4 Low frequency DAC#4 positive analog output (requires separate FW activation).
15	GND	Supply	Ground.
16	BGRES	Analog In	Bandgap Resistor.
17	AVDD33	Supply	+3.3V DC Supply Voltage for analog circuits.
18	GND	RF Shield	Ground for shield of RF signal.
19	RFINP	Analog In	RF Input Signal, differential input. See S-parameters for complex impedance values.
20	RFINN		
21	GND	RF Shield	Ground for shield of RF signal.
22	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
23	AVDD33	Supply	+3.3V DC Supply Voltage for analog circuits.
24	ADCIN0P	Analog In	Low frequency ADC#0 positive analog input (requires separate FW activation).
25	ADCIN0N	Analog In	Low frequency ADC#0 negative analog input (requires separate FW activation).
26	ADCIN1P	Analog In	Low frequency ADC#1 positive analog input (requires separate FW activation).
27	ADCIN1N	Analog In	Low frequency ADC#1 negative analog input (requires separate FW activation).
28	AVDD33	Supply	+3.3V DC Supply Voltage for analog circuits.
29	GND	RF Shield	Ground for shield of RF signal.
30	RFFBP	Analog In	RF Feedback Signal, differential input. See S-parameters for complex impedance values.
31	RFFBN		
32	GND	RF Shield	Ground for shield of RF signal.

PIN	NAME	TYPE	FUNCTION
33	FLTCAP0P	Analog Out	Dedicated external filter capacitor #0.
34	FLTCAP0N		
35	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
36	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
37	FLTCAP1P	Analog Out	Dedicated external filter capacitor #1.
38	FLTCAP1N		
39	FLTCAP2P	Analog Out	Dedicated external filter capacitor #2.
40	FLTCAP2N		
41	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
42	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
43	FLTCAP3P	Analog Out	Dedicated external filter capacitor #3.
44	FLTCAP3N		
45	XTALI	Analog In	Crystal Input. For standard internal clock, connect crystal or ceramic resonator from XTALI to XTALO. May alternatively be driven by an external clock.
46	XTALO	Analog Out	Crystal Output. Excitation driver for crystal or ceramic resonator.
47	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
48	DVDD18	Supply	+1.8V DC Supply Voltage for digital circuits.
49	RESETN	Digital In	Reset when "Low". Has internal pull-up to DVDD33.
50	WDTENB	Digital In	Watch Dog Timer Enable. WDTENB enabled when high. Has internal pull-up to DVDD33. See applications schematic for further details.
51	SCLK	Digital In	SPI clock. Has internal pull-down to GND.
52	SSN	Digital In	SPI slave select enabled "Low". Has internal pull-up to DVDD33.
53	SDI	Digital In	SPI slave data input to RFPAL. Has internal pull-down to GND.
54	SDO	Digital Out	SPI slave data output from RFPAL. Tri-state. DVDD33 logic.
55	DVDD18	Supply	+1.8V DC Supply Voltage for digital circuits.
56	DGPIN1	Digital In	Digital General Purpose Input 1. Has internal pull-up to DVDD33. See Firmware Release Notes for further details.
57	STATO	Digital Out	General Purpose Status Output as defined in Firmware Release Notes. Open-drain output with internal pull-up to DVDD33.
58	DVDD33	Supply	+3.3V DC Supply Voltage for digital circuits.
59	DVDD18	Supply	+1.8V DC Supply Voltage for digital circuits.
60	LOADENB	Digital In	Load Enable. Required for FW upgrades. Has internal pull-down to GND. See applications schematic for further details.
61	TESTSEL1	Reserved	Do not connect. Reserved for internal use. Has internal pull-down to GND.
62	TESTSEL2	Reserved	Do not connect. Reserved for internal use. Has internal pull-down to GND.
63	DGPIN0	Digital In	Digital General Purpose Input 0. Do not connect. Reserved for future use. Has internal pull-down to GND. See applications schematic for further details.
64	DVDD18	Supply	+1.8V DC Supply Voltage for digital circuits.
65	GNDPAD	Supply	Common Ground for entire integrated circuit. Also provides path for thermal dissipation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD33 to GND).....-0.3 V to +3.8 V
Supply Voltage (VDD18 to GND).....-0.2 V to +2.2 V
Input Voltage (1.8 V pins).. -0.2 V to VDD18 + 0.2 V
Input Voltage (3.3 V pins).. -0.3 V to VDD33 + 0.3 V
Input into the BALUN (RMS) .....+7 dBm
Junction Temperature ..... +150 ºC
Storage Temperature .....-65 ºC to +150 ºC

Warning: Any stress beyond the ranges indicated may damage the device permanently. The specified stress ratings do not imply functional performance in these ranges. Exposure of the device to the absolute maximum ratings for extended periods of time is likely to degrade the reliability of this product

OPERATING RATING

Operating Case Temperature……-40 ºC to +105 ºC

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage (VDD33 to GND)	3.1	3.3	3.5	V
Supply Voltage (VDD18 to GND)	1.7	1.8	1.9	V
Supply Peak Current (VDD33 to GND)[1,2,3,4]		100	120	mA
Supply Peak Current (VDD18 to GND)[1,2,3,4]		840	900	mA
Average Power Dissipation: Full Scale Adaptation, Track & AF[2,3,4]		1200	1400	mW
Average Power Dissipation: Duty Cycled Feedback[2,4,5]		600		mW

1 – Peak Current includes supply decoupling network. Refer to Hardware Design Guide for proper sizing of the on board-regulators.
2 – Characterized at typical voltages, 25°C operating case temperature and 20MHz input signal BW.
3 – Continuous adaptation, tracking (100% duty cycled feedback), and Advanced Features active or inactive.
4 – Power dissipation may be FW dependent. Refer to the FW release notes for any changes to values listed above.
5 – Duty cycled feedback power dissipation averaged over ON time of 100ms (9%), OFF time of 1.0s (91%) and Advanced Features are active or inactive.

RADIO FREQUENCY SIGNALS

Operation at 25 °C, AVDD18 = 1.8 V, AVDD33 = 3.3 V, DVDD18 = 1.8 V and 20 MHz external clock unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency[1]	F		225		3800	MHz
Input Signal Bandwidth[2]	BW_{signal}		1.2		75[3]	MHz
Noise Power[4]		Referred to 0dBm at PA input		-140	-137	dBm/Hz

1 – See Operating Frequency Ranges table for frequency limits of each defined band. For operation from 225 MHz to less than 470 MHz, please contact factory. Operation in this range is for prototyping purposes only.
2 – In the case where 40MHz < $BW_{signal} \leq$ 75 MHz and the carrier configuration is NON-fully occupied, then the average power delta between the two outermost carriers must be $\leq$ 20 dB, the carrier configuration must be static (no hopping), the outermost carriers must be $\geq$ 5MHz and the F_c must be stored in EEPROM.
3 – Correction performance across range of input signal BWs also depends on PA output power and carrier configuration.
4 – Worst case over supply voltage and temperature range.

RF INPUT RANGE FOR MAXIMUM CORRECTION – 225 MHz to 470 MHz *(For Prototyping Only)*

Operation at 25 °C, AVDD18 = 1.8 V, AVDD33 = 3.3 V, DVDD18 = 1.8 V and 20 MHz external clock unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak RFIN_BLN[1,3]	$P_{RFIN\_BLN\_P}$	When PA operates at maximum power	-6	0	+2	dBm
Peak RFFB_BLN[1,3]	$P_{RFFB\_BLN\_P}$		-16	-8	-6	dBm
RMS RFIN_BLN[2,3]	P_{RFIN_BLN}		-13	-10	-8	dBm
RMS RFFB_BLN[2,3]	P_{RFFB_BLN}		-23	-18	-16	dBm
RFIN_BLN Operating Range	P_{RFIN_BLN}	RMS Power, over PA output power range	-48		-8	dBm
RFFB_BLN Operating Range	P_{RFFB_BLN}		-56		-16	dBm

RF INPUT RANGE FOR MAXIMUM CORRECTION – 470 MHz to 700 MHz

Operation at 25 °C, AVDD18 = 1.8 V, AVDD33 = 3.3 V, DVDD18 = 1.8 V and 20 MHz external clock unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak RFIN_BLN[1,3]	$P_{RFIN\_BLN\_P}$	When PA operates at maximum power	-6	0	+2	dBm
Peak RFFB_BLN[1,3]	$P_{RFFB\_BLN\_P}$		-16	-8	-6	dBm
RMS RFIN_BLN[2,3]	P_{RFIN_BLN}		-13	-10	-8	dBm
RMS RFFB_BLN[2,3]	P_{RFFB_BLN}		-23	-18	-16	dBm
RFIN_BLN Operating Range	P_{RFIN_BLN}	RMS Power, over PA output power range	-48		-8	dBm
RFFB_BLN Operating Range	P_{RFFB_BLN}		-56		-16	dBm

RF INPUT RANGE FOR MAXIMUM CORRECTION – 700 MHz to 2700 MHz

Operation at 25 °C, AVDD18 = 1.8 V, AVDD33 = 3.3 V, DVDD18 = 1.8 V and 20 MHz external clock unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak RFIN_BLN[1,3]	$P_{RFIN\_BLN\_P}$	When PA operates at maximum power	-2	+4	+6	dBm
Peak RFFB_BLN[1,3]	$P_{RFFB\_BLN\_P}$		-12	-4	-2	dBm
RMS RFIN_BLN[2,3]	P_{RFIN_BLN}		-9	-6	-4	dBm
RMS RFFB_BLN[2,3]	P_{RFFB_BLN}		-19	-14	-12	dBm
RFIN_BLN Operating Range	P_{RFIN_BLN}	RMS Power, over PA output power range	-49		-4	dBm
RFFB_BLN Operating Range	P_{RFFB_BLN}		-52		-12	dBm

RF INPUT RANGE FOR MAXIMUM CORRECTION – 2700 MHz to 3300 MHz

Operation at 25 °C, AVDD18 = 1.8 V, AVDD33 = 3.3 V, DVDD18 = 1.8 V and 20 MHz external clock unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak RFIN_BLN[1,3]	$P_{RFIN\_BLN\_P}$	When PA operates at maximum power		+6		dBm
Peak RFFB_BLN[1,3]	$P_{RFFB\_BLN\_P}$			-4		dBm
RMS RFIN_BLN[2,3]	P_{RFIN_BLN}			-4		dBm
RMS RFFB_BLN[2,3]	P_{RFFB_BLN}			-14		dBm
RFIN_BLN Operating Range	P_{RFIN_BLN}	RMS Power, over PA output power range	-44		-4	dBm
RFFB_BLN Operating Range	P_{RFFB_BLN}		-54		-14	dBm

RF INPUT RANGE FOR MAXIMUM CORRECTION – 3300 MHz to 3800 MHz

Operation at 25 °C, AVDD18 = 1.8 V, AVDD33 = 3.3 V, DVDD18 = 1.8 V and 20 MHz external clock unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak RFIN_BLN[1,3]	$P_{RFIN\_BLN\_P}$	When PA operates at maximum power	+3	+9	+11	dBm
Peak RFFB_BLN[1,3]	$P_{RFFB\_BLN\_P}$		-12	-4	-2	dBm
RMS RFIN_BLN[2,3]	P_{RFIN_BLN}		-4	-1	+1	dBm
RMS RFFB_BLN[2,3]	P_{RFFB_BLN}		-19	-14	-12	dBm
RFIN_BLN Operating Range	P_{RFIN_BLN}	RMS Power, over PA output power range	-41		+1	dBm
RFFB_BLN Operating Range	P_{RFFB_BLN}		-52		-12	dBm

1 – Peak power is defined as the 10^{-4} point on the CCDF (Complementary Cumulative Distribution Function) of the signal.
2 – Power (MAX RMS) + PAR must not exceed the Peak Power limits specified above, there is no maximum limit on the PAR.
3 – Referred to 50 Ω impedance into a 1:2 balun.

OPERATING FREQUENCY RANGES

FREQUENCY RANGE[1]	RECOMMENDED APPLICATIONS	DESIGNATION
225 MHz to 520 MHz	TV White Space	-02
225 MHz to 960 MHz	UHF broadcast, TV White Space, public safety	-03
520 MHz to 1040 MHz	Low band cellular (698 MHz to 960 MHz), UHF broadcast, TV White Space, public safety	-04
1040 MHz to 2080 MHz	LTE for Japan (1400 MHz to 1510MHz)	-05
698 MHz to 2700 MHz	Low and high band cellular, IF for SATCOMM (950 MHz to 1450 MHz)	-06
1800 MHz to 2700 MHz (DEFAULT)	High Band cellular (1800 MHz to 2700 MHz)	-07
2700 MHz to 3500 MHz		-08
3300 MHz to 3800MHz	Microwave (IF), WiMAX	-09

1 – Default is -07. User may reprogram for other ranges listed above. Refer to design guide for programming information.

DIGITAL I/O – DC CHARACTERISTICS

Guaranteed performance across worst case supply voltage and temperature range unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS Input logic low	V_{IL}		-0.3		0.8	V
CMOS Input logic high	V_{IH}	VDD = 3.3V	2.0			V
CMOS Output logic low	V_{OL}				0.4	V
CMOS Output logic high	V_{OH}	VDD = 3.3V	2.4			V
SDO CMOS Output Current	I_{OL} / I_{OH}	Tri-State	-16.0		16.0	mA
STATO CMOS Output Current	I_{OL} / I_{OH}	Open Drain	-16.0		0.0	mA
MGPOUT0-3 CMOS Output logic high	V_{OH}	VDD = 1.8 V	1.5			V
MGPOUT0-3 CMOS Output logic low	V_{OL}				0.3	V
MGPOUT0-3 CMOS Output Current[1]	I_{OL} / I_{OH}		-10.0		5.0	mA

1 –May be reprogrammed by user for analog output. Refer to SC1894-Advanced-Features13_Datasheet for detailed specifications.

DIGITAL I/O – EXTERNAL CLOCK (XTALI)

Guaranteed performance across worst case supply voltage and temperature range unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
User Programmable External Clock[1,2]	F_{CLK}		10	20	30.72	MHz
External Clock Frequency Accuracy					1	%
External Clock Frequency Drift		Including aging and temperature			100	ppm
Duty Cycle		Square wave	45		55	%
External Clock Amplitude	V_{CLK}	Sine or square wave	500		1500	mV_{p-p}
External Clock Phase Noise	PN_{CLK}	At TBD offset			TBD	dBc/Hz

1 – Selecting an external reference clock frequency other than 20 MHz requires programming the SC1894 through the SPI bus. See Programming Guide and HW Design Guide for more information.
2 – User may program the SC1894 to accept the following clock frequencies: 10, 13, 15.36, 19.2, 20, 26 and 30.72 MHz

CRYSTAL REQUIREMENTS

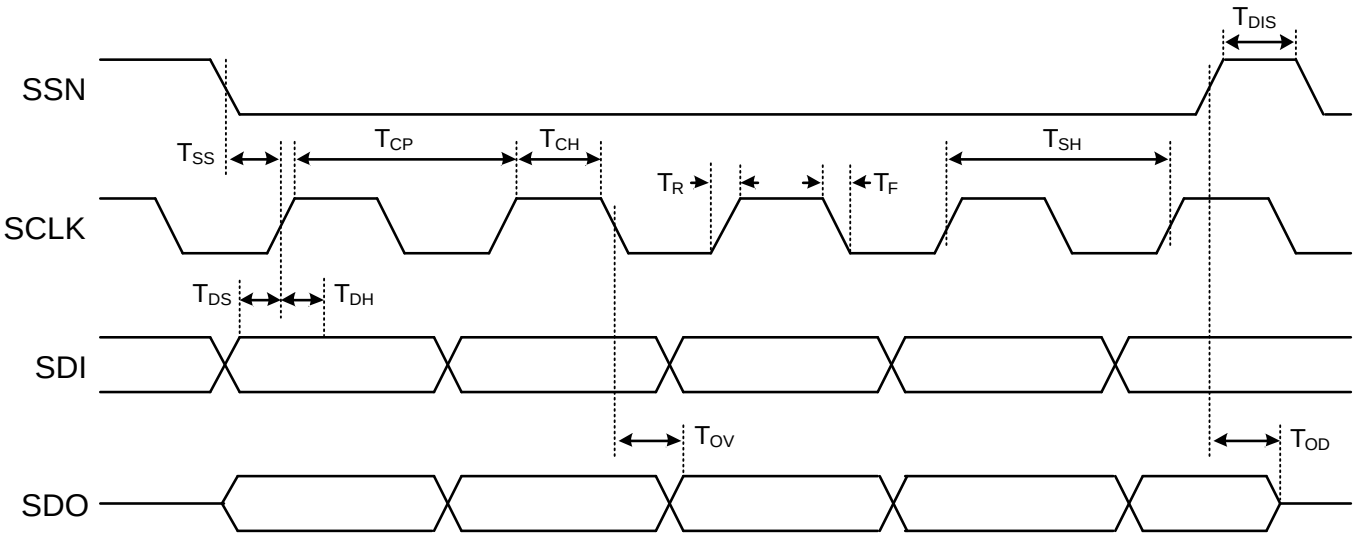
Guaranteed performance across worst case supply voltage and temperature range unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESR					50	Ω
Capacitive load to ground				10	12	pF
Frequency Accuracy					250	ppm
Frequency Drift		Including aging and temperature			100	ppm

SERIAL PERIPHERAL INTERFACE (SPI) BUS SPECIFICATIONS

Guaranteed performance across worst case supply voltage and temperature range unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Select Setup Time	T_{SS}		100			ns
Select Hold Time	T_{SH}		250			ns
Select Disable Time	T_{DIS}		100			ns
Data Setup Time	T_{DS}		25			ns
Data Hold Time	T_{DH}		45			ns
Rise Time	T_R				25	ns
Fall Time	T_F				25	ns
Clock Period	T_{CP}		250			ns
Clock High Time	T_{CH}		100			ns
Time to Output Valid	T_{OV}				100	ns
Output Data Disable	T_{OD}				0	ns



When used in its base linearizer configuration (Product Configuration (PC) = 00), use of the SPI is optional as the SC1894 is capable of fully autonomous operation.

Use of the Advanced Features (Product Configuration (PC) = 13) require that the SPI bus be connected to a host controller in order to read or write customer accessible parameters.

EEPROM Endurance

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM write/erase cycles		Page mode, 25°C	1M			E/W Cycles

Top Mark

LINE	TOP MARK	DESCRIPTION
1	SCINTERA	Company Name
2	SC1894	Product Part Number
2	A	Product Revision
2	-00 -13	Product Configuration (PC): -00 = RFPAL Base Configuration -13 = RFPAL + Advanced Features
3	XXXXXXXXXX	Assembly Lot Number (up to 10 characters)
4	WW	Date Code - Work Week
4	YY	Date Code - Year
4	RRRR	Reserved

ESD

ESD (Electro-Static Discharge) sensitive device. Although this product incorporates ESD protection circuitry, permanent damage may occur on devices subjected to electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or device failure.

Electro-Static Discharge (ESD) Protection Characteristics

TEST METHODOLOGY	CLASS	VOLTAGE	UNIT
Human Body Model (per JESD22-A114)	1C	1000	V
Charge Device Model (per JESD22-C101)	II	250	V

Package Information

Specifications regarding the 64-pin, 9mm x 9mm QFN package and the recommended solder pad layout are available online at http://www.scintera.com/pdfs/64p-9x9QFN-package-and-solder-pad-information.pdf.

Additional information regarding quality, reliability, package and environmental information can be found online at http://www.scintera.com/resource-center/quality-reliability-package-environmental-information/.

Product Ordering Information

PART NUMBER	DESCRIPTION
SC1894A-00A00	IC, RFPAL, 225-3800 MHz, FW4.0.05.10 NOT RECOMMENDED FOR NEW DESIGNS
SC1894A-00B00	IC, RFPAL, 225-3800 MHz, FW4.1.01
SC1894A-00B13PS*	IC, RFPAL + Advanced Features, 225-3800 MHz, FW4.1.XX, Final PON = SC1894A-00B13

* Prototype samples are available now. Production available in Q4'2013.

Note: PON (Part Ordering Number)

Shipping designator:
E = 7" tape & reel
Append shipping designator (E) at end of part number. If left blank, designates bulk shipping option.

Evaluation Kit Ordering Information

PART NUMBER	DESCRIPTION
SC1894-EVK200	Eval Kit, RFPAL, 225-470 MHz (For Prototyping Only)
SC1894-EVK500	Eval Kit, RFPAL, 470-928 MHz
SC1894-EVK900	Eval Kit, RFPAL, 698-960 MHz
SC1894-EVK1500*	Eval Kit, RFPAL, 1350-1800 MHz
SC1894-EVK1900	Eval Kit, RFPAL, 1800-2200 MHz
SC1894-EVK2400	Eval Kit, RFPAL, 2300-2700 MHz
SC1894-EVK3400	Eval Kit, RFPAL, 3300-3800 MHz
SC-USB-SPI	Adapter, SPI-USB Interface/Controller

* Please contact Scintera Sales for availability.

EVKs will ship with most recent release of FW and with all available functions enabled.

For More Information Contact Scintera:

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