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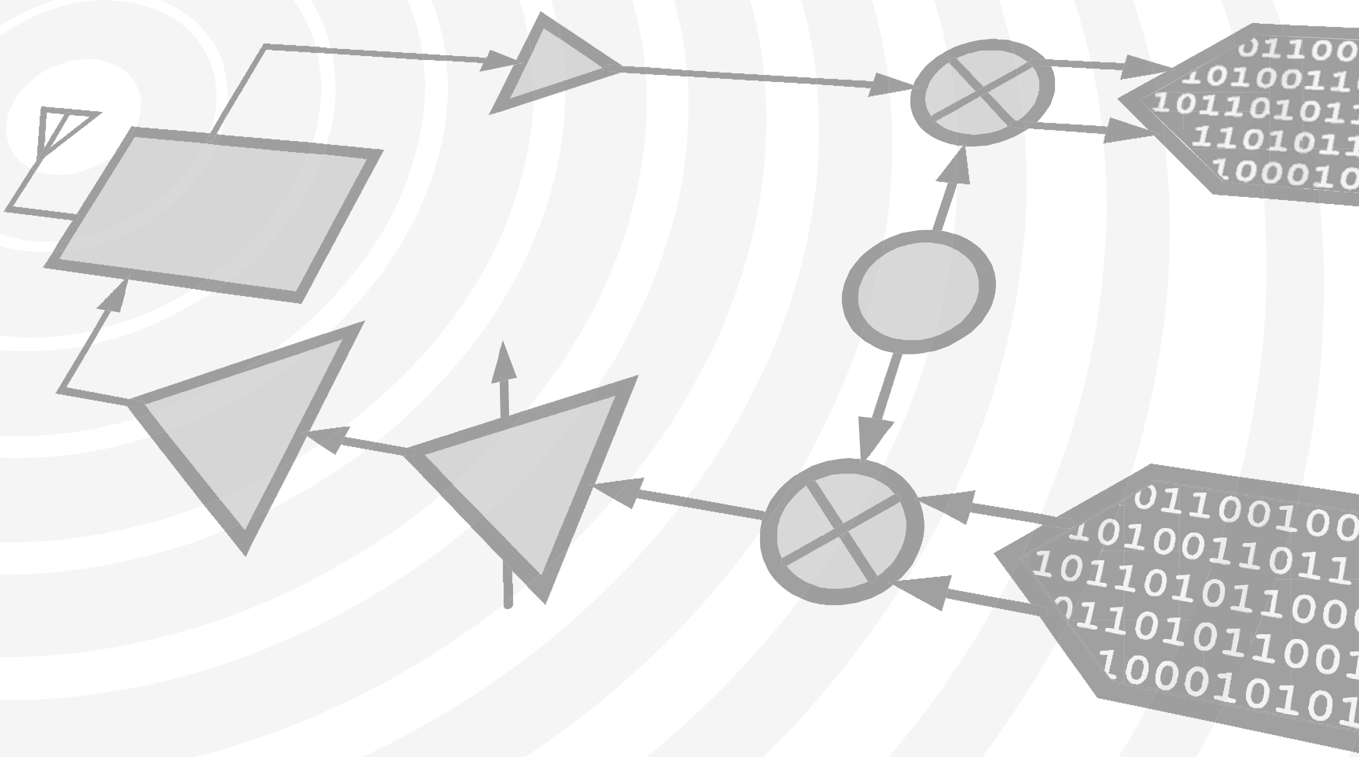
NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



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HMC6590

43 Gbps TRANSIMPEDANCE AMPLIFIER

Typical Applications

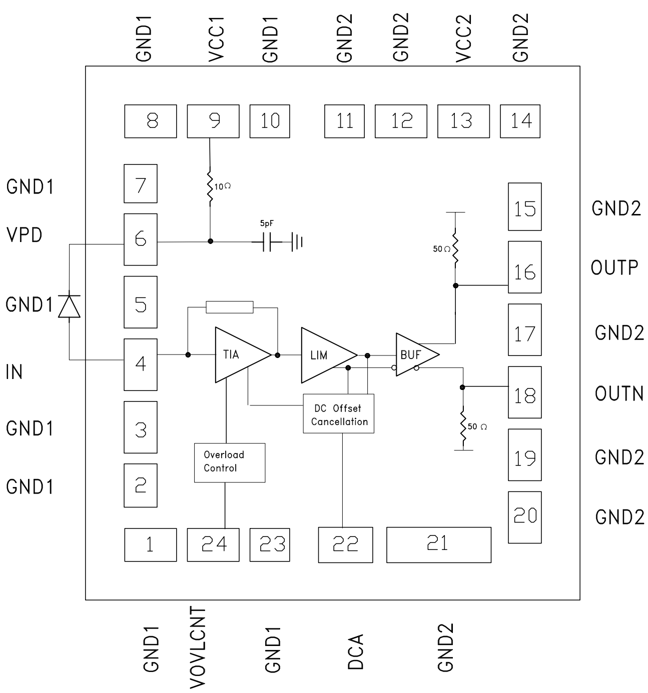
The HMC6590 is ideal for:

- 40 GbE-FR
- 40 GBps VSR / SFF
- Short, intermediate, and long-haul optical receivers

Features

- Supports data rates up to 43 Gbps
- Internal DCA feedback with external adjustment option
- 4 Kohm differential transimpedance gain
- Low-power dissipation < 300 mW
- -10.5 dBm optical input sensitivity
- +5 dBm optical overload
- Small die size: 1.15 mm x 1.21 mm x 0.15 mm

Functional Diagram



General Description

The HMC6590 is a high-speed, high gain, low-power limiting transimpedance amplifier (TIA) used in optical receivers with data rates up to 43 Gbps. It features low input referred noise, 36 GHz bandwidth, 4 kohm differential small signal transimpedance and output cross point adjustment. HMC6590 exhibits an optical input dynamic range between -10 dBm and +5 dBm while maintaining 10e-12 BER at 43 Gbps operation.

The HMC6590 is available in die form, includes an on-chip VCC bypass capacitor. It requires only supply decoupling capacitor as external component.

The HMC6590 requires a single 3.3V ±5% supply and it typically dissipates less than 300 mW. The device is characterized for operation from –5 °C to +85 °C temperature.

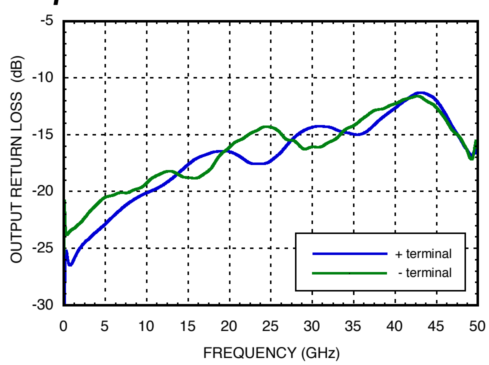
43 Gbps TRANSIMPEDANCE AMPLIFIER

Electrical Specifications, T_A = +25°C, Vcc = 3.3V

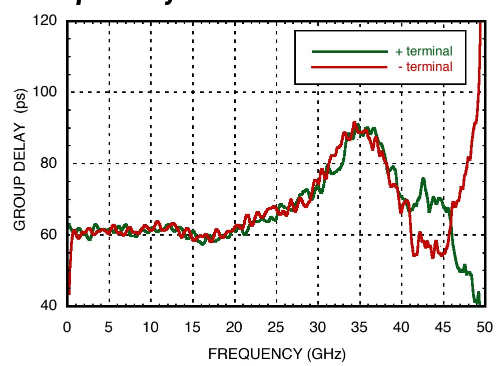
Parameter	Conditions	Min.	Typ.	Max.	Units
Max Data Rate	NRZ	43			Gbps
Z21 Small Signal Bandwidth[3]	3 dB cut off		39		GHz
Z21 3 dB Low Cutoff Frequency			50		KHz
Transimpedance (Z21)	Differential @ 100 MHz		4		KOhm
Group Delay Variation	Up to 40 GHz		± 15		psec
Differential Output Swing	@ 43 Gbps (saturated)		450		mVp-p
Input Referred RMS Noise	Up to 35 GHz		3.3		uA
Input Referred Noise Densitiy.	RMS noise per 35 GHz		20		pA/√Hz
Optical Input Sensitivity[1] (OMA)	Responsivity = 0.65A/W, ER = 9 dB		-10.5		dBm
Optical Overload Power[2] (OMA)	Responsivity = 0.65 A/W, ER = 9dB		+5		dBm
Input Overload Current			4		mAp-p
Output Return Loss (S22)	Up to 40 Ω GHz			-10	dB
Additive RMS Jitter	40 Gbps 1010... stream			0.5	ps
Input DC Voltage	Internally generated		1.2		V
Operational Supply Voltage Range	± 5%	3.15	3.3	3.45	V
Supply Current	Vcc = 3.3V		94		mA
Operating Temperature Range (Die backside)		-5		+85	°C

[1] Sensitivity depends on photo diode, packaging, BERT sensitivity, input eye quality and optical coupling.
[2] Vovlcnt= 1.7V
[3] 50 Ω on wafer measurement results.

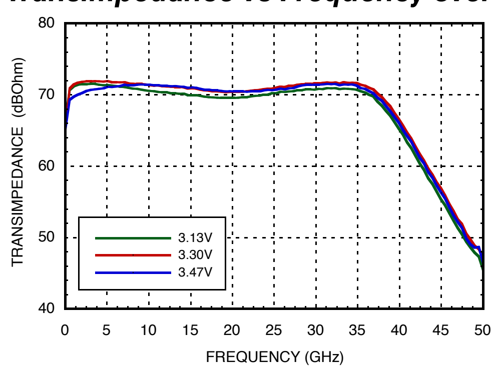
Output Return Loss @ VCC = 3.3V[1]



Group Delay @ VCC = 3.3V[1]



Transimpedance vs Frequency over Supply[2]

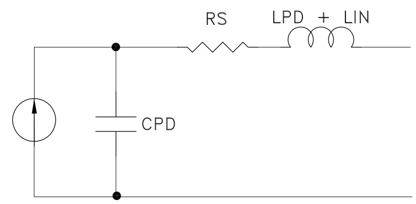


[1] 50 Ω on wafer measurement results .
[2] Assumes photo diode and assembly model on page 3.

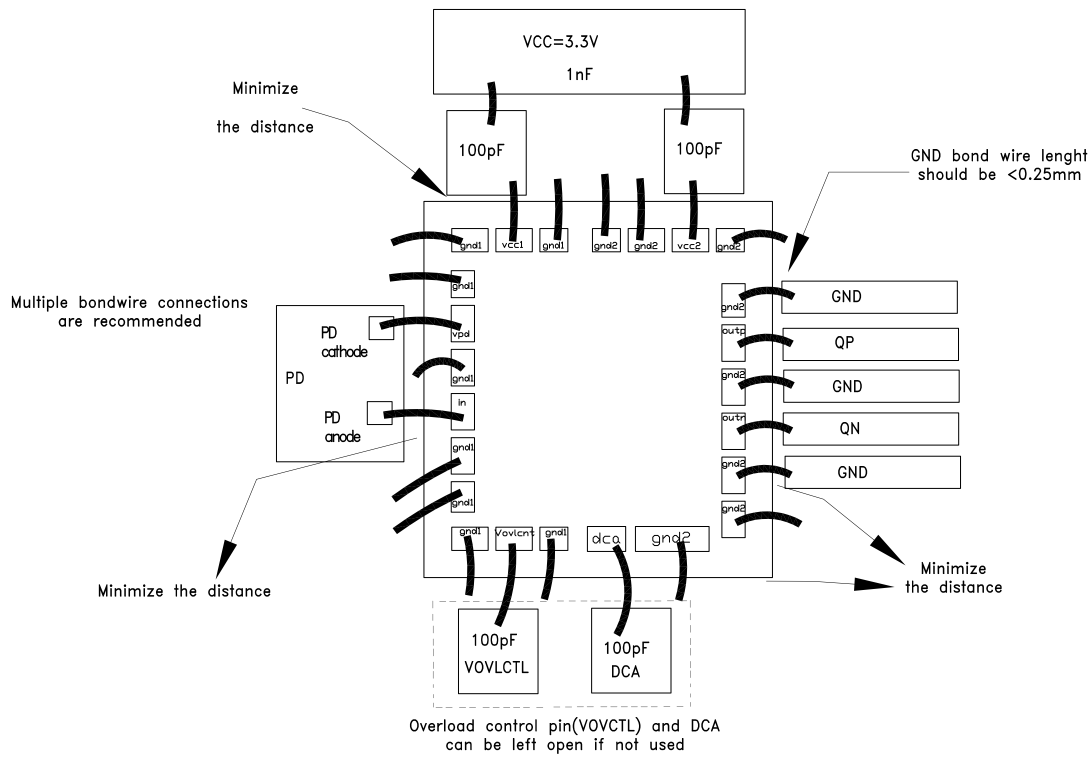
Photo Diode Model and Assembly Assumptions

Photo diode and assembly diagram model used in Z21 and input referred noise density calculations:

- C_{PD} = 50 fF
- R_S = 15 Ω
- $L_{PD}+L_{IN}$ = 0.35 nH
- L_{OUT} = 0.25 nH
- L_{GND} = 0.25 nH
- L_{VDD} = 0.25 nH



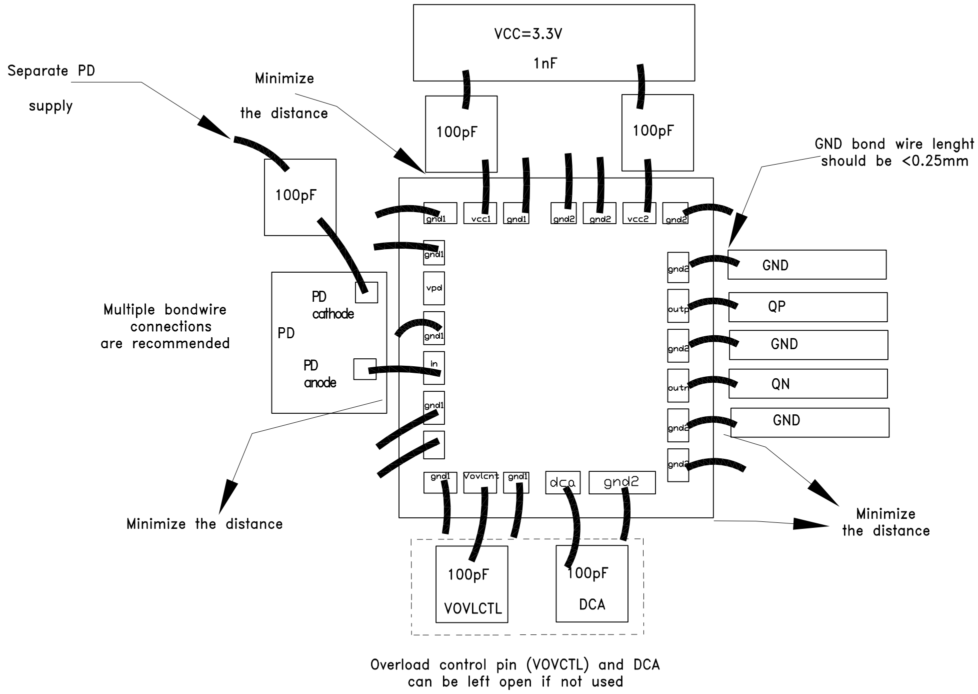
Assembly Diagram for Using Integrated Photo Diode Supply VPD



Suggested assembly configuration for using internal supply for photo-diode. Suggested bond-wire length for optimum performance is as follows:

- $L_{PD} + L_{IN}$ < 0.35 mm
- L_{OUT} < 0.25 mm (double-bond is recommended)
- L_{GND} < 0.25 mm (double-bond for larger pads)
- L_{VCC} < 0.25 mm (double-bond is recommended)

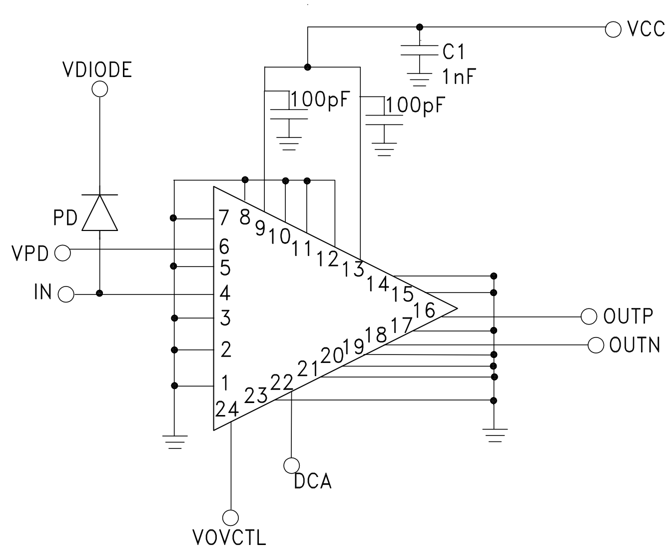
Assembly Diagram for Separate Photo Diode Supply



Suggested assembly configuration for separate photo diode supply. Suggested bond-wire length for optimum performance is as follows:

- $L_{PD} + L_{IN} < 0.35$ mm
- $L_{OUT} < 0.25$ mm (double-bond is recommended)
- $L_{GND} < 0.25$ mm (double-bond for larger pads)
- $L_{VCC} < 0.25$ mm (double-bond is recommended)

Application Circuit



RoHS✓ EARTH FRIENDLY

Absolute Maximum Ratings

Voltage level at the RF input (Vin)	-0.6V to 2.5V
Current level at the RF input (In)	0 to 10 mA
Voltage level at the RF output	VCC-1 to VCC+1
Supply Voltage (VCC)	-0.6V to 3.75V
Max. Junction Temperature	125 °C
Continuous Pdiss (T=85°C) (Derate 30.23 mW/°C above 85°C)	1.21 W
Thermal Resistance R_{th} (Junction to die bottom)	33.08 °C/W
Storage Temperature	-55 to +125 °C
Operating Temperature (Die backside)	-5 to +85 °C
ESD Sensitivity Level (HBM)	Class 0 (>150V)

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Die Packaging Drawing [1]

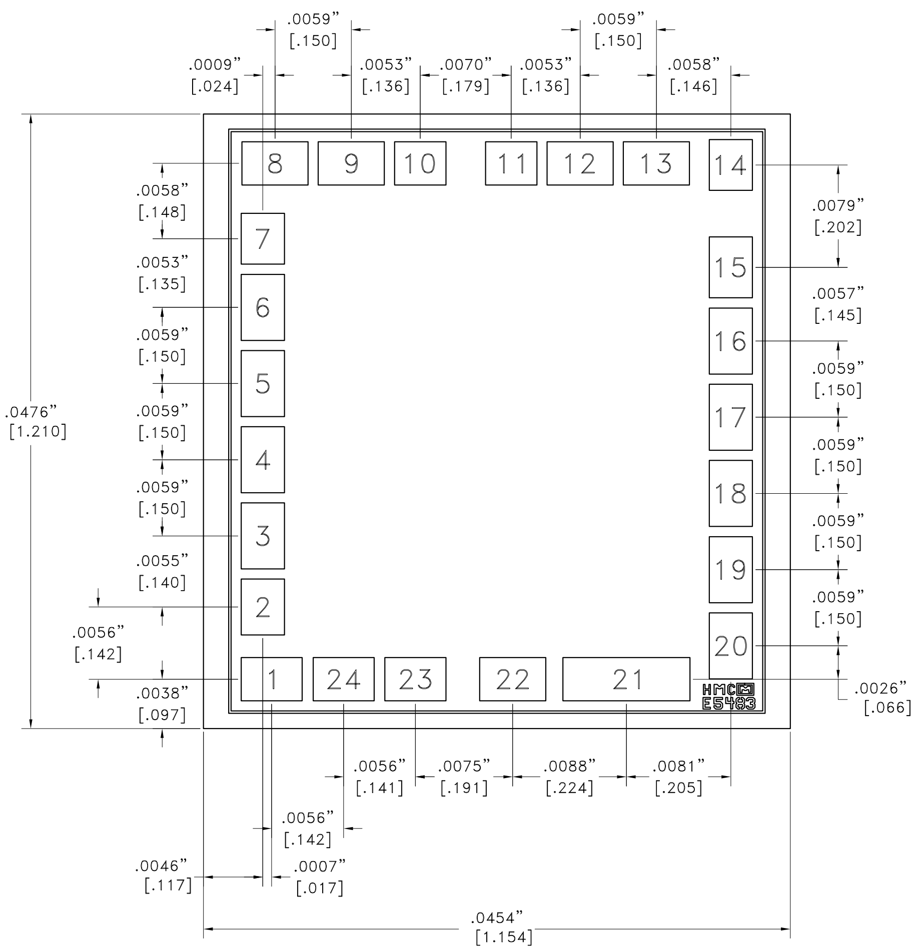
Standard	Alternate
GP-1 (Gel Pack)	[2]

[1] For more information refer to the "Packaging Information" Document in the Product Support Section of our website .
[2] For alternate packaging information contact Hittite Microwave Corporation.

Die Pads Dimensions

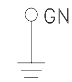
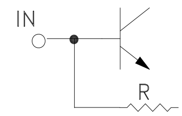
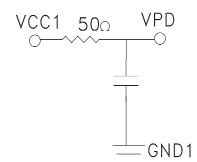
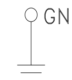
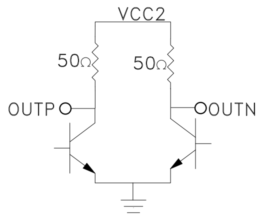
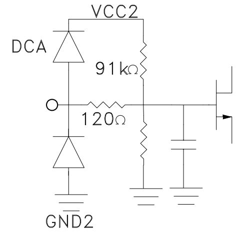
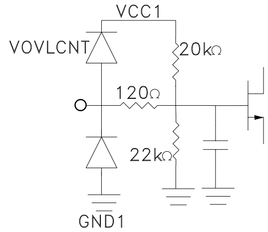
Pads	Pad Size
1,23,24	0.0047[0.120] X 0.0033[0.085]
2	0.0033[0.085] X 0.0043[0.110]
3-6,16-20	0.0033[0.085] X 0.0051[0.130]
7	0.0033[0.085] X 0.0039[0.100]
8,9,12,13,22	0.0051[0.130] X 0.0033[0.085]
10,11	0.0040[0.101] X 0.0033[0.085]
14	0.0033[0.085] X 0.0093[0.100]
15	0.0033[0.085] X 0.0047[0.120]
21	0.0098[0.250] X 0.0033[.085]

Outline Drawing



NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MM]
2. DIE THICKNESS IS .006"
3. BOND PAD METALIZATION: ALUMINUM
4. NO BACKSIDE METAL
5. OVERALL DIE SIZE ±.002"

Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1,2,3,5,7,8,10 23,26	GND1	Ground connection for TIA.	
4	IN	TIA input.	
6	VPD	Provides bias voltage for photo-diode (PD) through a 50 Ω resistor/capacitor network from VCC1.	
9	VCC1	Power supply for input stage and PD.	
11,12,14,15,17 19-22,25	GND2	Ground connection for TIA.	
13	VCC2	Power supply for output buffers.	
16	OUTP	Non-inverted data output with 50 Ω back termination.	
18	OUTN	Inverted data output with 50 Ω back termination.	
22	DCA	DC offset control. Voltage at this pad sets output DC offset. When it is floating, DC offset is at 0V.	
24	VOVLCNT	Overload current compensation control. Voltage at this pad sets the strength of the input overload current control. When it is floating, overload control is set to nominal(VCC1/2). Overload performance can be optimized by adjusting VOVLCNT voltage between 1.6V - 3.3V .	

Mounting & Bonding Techniques for MMICs

The die should be attached directly to the ground plane with epoxy (see HMC general Handling, Mounting , Bonding Note).

50 Ω Microstrip transmission lines on 0.254 mm (10 mil) thick alumina thin film substrates are recommended for bringing high speed differential signal from the chip RF to and from the chip (Figure 1).

Microstrip substrates should be placed as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076 mm to 0.152 mm (3 to 6 mils).

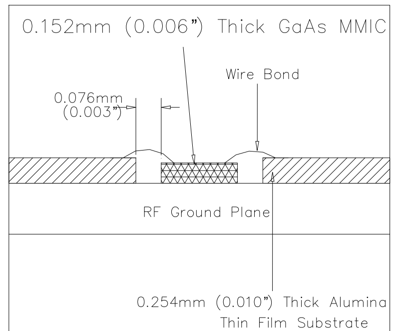


Figure 1.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: The chip may be handled by a vacuum collet or with a pair of sharp tweezers.

Mounting

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.