AH323

2W High Linearity 5V 2-Stage Amplifier

Applications

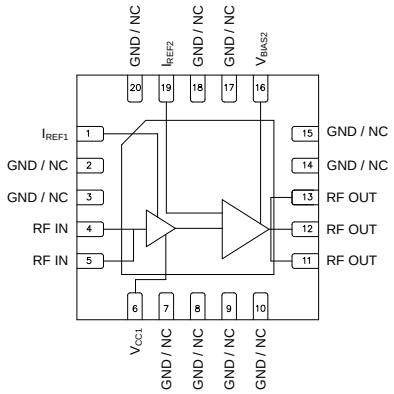
- Base stations / Repeaters
- High Power Amplifiers
- 2G / 3G / 4G Wireless Infrastructure
- Femtocells
- LTE / WCDMA / CDMA

20 Pin 5x5 mm QFN Package

Product Features

- 700-2700 MHz
- 27.2 dB Gain at 2140 MHz
- +33 dBm P1dB
- High linearity: +50 dBm OIP3
- 24 dBm Output Power at -50 dBc WCDMA ACLR
- Integrated interstage matching
- Excellent return loss (>14 dB)
- +5V Supply Voltage
- MTTF > 1000 Years

Functional Block Diagram



General Description

The AH323 is a high dynamic range two-stage driver amplifier in a low-cost surface-mount package. The amplifier is able to achieve high performance across a broad range of frequencies with +50 dBm OIP3 and +33 dBm P1dB while only consuming 680 mA current. The InGaP/GaAs HBT integrates two high performance amplifier stages onto a MMIC to allow for a more compact system design. The integrated interstage match minimizes performance variation that would otherwise be attributed to external matching component value and placement tolerances. The AH323 is available in a standard lead-free /green/RoHS-compliant 20 pin 5x5mm QFN package. All devices are 100% RF and DC tested.

The AH323 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. This driver amplifier is able to deliver high power while maintaining superior ACLR performance. The integrated active bias circuitry in the devices enable excellent linearity performance over temperature with little variance.

The AH323 is footprint compatible with other TriQuint 2W devices such as the AH314 for 2.3-2.9GHz applications.

Pin Configuration

Pin No.	Label
1	I_{REF1}
4,5	RF In
6	V_{CC1}
11,12,13	RF Out / V_{CC2}
16	V_{BIAS2}
19	I_{REF2}
2,3,7,8,9,10,14,15, 17,18,20	N/C or GND
Backside Paddle	GND

Ordering Information

Part No.	Description
AH323-G	2W 5V 2-stage Amplifier
AH323-PCB2140	2140 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150°C
RF Input Power, CW, 50Ω, T=25°C	+18 dBm
Supply Voltage (V_{CC})	+8 V
Device Current	1900 mA
Power Dissipation	8 W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{CC})		5.0	6.0	V
T_{CASE}	−40		+85	°C
Tj for >10^6 hours MTTF			+200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

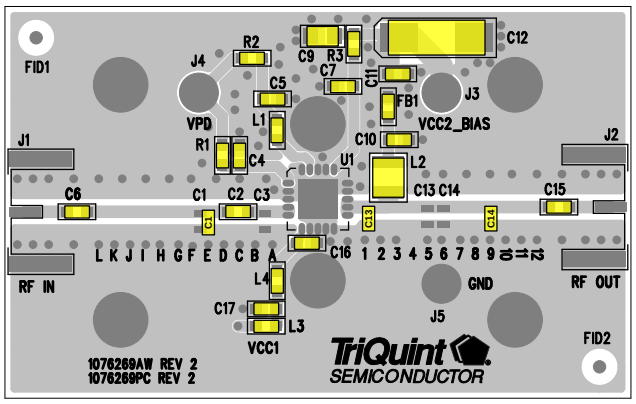
Test conditions unless otherwise noted: $V_{CC} = V_{PD}$ = +5V, Temp= +25°C, 50 Ω system.

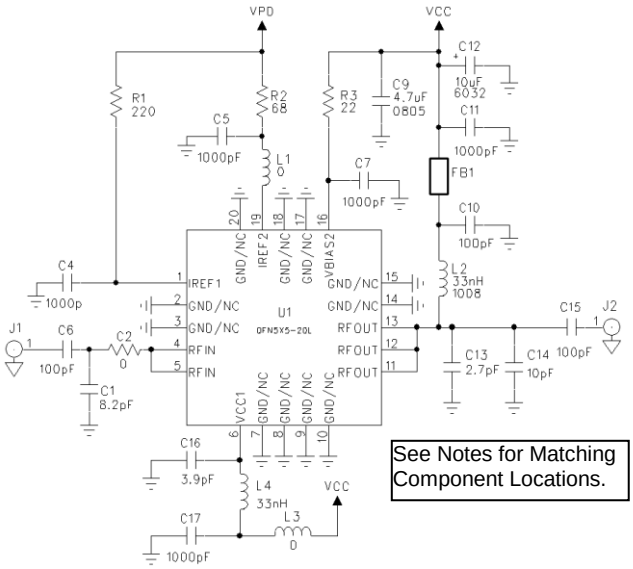
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		700		2700	MHz
Test Frequency			2140		MHz
Gain		24.2	27.2		dB
Input Return Loss			25		dB
Output Return Loss			17		dB
Output P1dB		+32.4	+33.1		dBm
Output IP3	Pout = +20 dBm/tone, Δf = 1 MHz	+44.5	+50		dBm
WCDMA Channel Power [1]	ACLR = -50 dBc		+23.9		dBm
Reference Current	$I_{REF1} + I_{REF2}$		35		mA
Quiescent Current, Icq	$I_{CQ1} + I_{CQ2}$	600	700	800	mA
Thermal Resistance, θ_{jc}	Module (junction to case)			11.7	°C/W

Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

Reference Design 700-800 MHz





Notes:
1. See PC Board Layout, page 15 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C1 is placed at 250 mils from the U1 device package (10° @ 750 MHz).
6. The edge of C13 is placed at 50 mils from the edge of U1 device package (2° @ 750 MHz).
7. The edge of C14 is placed at 440 mils from the edge of U1 device package (17.5° @ 750 MHz).
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.
12. C16 is critical for large signal performance.

Typical Performance 700-800 MHz

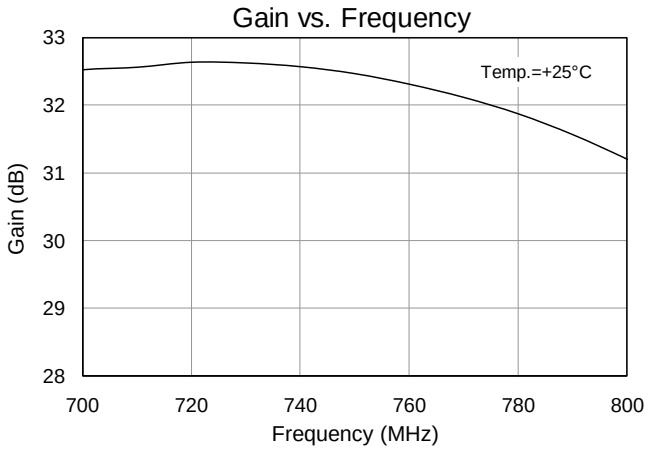
Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

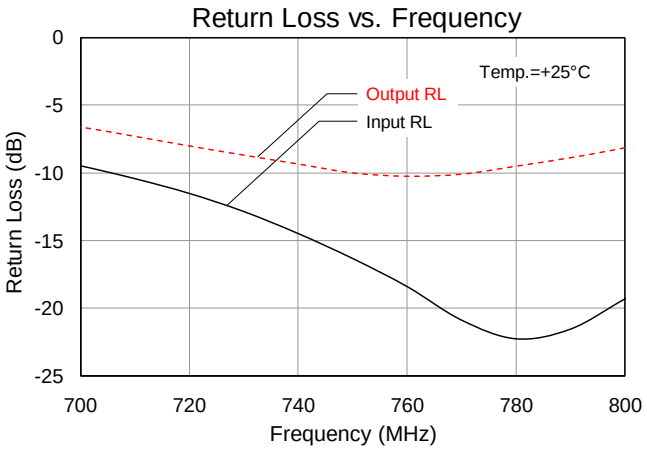
Parameter	Conditions				Units
Frequency		700	750	800	MHz
Gain		32.5	32.5	31.2	dB
Input Return Loss		9.5	16	19	dB
Output Return Loss		6.6	10	8	dB
Output P1dB		+32.5	+33	+32.6	dBm
OIP3	Pout = +24 dBm/tone, Δf = 1 MHz	+45	+45.7	+45	dBm
WCDMA Channel Power [1]	ACLR = -50 dBc	+22.7	+23.1	+23.6	dBm

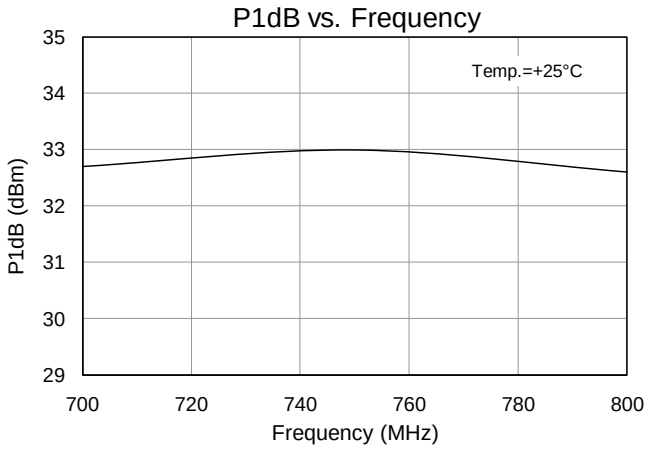
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

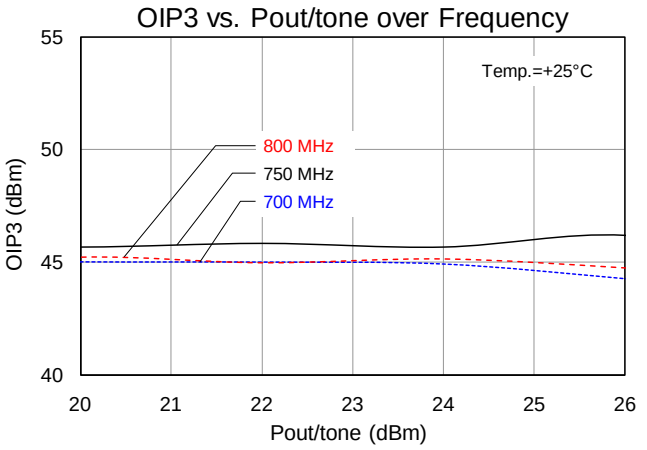
Performance Plots 700-800 MHz

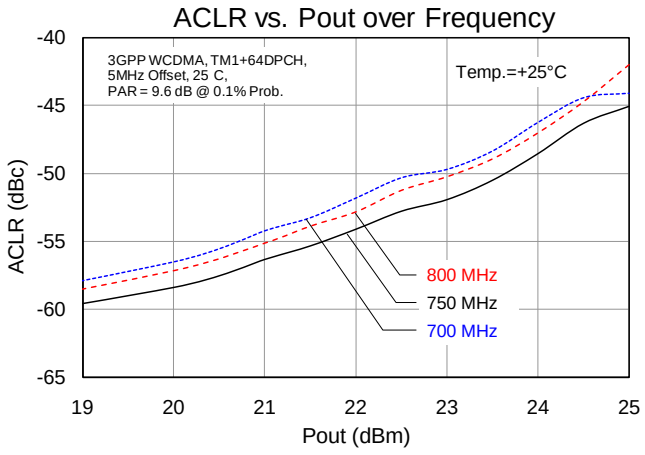
Test conditions unless otherwise noted: $V_{CC} = V_{PD}$ = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)



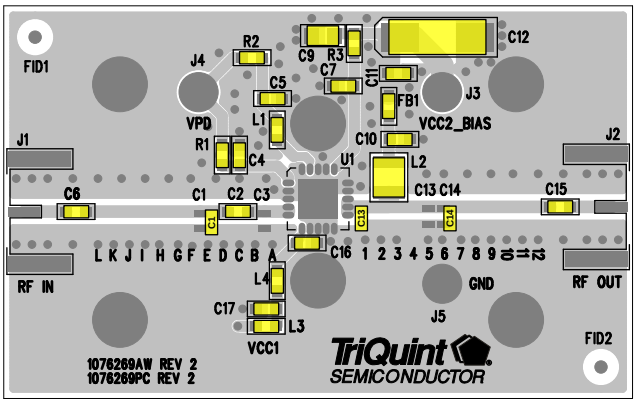


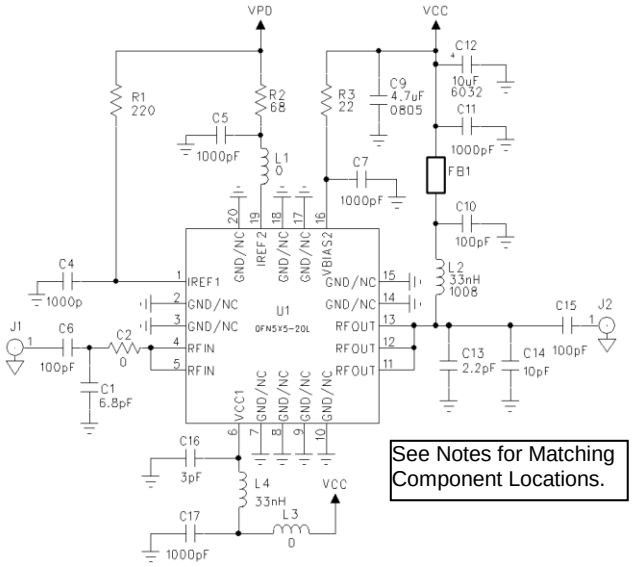






Reference Design 800-900 MHz





Notes:

1. See PC Board Layout, page 15 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C1 is placed at 225 mils from the edge of U1 device package (10° @ 850 MHz).
6. The edge of C13 is placed at 10 mils from the edge of U1 device package (0.5° @ 850 MHz).
7. The edge of C14 is placed at 320 mils from the edge of U1 device package (14.5° @ 850 MHz).
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.
12. C16 is critical for large signal performance.

Typical Performance 800-900 MHz

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

Parameter	Conditions				Units
Frequency		800	850	900	MHz
Gain		31.9	32	31.1	dB
Input Return Loss		9	14	23	dB
Output Return Loss		7.7	15	11.7	dB
Output P1dB		+33	+33.7	+34	dBm
OIP3	Pout = +24 dBm/tone, Δf = 1 MHz	+46	+45.5	+45.3	dBm
WCDMA Channel Power [1]	ACLR = -50 dBc	+23.4	+24.1	+24.1	dBm

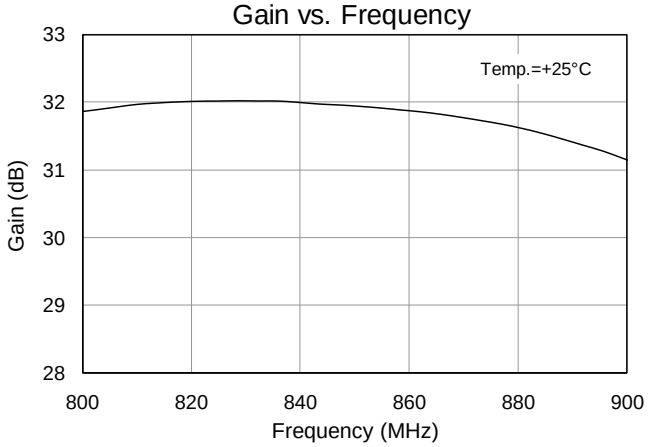
Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

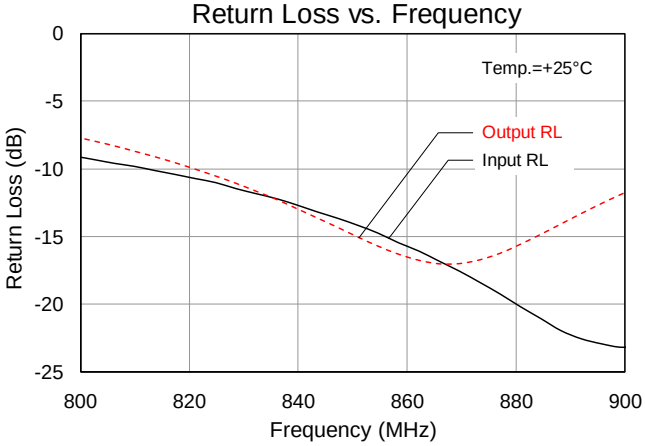
Performance Plots 800-900 MHz

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

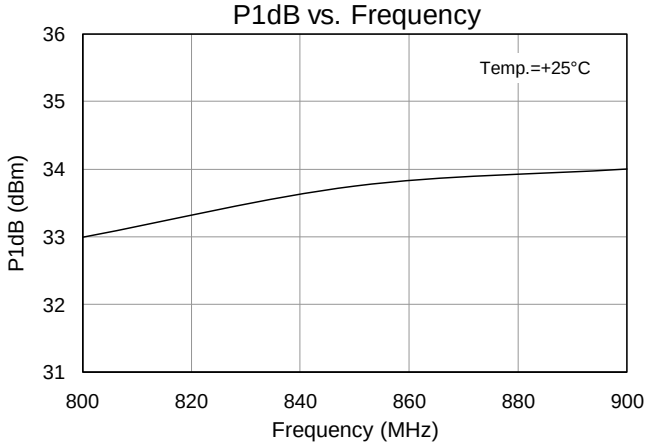
Gain vs. Frequency



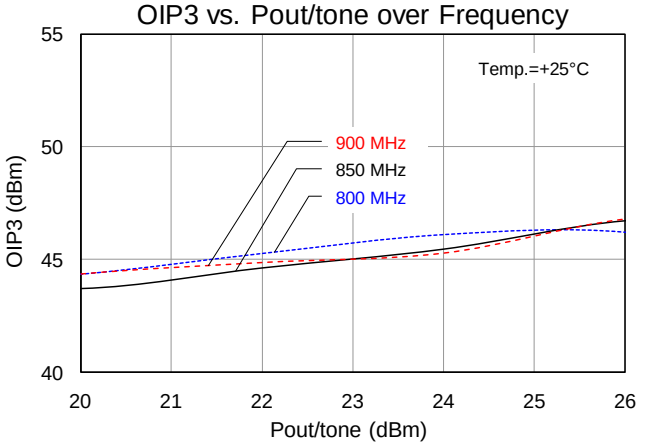
Return Loss vs. Frequency



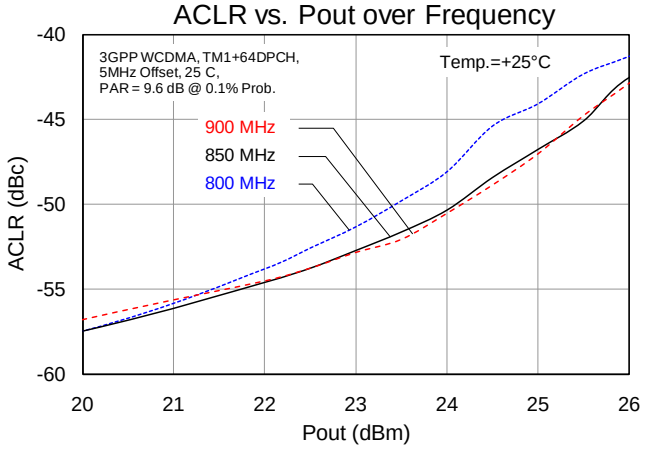
P1dB vs. Frequency



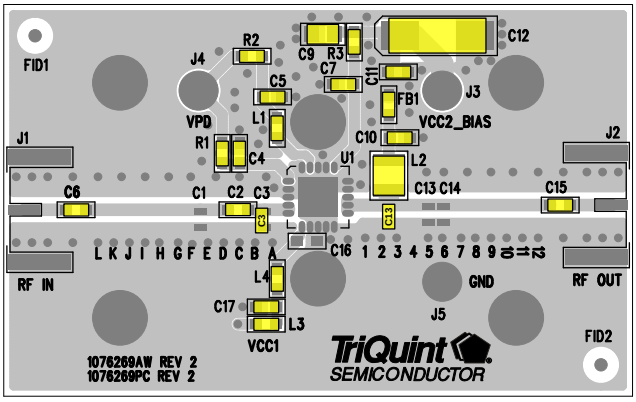
OIP3 vs. Pout/tone over Frequency

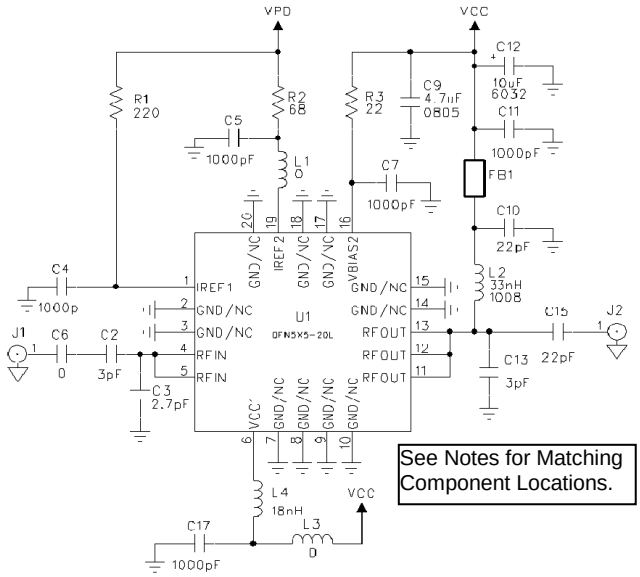


ACLR vs. Pout over Frequency



Reference Design 1800-1900 MHz





Notes:

1. See PC Board Layout, page 15 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C2 is placed at 128 mils from the U1 device package (12.5° @ 1850 MHz).
6. The edge of C3 is placed at 70 mils from the edge of U1 device package (7° @ 1850 MHz).
7. The edge of C13 is placed at 110 mils from the edge of U1 device package (10.7° @ 1850 MHz).
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.

Typical Performance 1800-1900 MHz

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

Parameter	Conditions				Units
Frequency		1800	1850	1900	MHz
Gain		28.6	28.8	28.6	dB
Input Return Loss		13	17.6	20.5	dB
Output Return Loss		10.5	13	14.4	dB
Output P1dB		+33.2	+33.3	+33.1	dBm
OIP3	Pout = +24 dBm/tone, Δf = 1 MHz	+49	+50	+49	dBm
WCDMA Channel Power [1]	ACLR = -50 dBc	+23.7	+23.9	+23.9	dBm

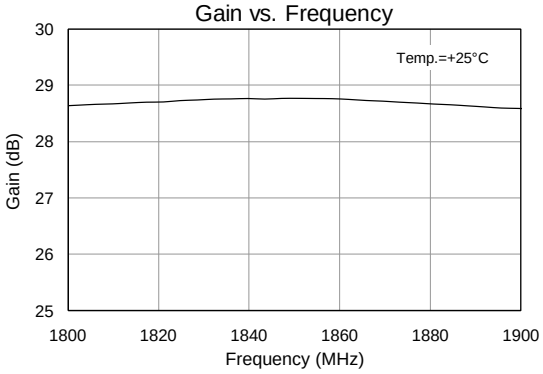
Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

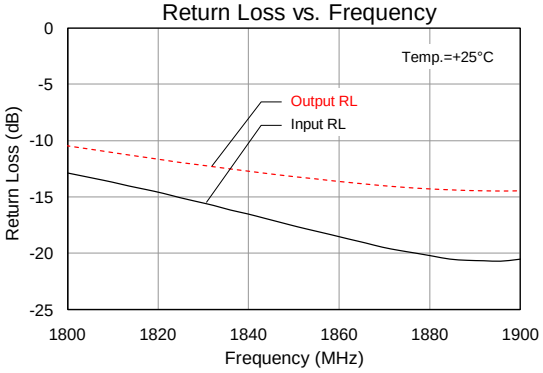
Performance Plots 1800-1900 MHz

Test conditions unless otherwise noted: $V_{CC} = V_{PD}$ = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

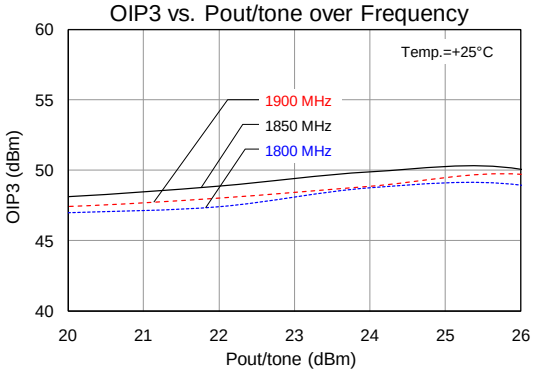
Gain vs. Frequency



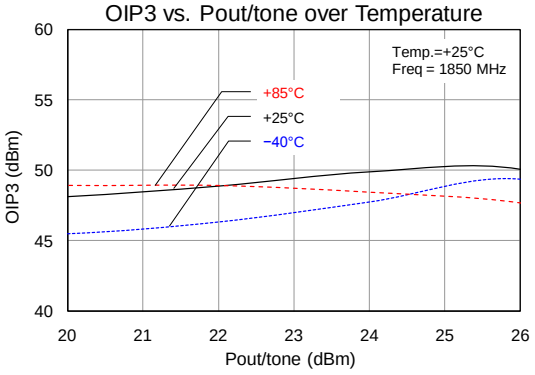
Return Loss vs. Frequency



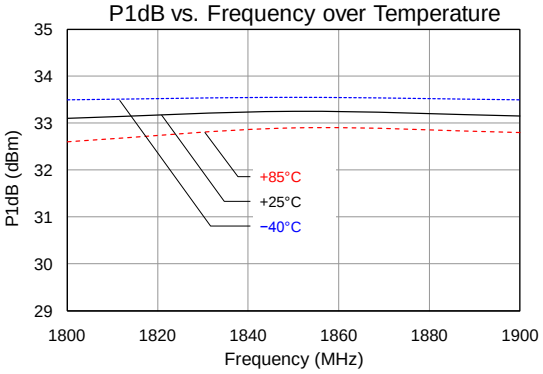
OIP3 vs. Pout/tone over Frequency



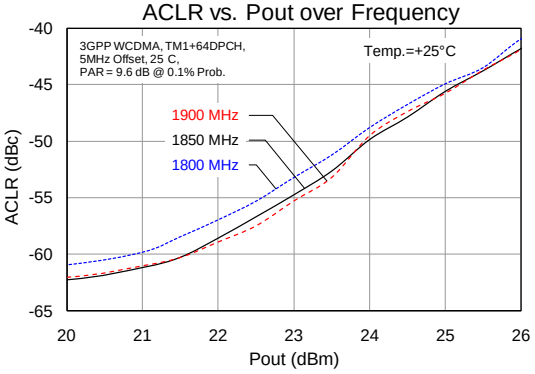
OIP3 vs. Pout/tone over Temperature



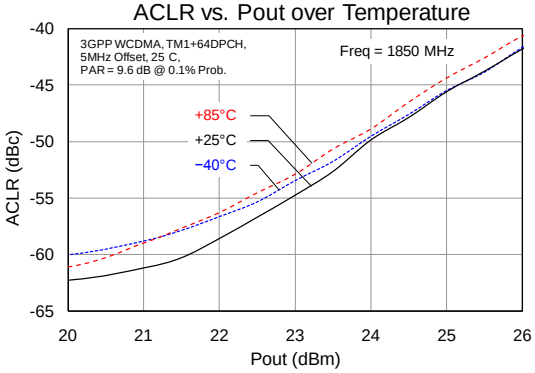
P1dB vs. Frequency over Temperature



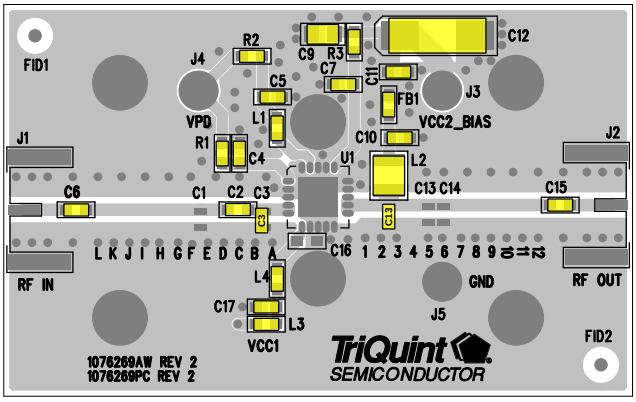
ACLR vs. Pout over Frequency

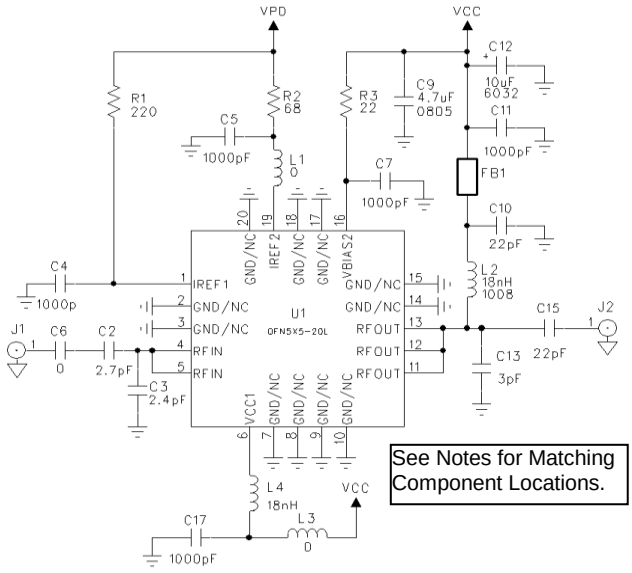


ACLR vs. Pout over Temperature



Reference Design 1930-1990 MHz





Notes:
1. See PC Board Layout, page 15 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C2 is placed at 128 mils from the U1 device package (13° @ 1960 MHz).
6. The edge of C3 is placed at 70 mils from the edge of U1 device package (7.3° @ 1960 MHz).
7. The edge of C13 is placed at 100 mils from the edge of U1 device package (10.4° @ 1960 MHz).
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.

Typical Performance 1930-1990 MHz

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

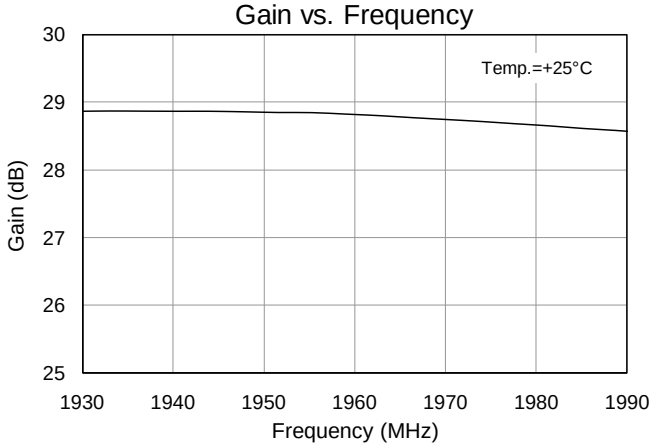
Parameter	Conditions				Units
Frequency		1930	1960	1990	MHz
Gain		28.9	28.8	28.6	dB
Input Return Loss		20	24	22	dB
Output Return Loss		16.5	19.6	20.6	dB
Output P1dB		+33.2	+33.1	+33.1	dBm
OIP3	Pout = +24 dBm/tone, Δf = 1 MHz	+50.3	+50.3	+50.3	dBm
WCDMA Channel Power [1]	ACLR = -50 dBc	+24	+23.8	+23.8	dBm

Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

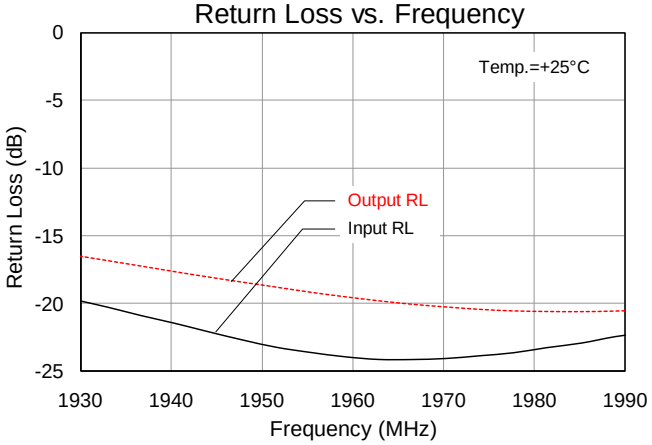
Performance Plots 1930-1990 MHz

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

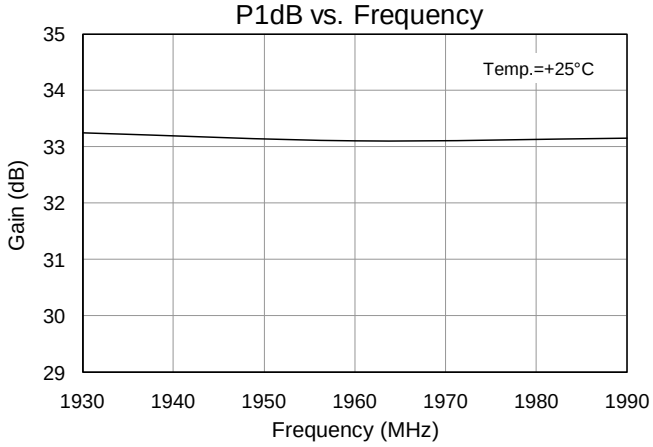
Gain vs. Frequency



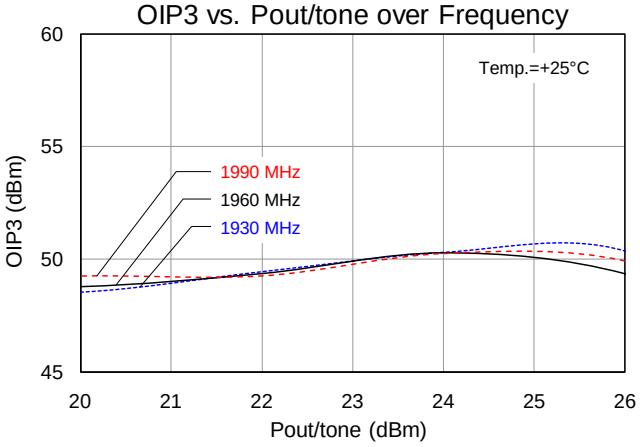
Return Loss vs. Frequency



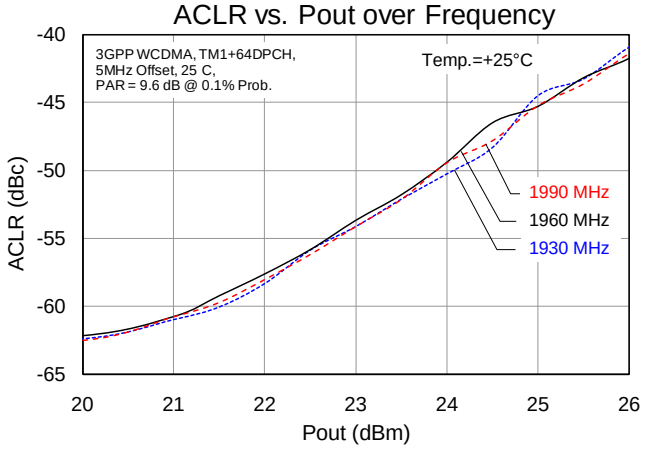
P1dB vs. Frequency



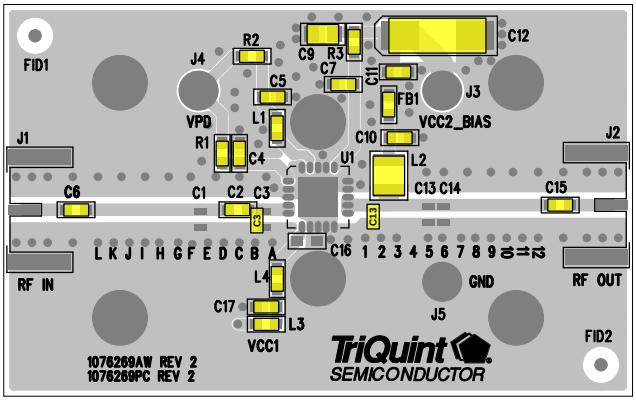
OIP3 vs. Pout/tone over Frequency

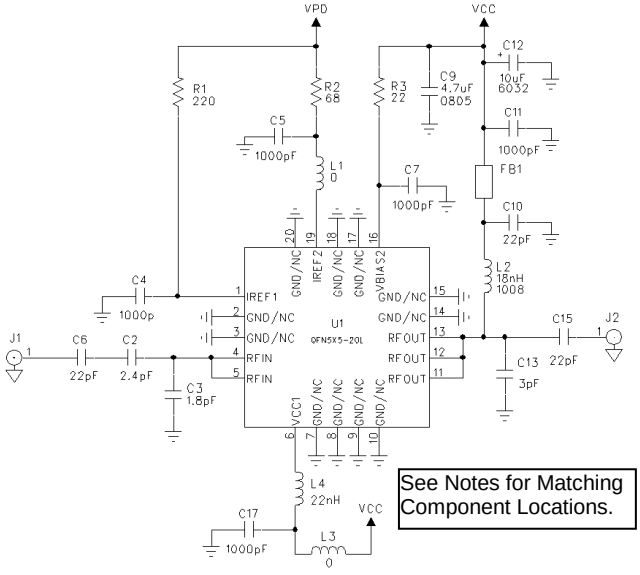


ACLR vs. Pout over Frequency



AH323-PCB2140 Evaluation Board (2110−2170 MHz)





Notes:

1. See PC Board Layout, page 15 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C2 is placed at 128 mils from the U1 device package (14.5° @ 2140 MHz).
6. The edge of C3 is placed at 80 mils from the edge of U1 device package (9° @ 2140 MHz).
7. The edge of C13 is placed at 70 mils from the edge of U1 device package (8° @ 2140 MHz).
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.
12. Low cost ceramic SQ series capacitors are used for matching.

Typical Performance – AH323-PCB2140

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

Parameter	Conditions				Units
Frequency		2110	2140	2170	MHz
Gain		27.3	27.2	27.0	dB
Input Return Loss		20	25	32	dB
Output Return Loss		17	16.6	17	dB
Output P1dB		+33.2	+33.1	+33.1	dBm
OIP3	Pout = +24 dBm/tone, Δf = 1 MHz	+49.7	+50	+50	dBm
WCDMA Channel Power [1]	ACLR = -50 dBc	+24	+23.9	+23.9	dBm
Noise Figure		4.2	4.2	4.3	dB

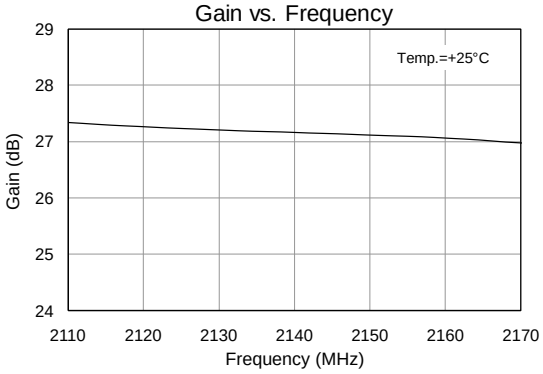
Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

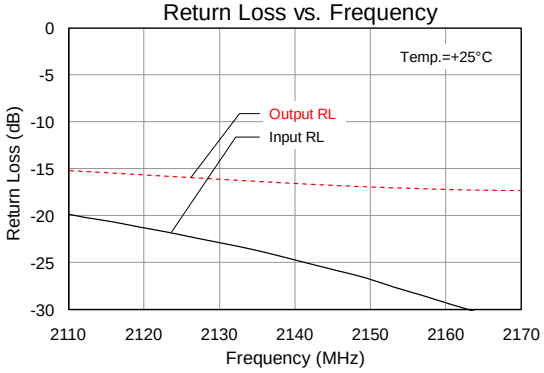
Performance Plots – AH323-PCB2140

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

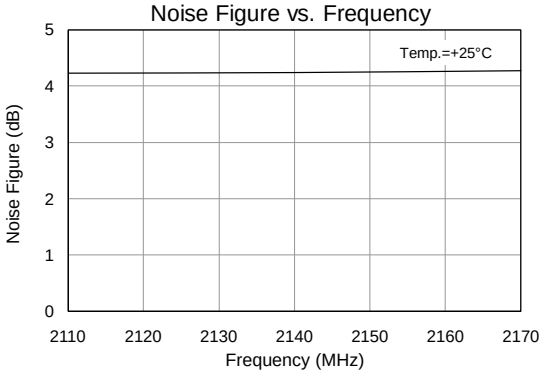
Gain vs. Frequency



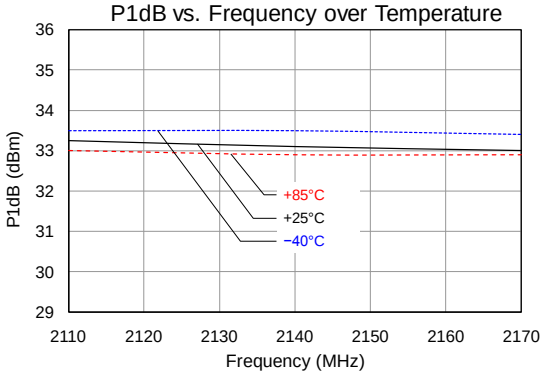
Return Loss vs. Frequency



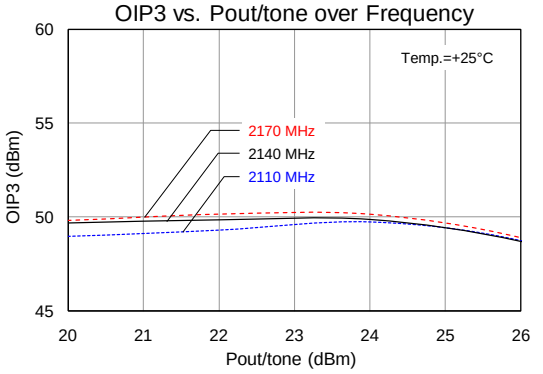
Noise Figure vs. Frequency



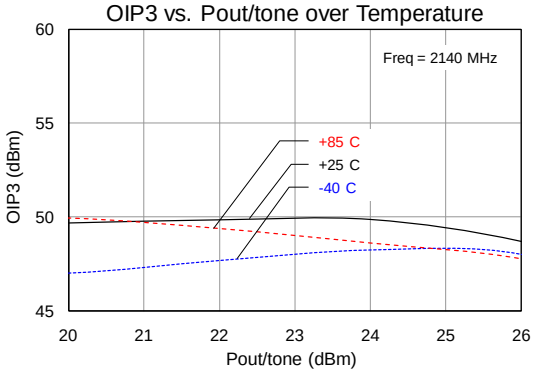
P1dB vs. Frequency over Temperature



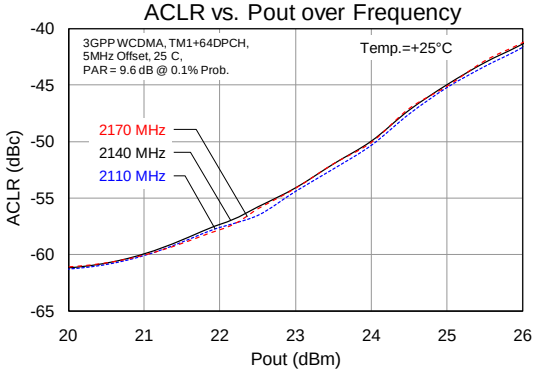
OIP3 vs. Pout/tone over Frequency



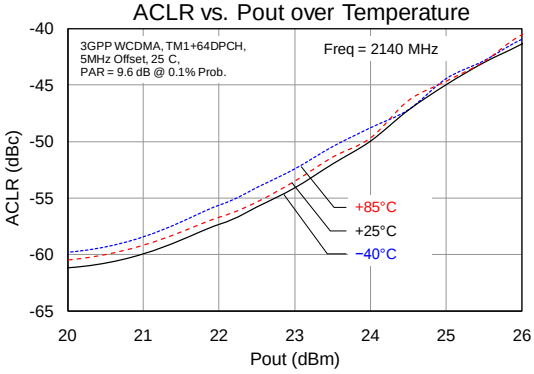
OIP3 vs. Pout/tone over Temperature



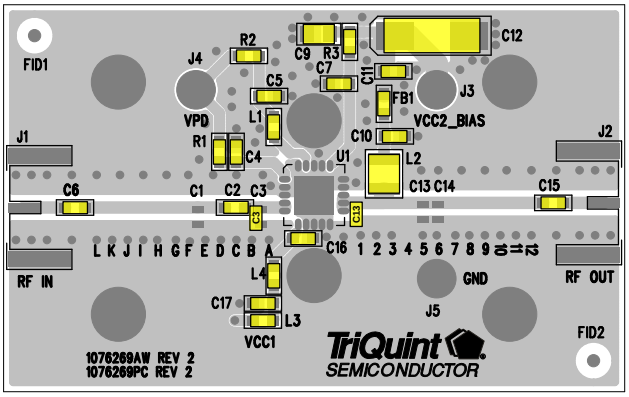
ACLR vs. Pout over Frequency

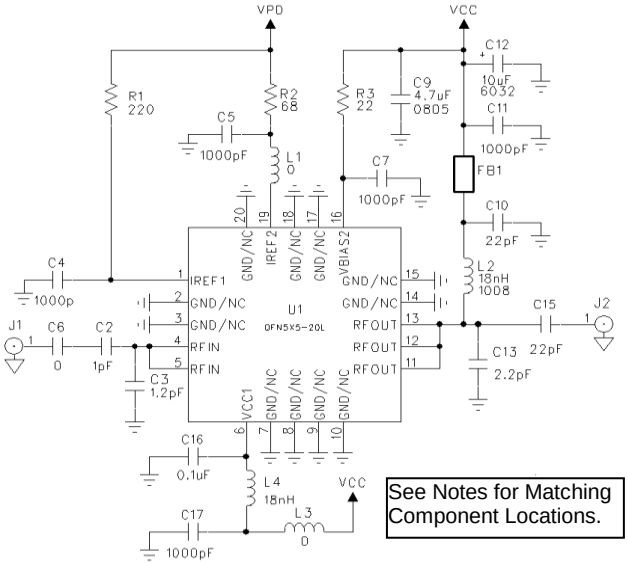


ACLR vs. Pout over Temperature



Reference Design 2500-2700 MHz





Notes:

1. See PC Board Layout, page 15 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C2 is placed at 128 mils from the U1 device package (18° @ 2650 MHz).
6. The edge of C3 is placed at 75 mils from the edge of U1 device package (10.5° @ 2650 MHz).
7. The edge of C13 is placed as close as possible to the edge of U1 device package.
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.

Typical Performance 2500-2700 MHz

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

Parameter	Conditions				Units
Frequency		2500	2600	2700	MHz
Gain		23.5	23	22	dB
Input Return Loss		9.5	15.5	21	dB
Output Return Loss		9	13	15	dB
Output P1dB		+32	+33	+33	dBm
OIP3	Pout = +24 dBm/tone, Δf = 1 MHz	+44	+44.5	+45	dBm
WCDMA Channel Power [1]	ACLR = -50 dBc	+22.5	+23.3	+23.5	dBm

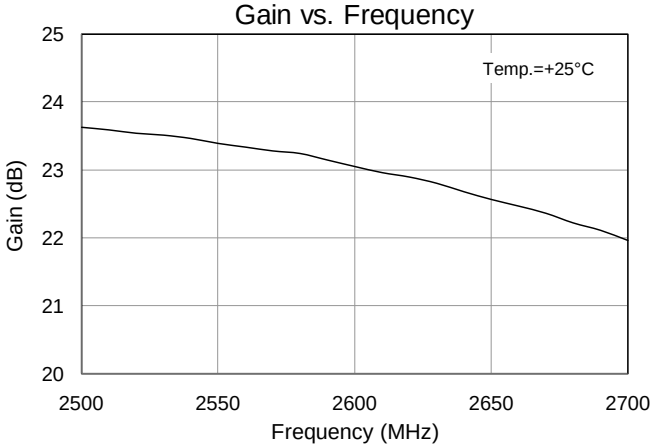
Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 10.2 dB @ 0.01% Prob.

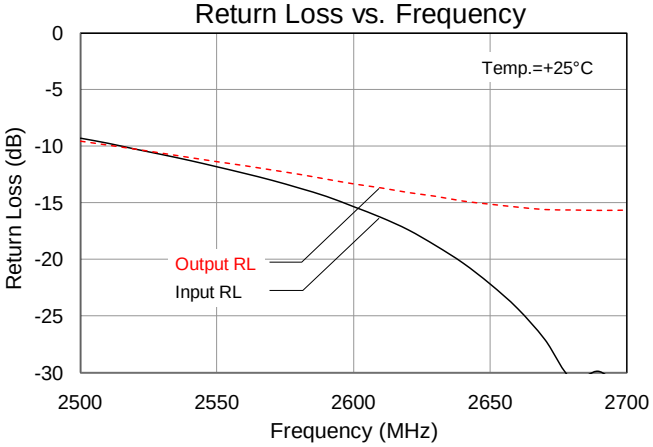
Performance Plots 2500-2700 MHz

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, Temp= +25°C, I_{CQ}=700 mA (typ.)

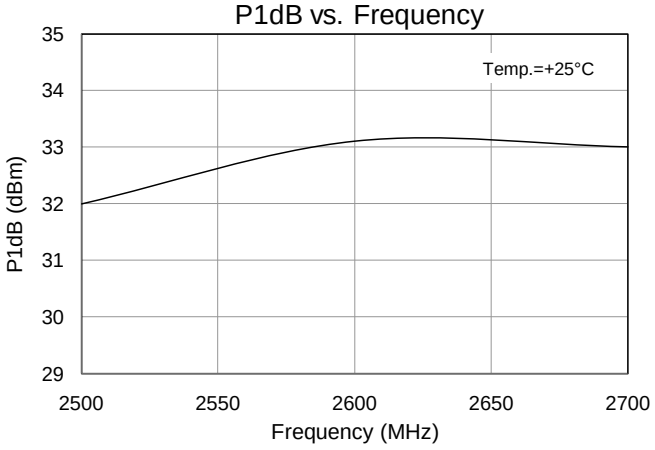
Gain vs. Frequency



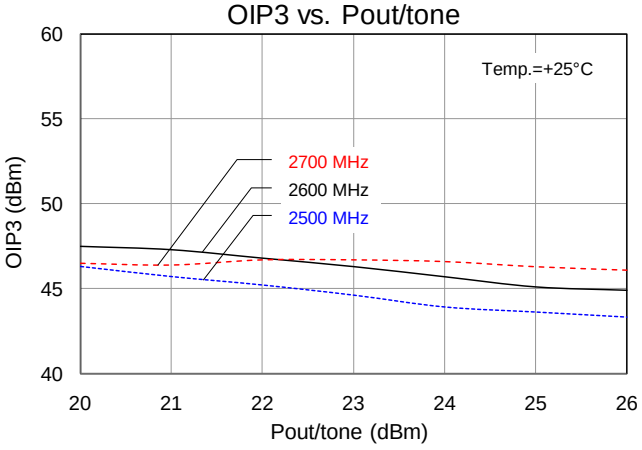
Return Loss vs. Frequency



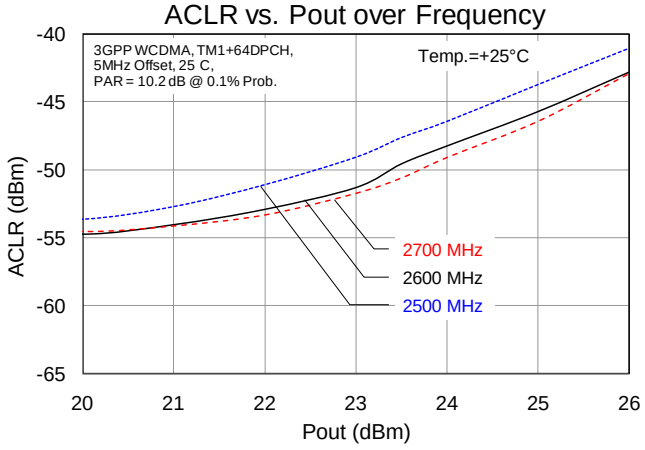
P1dB vs. Frequency



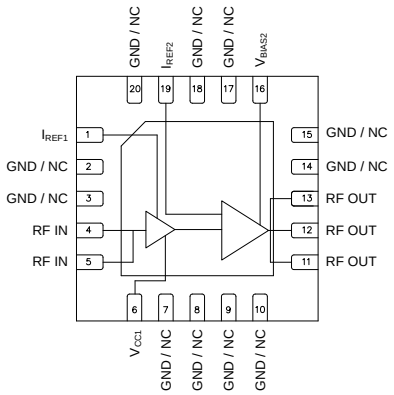
OIP3 vs. Pout/tone



ACLR vs. Pout over Frequency



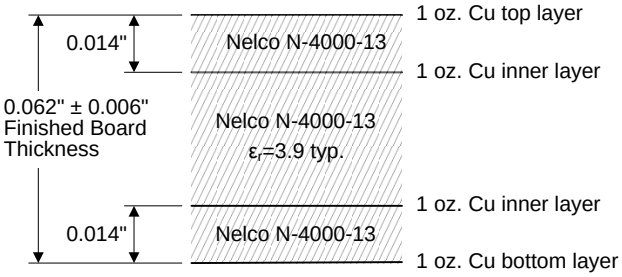
Pin Configuration and Description

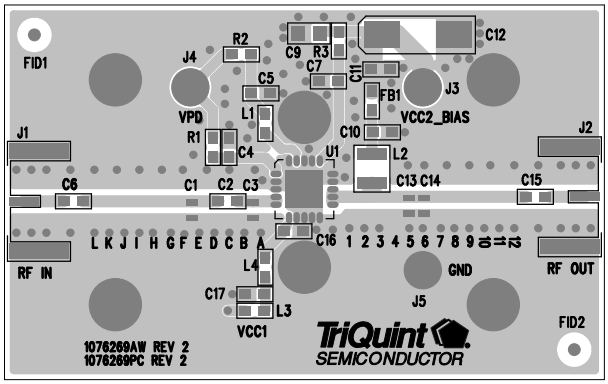


Pin No.	Label	Description
1	I_{REF1}	Reference current into internal active bias current mirror. Current into Iref sets device quiescent current for first stage. It can be used as on/off control. Iref1 current is set by providing +5Vpd through dropping resistor on EVB.
4,5	RF In	Input, requires matching for operation.
6	V_{CC1}	Supply voltage for first stage amplifier. RF Choke is needed.
11,12,13	RF Out / V_{CC2}	Output, requires matching for operation. Supply voltage for 2nd stage amplifier. RF Choke is needed.
16	V_{BIAS2}	Voltage supply for active bias for second stage. Bypass cap is recommended.
19	I_{REF2}	Reference current into internal active bias current mirror. Current into Iref sets device quiescent current for 2nd stage. It can be used as on/off control. Iref2 current is set by providing +5Vpd through dropping resistor on EVB.
2,3,7,8,9,10,14,15,17, 18,20	N/C or GND	No internal connection. This pin can be grounded or N/C on PCB.
Backside Paddle	RF / DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern.

Evaluation Board PCB Information

TriQuint PCB 1076269 Material and Stack-up

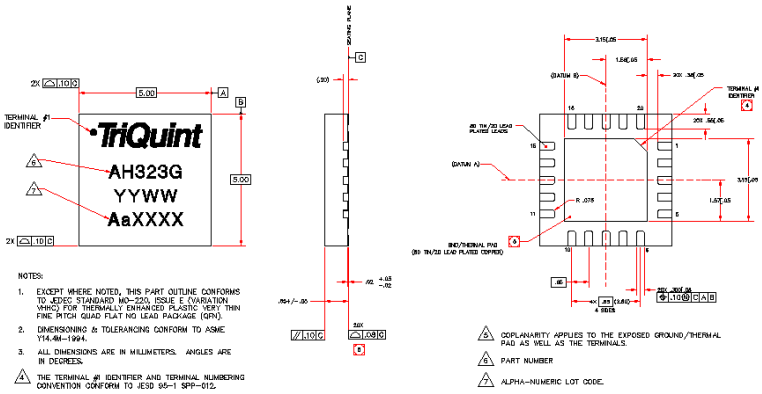




Mechanical Information

Package Marking and Dimensions

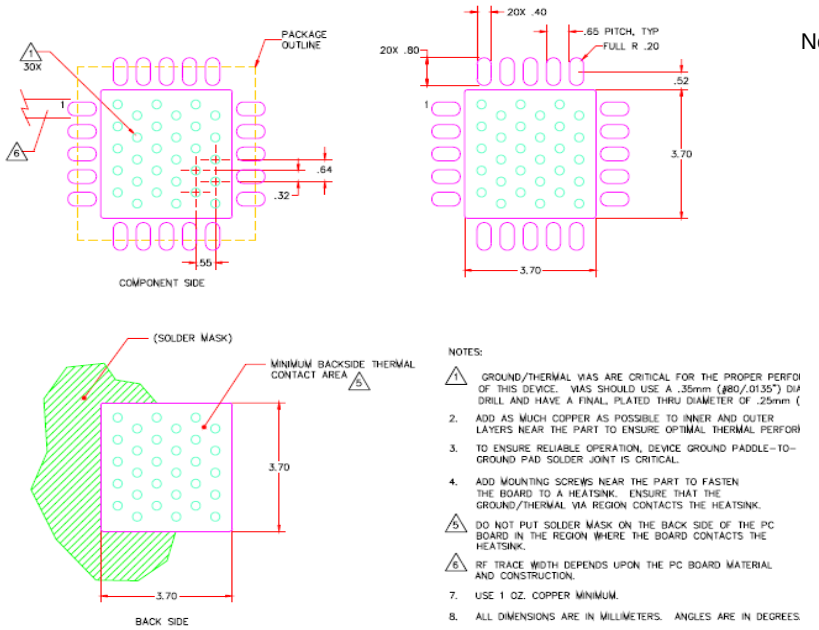
Marking: Part number –AH323G
Year/week/country code - YYWW
Lot code – AaXXXX



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. A heatsink underneath the area of the PCB for the mounted device is required for proper thermal operation.
4. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
5. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1C
Value: Passes ≥ 1000 V to < 2000 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 2000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

Contact plating: Annealed Matte Tin over Copper

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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Email: info-sales@triquint.com **Fax:** +1.503.615.8902

For technical questions and application information: **Email:** sjcapplications.engineering@triquint.com

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