5.5-9GHz Medium Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

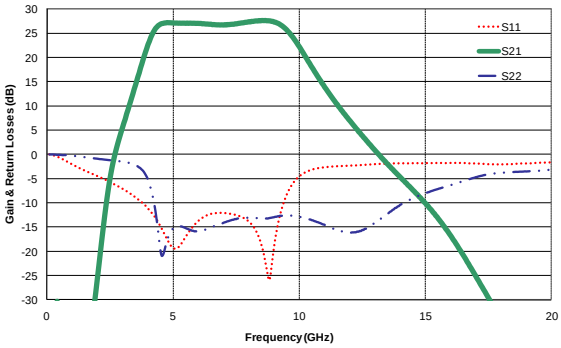
Description

The CHA5250-QDG is a three stages monolithic GaAs medium power circuit, close to 1 Watt output power.
It is designed for commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.5µm gate length.

Main Features

- Broadband performances: 5.5-9GHz
- 26dB Linear Gain
- 28dBm output power @1dB comp.
- 36dBm output TOI
- 30% PAE@1dB compression
- DC bias: Vd=7Volt@Id=280mA
- 24L-QFN4x4

Gain & RLoss



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.5		9.0	GHz
Gain	Linear Gain		26.0		dB
OTOI	Output TOI		36.0		dBm
Pout	Output Power @1dB comp.		28.0		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +7.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.5		9	GHz
Gain	Linear Gain		26		dB
RL_in	Input Return Loss		-12		dB
RL_out	Output Return Loss		-10		dB
OP1dB	Output power @1dB compression		28		dBm
Psat	Saturated output power		30		dBm
OIP3	Output IP3		36		dBm
PAE	Power Added Efficiency @ 1dB compression		30		%
NF	Noise figure		7		dB
Idq	Quiescent Drain current		280		mA
Vg	Gate voltage		-0.45		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	7.5V	V
Idq	Drain bias quiescent current	0.4	A
Vg	Gate bias voltage	-2 to +0	V
Pin	Input continuous power	8	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VD1	12	DC Drain voltage 1st stage	7	V
VD2	9	DC Drain voltage 2nd stage	7	V
VD3	7	DC Drain voltage 3rd stage	7	V
VG	22	DC Gate voltage tuned for Idq= 280mA	-0.45	V

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

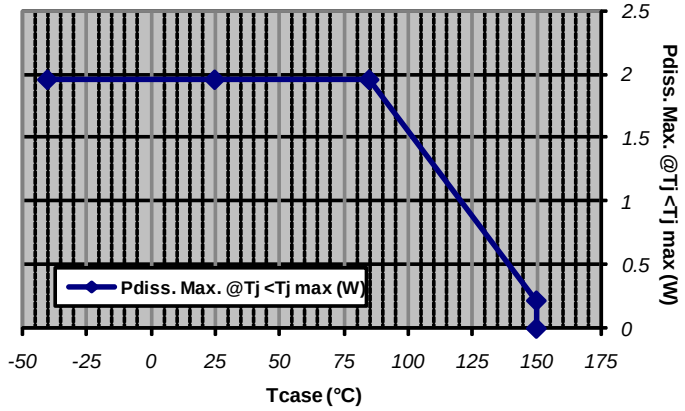
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

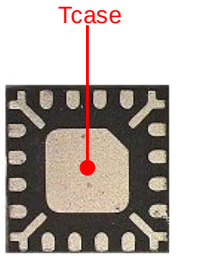
DEVICE THERMAL SPECIFICATION : CHA5250-QDG			
Recommended max. junction temperature (Tj max)	:	158	°C
Junction temperature absolute maximum rating	:	175	°C
Max. continuous dissipated power (Pdiss. Max.)	:	2.0	W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	27	mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<37	°C/W
Minimum Tcase operating temperature(3)	:	-40	°C
Maximum Tcase operating temperature(3)	:	85	°C
Minimum storage temperature	:	-55	°C
Maximum storage temperature	:	150	°C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temeprature reference point (Tcase) on package's bottom side

6.4

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Typical Package Sij parameters

Tamb.= +25°C, Vd = +7.0V, Idq = 280mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
2	-4.1	-153.5	-26.3	115.3	-76.2	147.1	-0.3	-77.1
2.5	-5.3	-175.6	-5.1	68.1	-75.5	138.7	-0.5	-98.6
3	-6.5	166.1	5.5	-11.9	-75.0	105.5	-1.0	-122.7
3.5	-8.1	150.2	13.7	-75.1	-69.7	100.4	-1.8	-151.9
4	-10.2	137.4	21.9	-149.1	-68.9	77.5	-4.5	168.5
4.5	-13.1	130.5	26.2	119.1	-71.0	87.0	-14.2	143.1
5	-16.3	138.6	26.6	41.8	-68.5	85.2	-18.2	-178.5
5.5	-16.7	160.9	26.4	-20.4	-63.4	60.0	-20.7	-167.4
6	-14.3	169.7	26.3	-76.4	-64.5	77.8	-21.3	-121.7
6.5	-12.3	164.8	26.2	-128.8	-64.6	57.5	-16.0	-111.2
7	-11.3	153.4	26.2	-179.1	-63.2	47.9	-12.8	-120.1
7.5	-11.3	138.8	26.4	131.2	-62.6	33.7	-11.0	-133.9
8	-12.6	120.5	26.6	80.5	-61.5	20.4	-10.0	-147.8
8.5	-18.2	91.7	26.9	27.5	-61.6	2.3	-9.7	-159.8
9	-19.2	-74.4	26.9	-31.0	-63.6	-28.1	-9.5	-170.3
9.5	-7.6	-124.4	25.7	-96.1	-64.1	-68.8	-9.4	176.4
10	-3.7	-158.7	22.4	-157.7	-70.4	-139.9	-10.2	162.8
10.5	-2.3	176.0	18.2	150.8	-72.0	-162.9	-11.4	153.8
11	-1.7	157.8	14.1	107.3	-68.3	132.4	-12.8	148.0
11.5	-1.3	143.3	10.3	68.7	-63.3	107.0	-14.5	145.9
12	-1.2	131.0	6.8	32.9	-65.0	95.9	-16.1	148.4
12.5	-1.0	120.0	3.7	-1.4	-64.2	82.5	-17.8	159.3
13	-0.9	109.5	0.8	-35.2	-63.2	115.2	-17.9	-179.4
13.5	-0.8	99.4	-1.8	-68.8	-56.6	79.6	-15.3	-164.4
14	-0.7	89.6	-4.4	-102.9	-57.5	61.0	-12.4	-163.5
14.5	-0.6	79.9	-6.8	-138.2	-60.4	55.5	-9.9	-168.9
15	-0.6	70.1	-9.3	-175.6	-57.3	54.7	-7.9	-177.9
15.5	-0.6	60.7	-12.1	145.2	-57.4	48.0	-6.3	171.2
16	-0.5	51.1	-15.3	104.2	-53.7	43.8	-5.2	159.0
16.5	-0.5	41.7	-19.2	64.3	-54.9	32.2	-4.3	146.0
17	-0.5	32.3	-23.5	27.0	-51.0	7.1	-3.6	133.0
17.5	-0.4	23.0	-28.3	-7.2	-53.7	-47.7	-3.1	119.8
18	-0.4	14.0	-33.3	-36.3	-61.7	-53.4	-2.7	106.9
18.5	-0.3	5.2	-38.4	-60.8	-69.3	-20.6	-2.3	93.4
19	-0.3	-3.5	-43.4	-82.2	-64.5	2.7	-2.0	79.7
19.5	-0.3	-11.6	-47.5	-105.2	-67.3	-114.2	-1.8	66.3
20	-0.2	-19.5	-53.3	-128.8	-69.8	49.6	-1.5	53.2

The Sij measurement calibration planes are defined in the paragraph “Definition of the Sij reference planes”.

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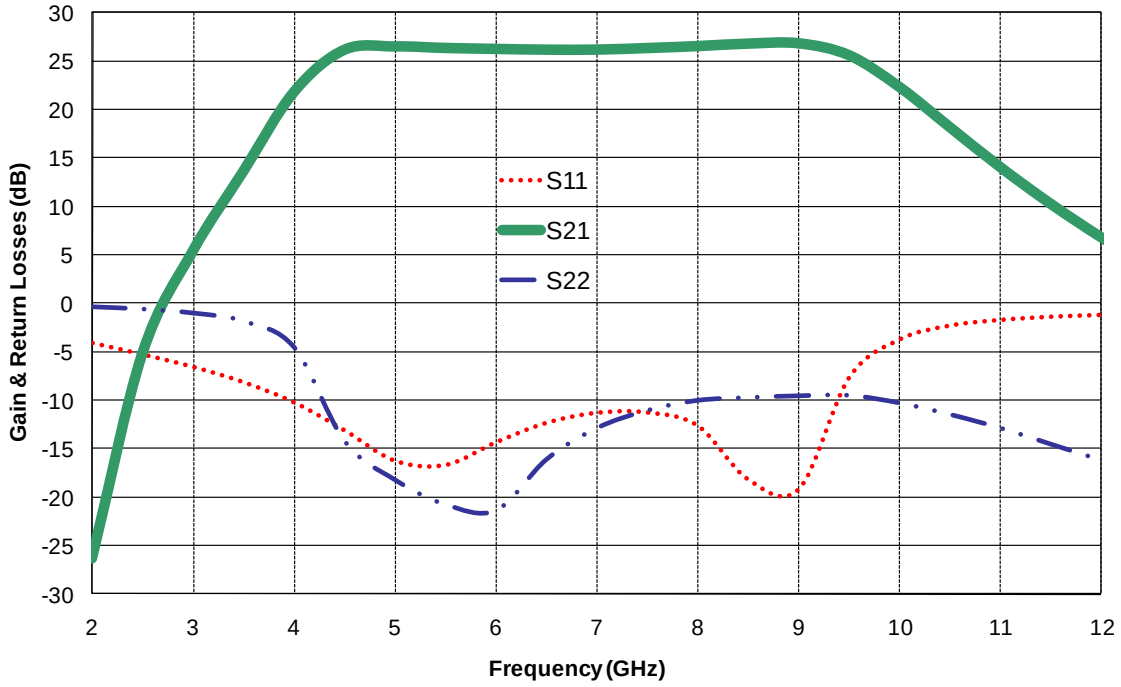
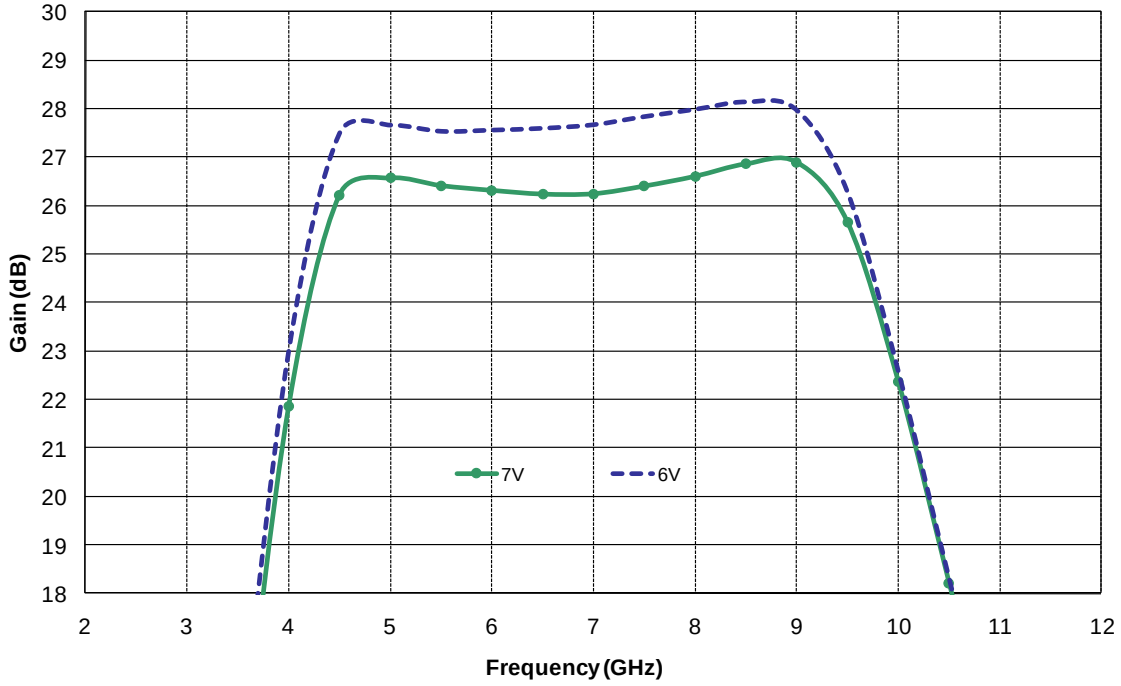
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Idq = 280mA
Measurement in the QFN planes as defined in paragraph “Definition of the Sij reference planes”

Linear Gain & Return Loss



Linear Gain versus Drain voltage



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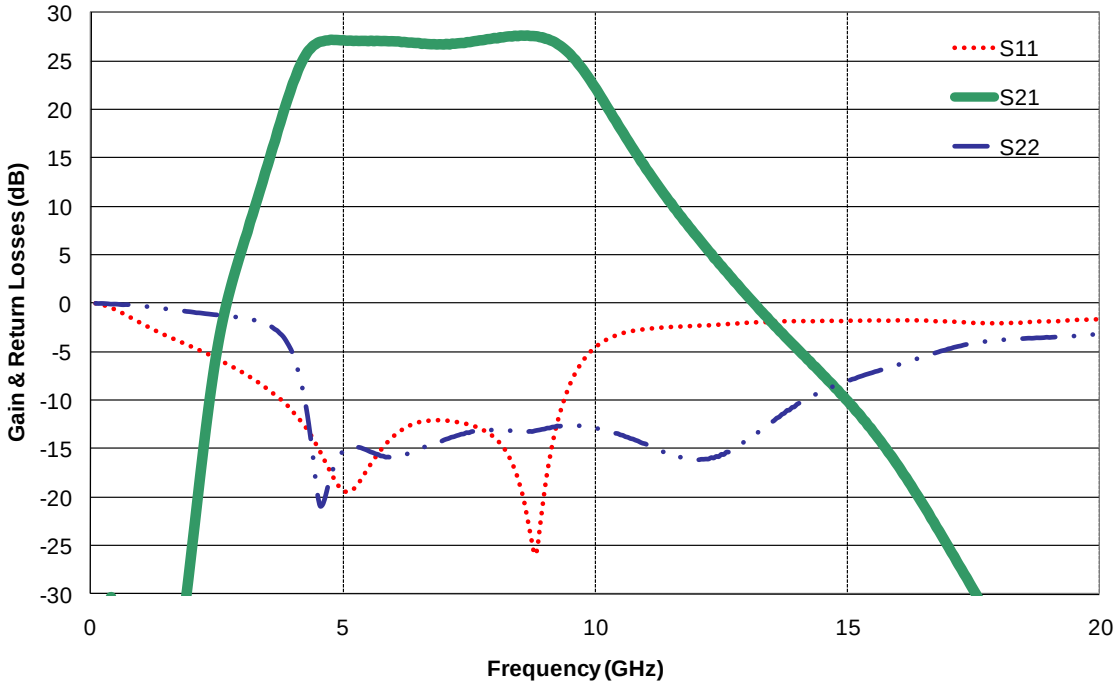
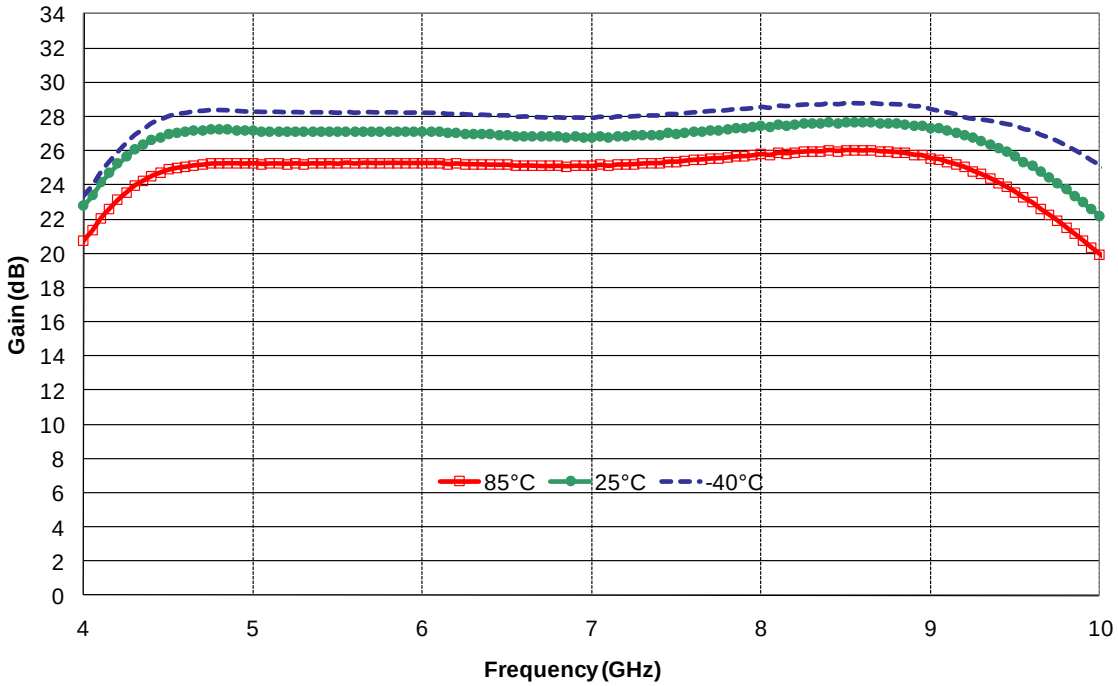
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Idq = 280mA
Measurement in the plan of the connectors, using the proposed land pattern & board, as defined in paragraph “Evaluation mother board”

Linear Gain & Return Loss



Linear Gain versus temperature



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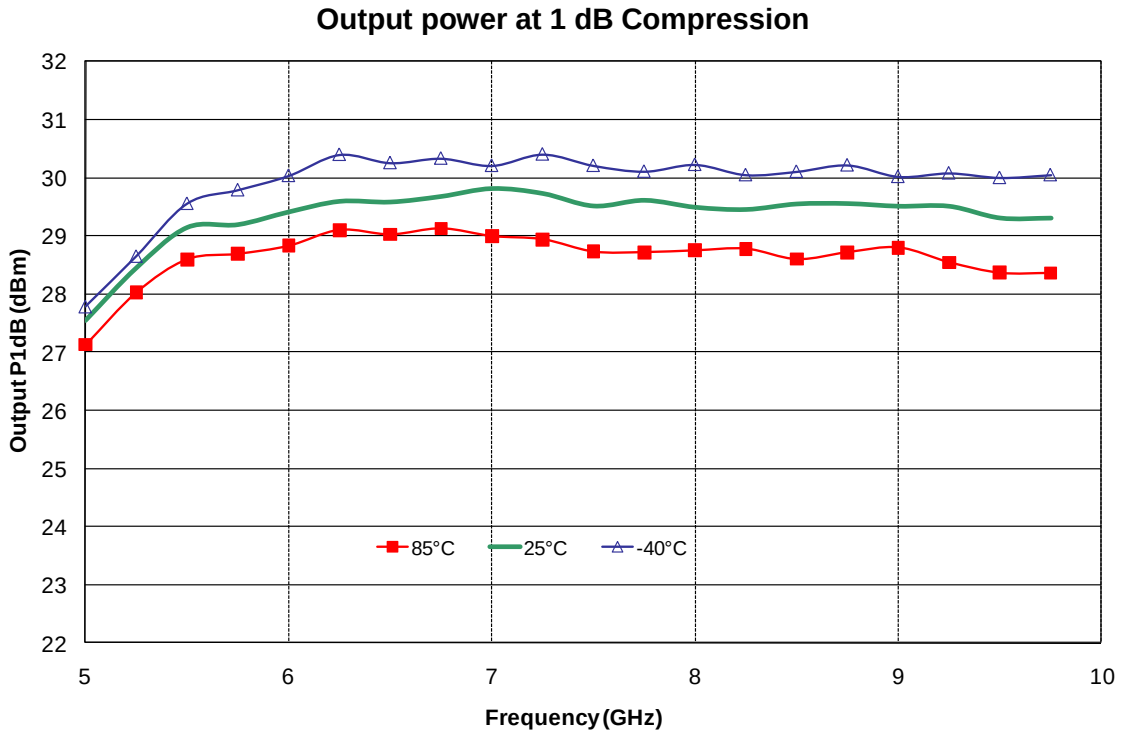
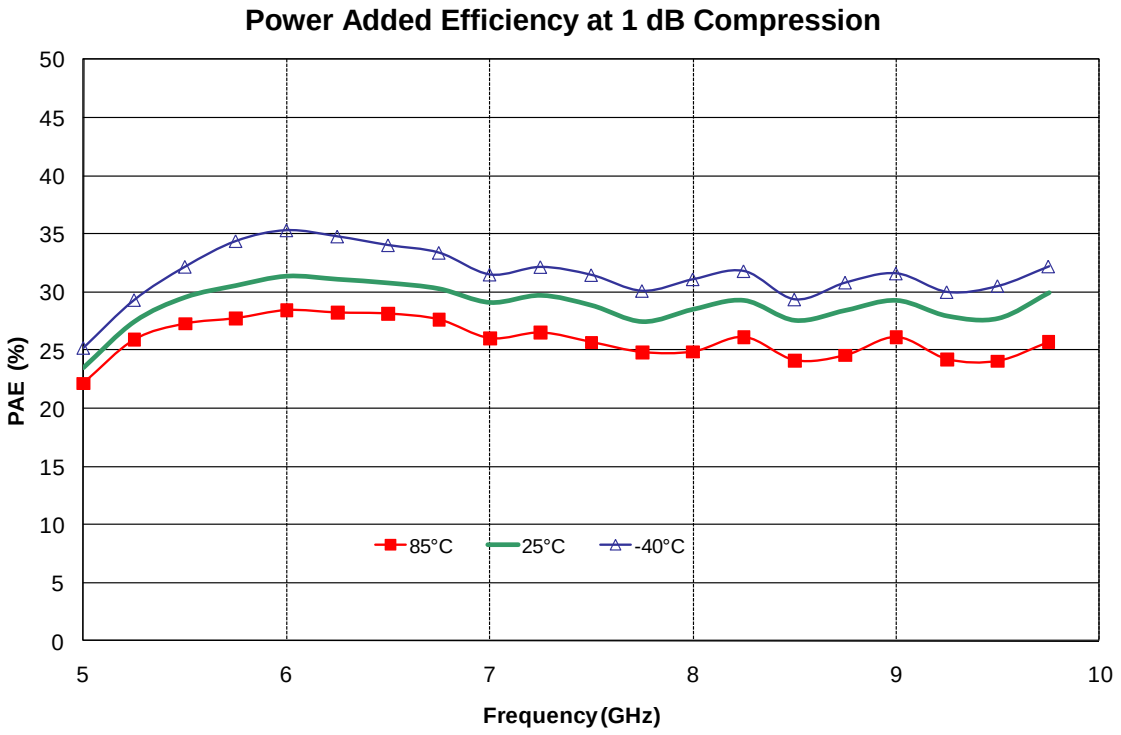
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Idq = 280mA





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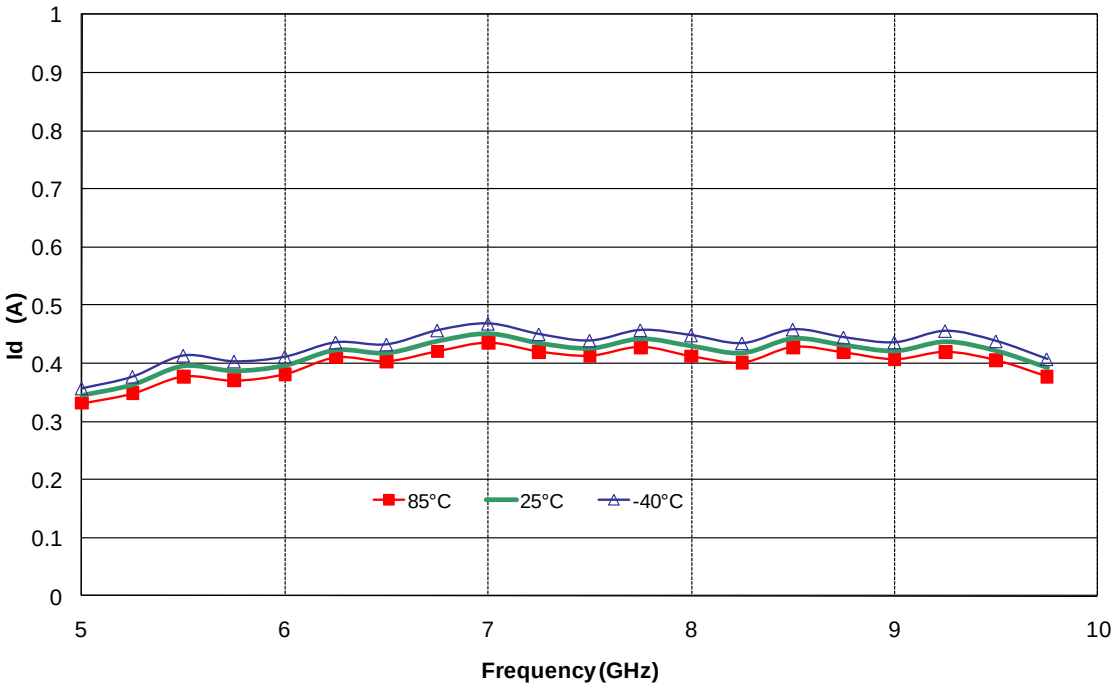
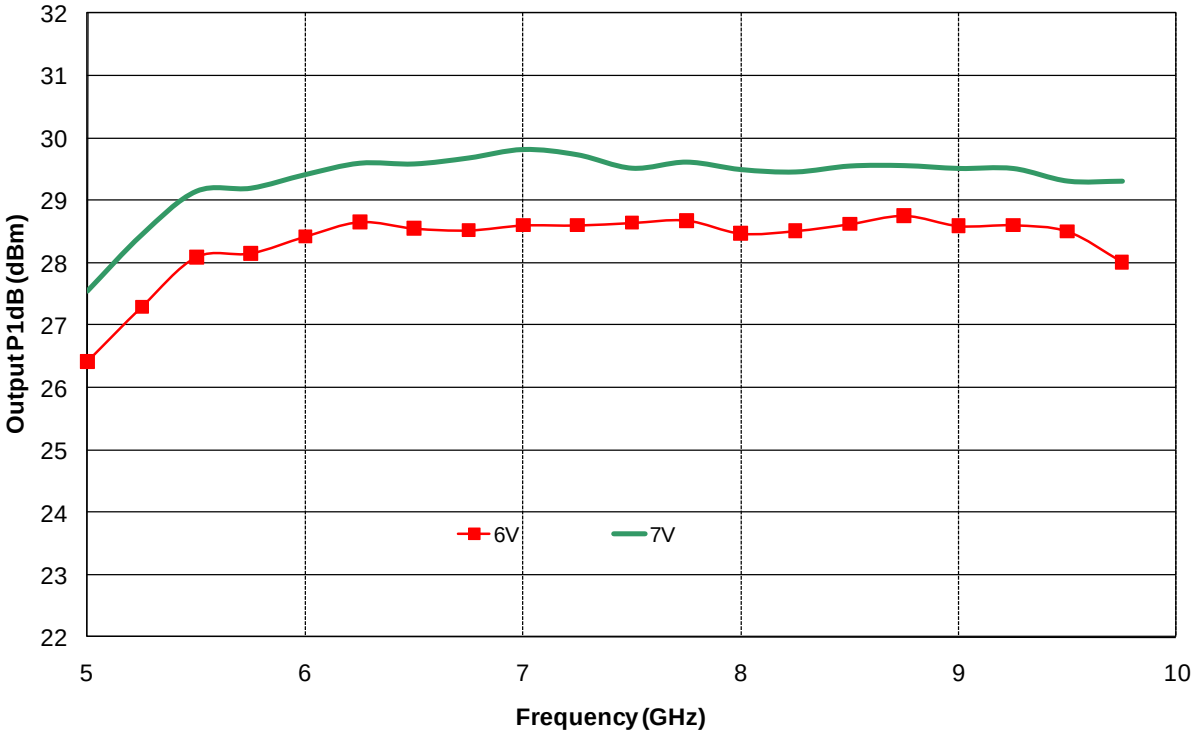
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Idq = 280mA

Drain current at 1 dB Compression



Output power at 1 dB Compression versus Vd



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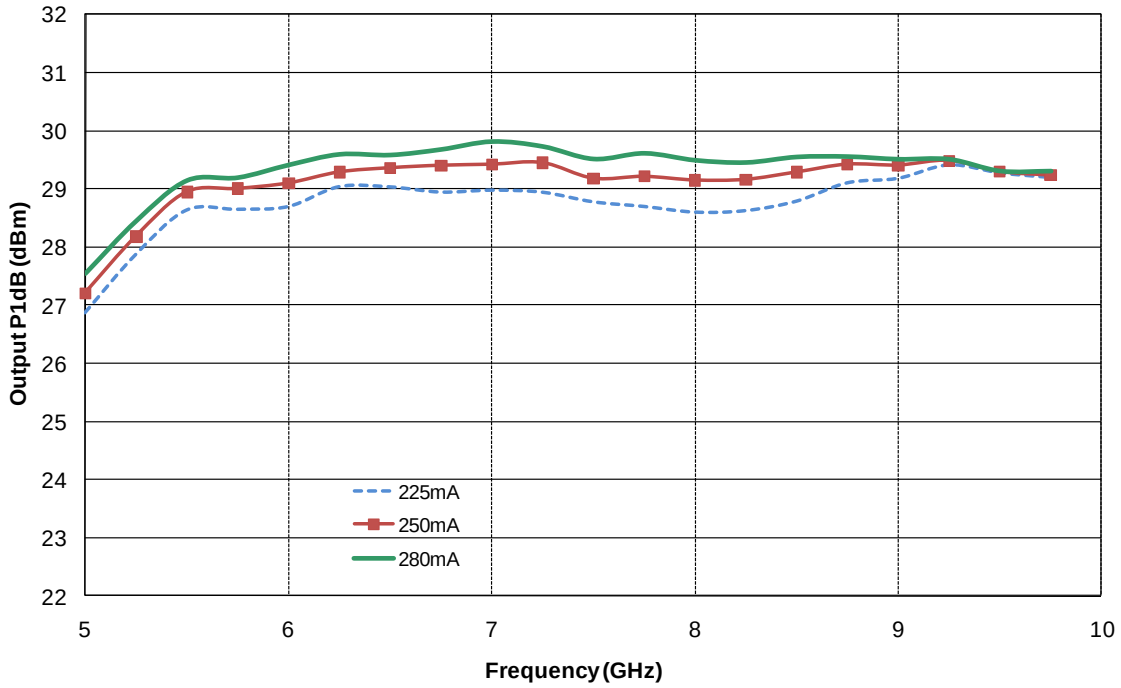
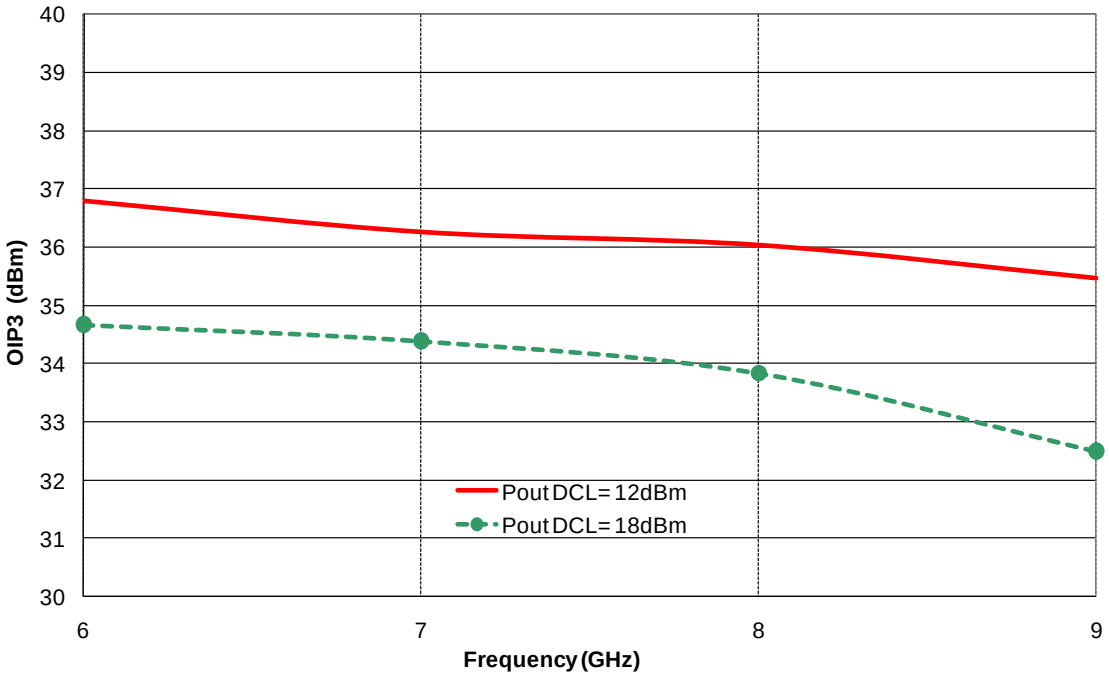
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Idq = 280mA

Output power at 1 dB Compression versus Idq



Output TOI (dBm) at two Pout



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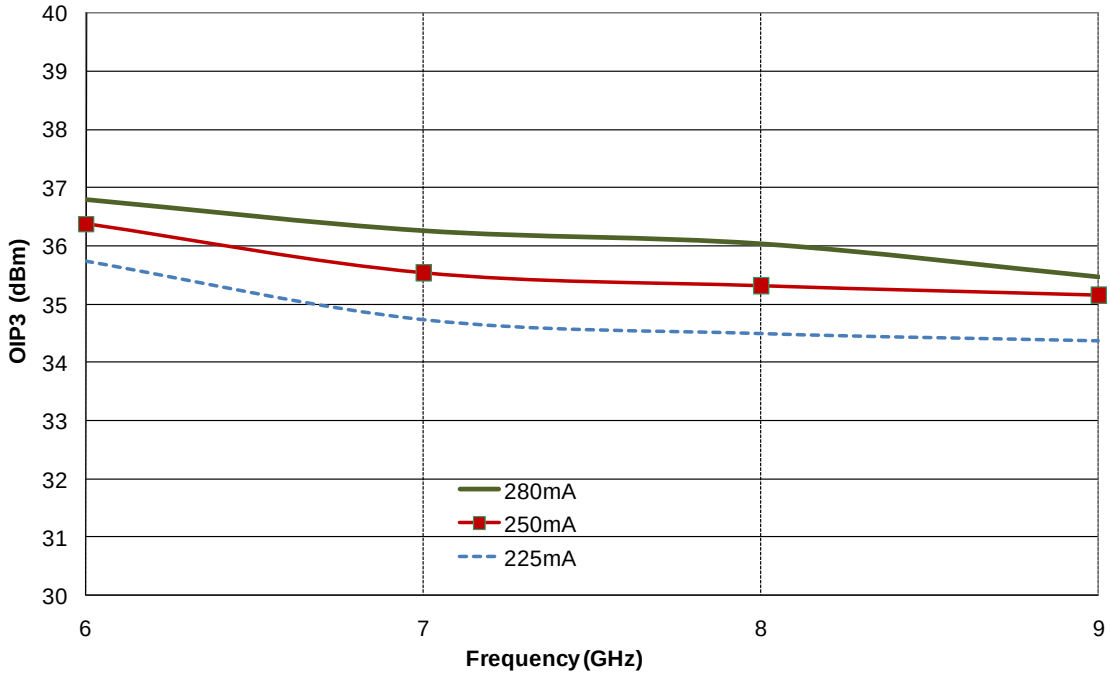
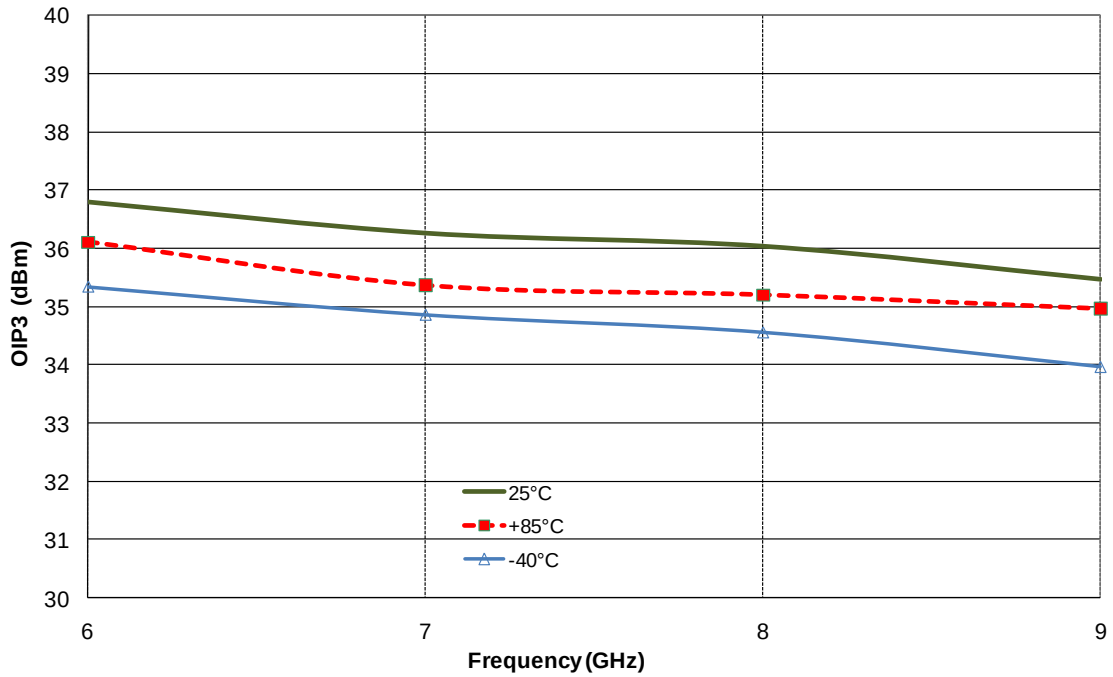
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Idq = 280mA

Output TOI (dBm) versus Idq at Pout=12dBm



Output TOI (dBm) versus temperature at Pout=12dBm



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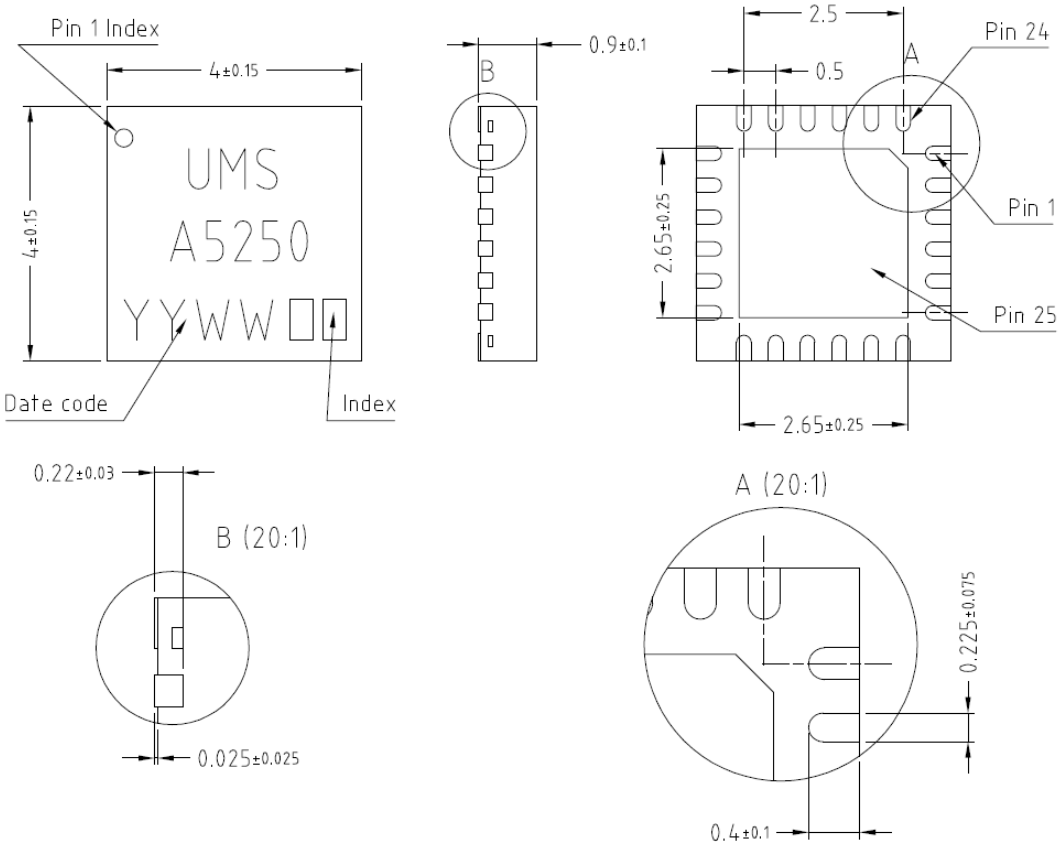
Package outline (1)



Matt tin, Lead Free	(Green)	1- Gnd(2)	9- Vd2	17- Gnd(2)
Units :	mm	2- Gnd(2)	10- Nc	18- Gnd(2)
From the standard :	JEDEC MO-220	3- Gnd(2)	11- Nc	19- Nc
	(VGGD)	4- RF out	12- Vd1	20- Nc
25-	GND	5- Gnd(2)	13- Gnd(2)	21- Nc
		6- Gnd(2)	14- Gnd(2)	22- Vg
		7- Vd3	15- RF in	23- Nc
		8- Nc	16- Gnd(2)	24- Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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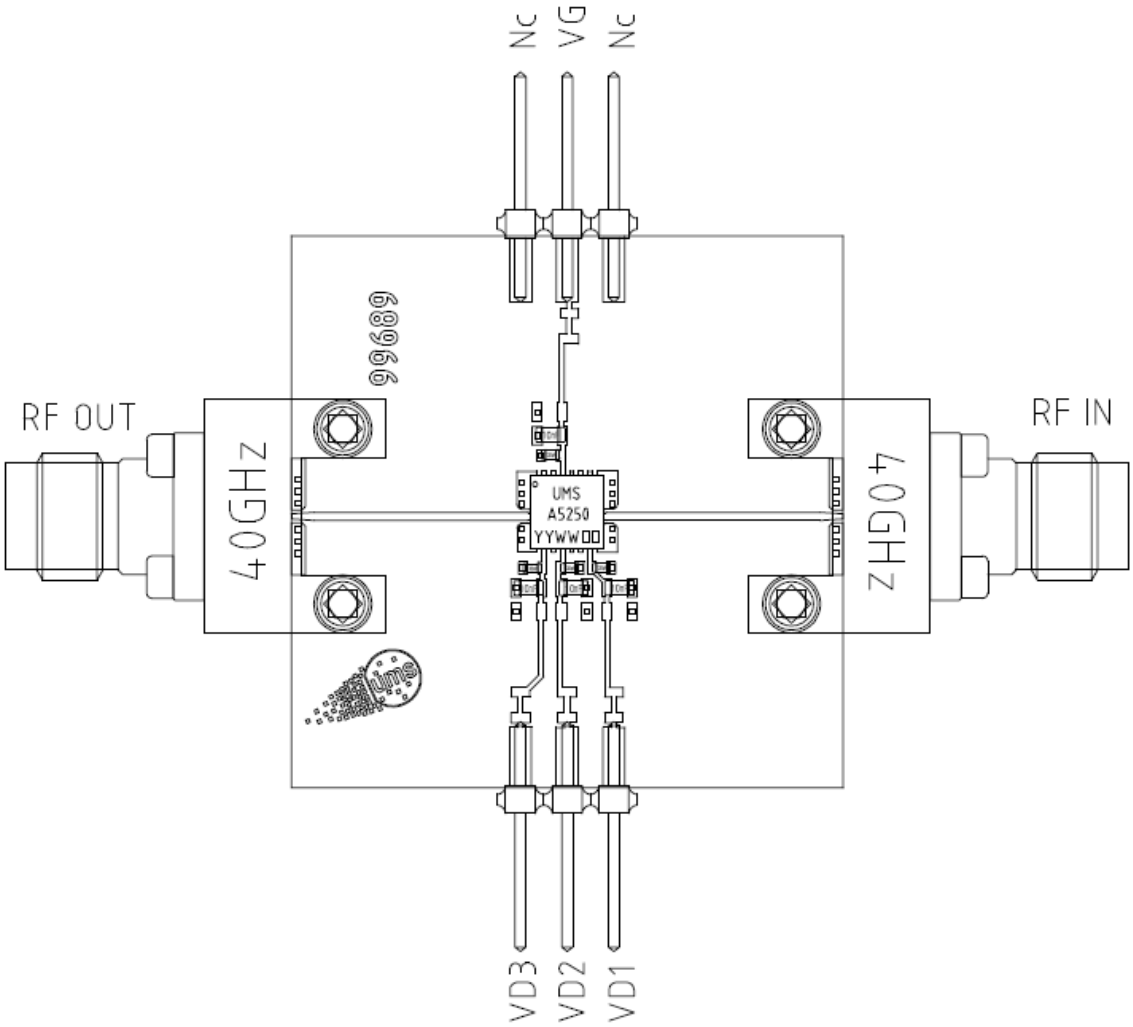
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- First decoupling network is done with 100pF capacitors, second decoupling network is done with 10nF capacitors.
- See application note AN0017 for details.



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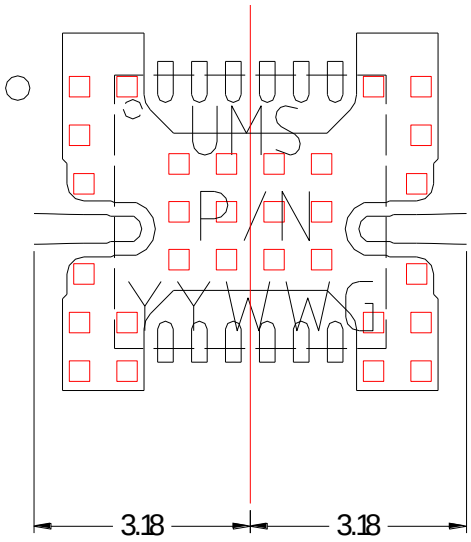
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



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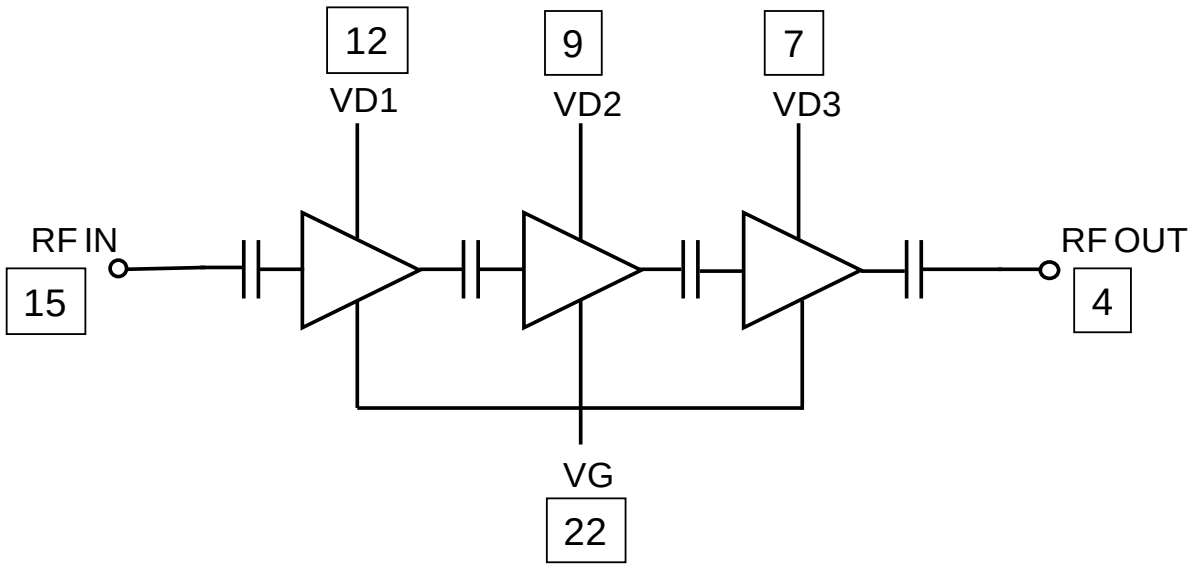
Notes



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF & 10nF) on the PC board, as close as possible to the package.

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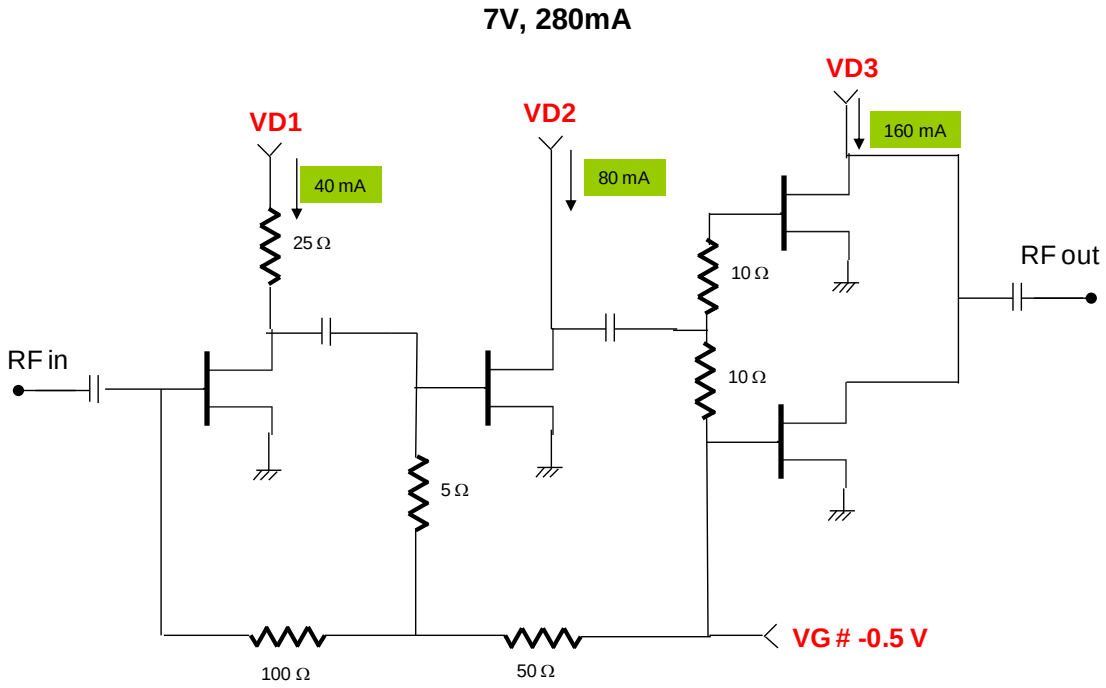
DC Schematic



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 RoHS compliant package:	CHA5250-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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