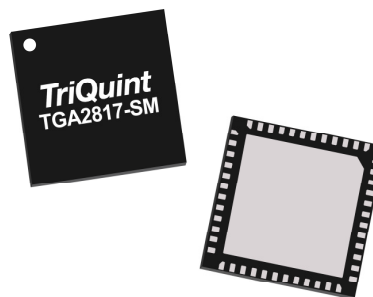


Applications

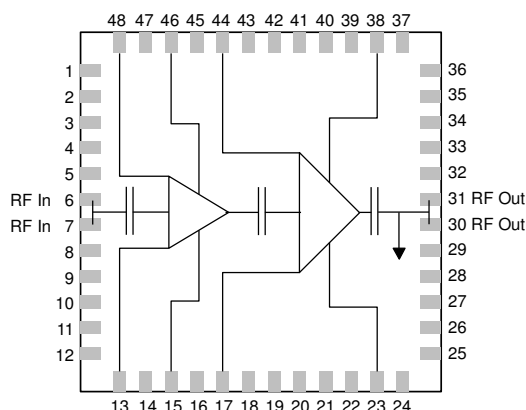
- Military Radar
- Commercial Radar



Product Features

- Frequency Range: 2.9 – 3.5 GHz
- Pout: > 48 dBm (at Pin = 24 dBm)
- Large Signal Gain: > 24 dB (at Pin = 24 dBm)
- PAE: > 54 % (at Pin = 24 dBm)
- Bias: $V_D = 28$ V, $I_{DQ} = 200$ mA, $V_G = -2.8$ V (Typ)
- Package Dimensions: 7.00 x 7.00 x 0.85 mm

Functional Block Diagram



General Description

TriQuint's TGA2817-SM is a high-power, S-band amplifier fabricated on TriQuint's TQGaN25 0.25um GaN on SiC production process. Covering 2.9-3.5 GHz, the TGA2817-SM provides > 48 dBm of saturated output power and > 24 dB of large-signal gain while achieving > 54 % power added efficiency.

The TGA2817-SM can also support a variety of operating conditions to best support system requirements. With good thermal properties, it can support a range of bias voltages and will perform well under pulse applications. The TGA2817-SM is matched to 50 ohms with integrated DC blocking caps on both I/O ports. It is ideal for use in both commercial and military radar systems.

Lead-free and RoHS compliant.

Evaluation board available on request.

Pad Configuration

Pad Number	Symbol
6, 7	RF Input
13, 48	V_{G1}
15, 46	V_{D1}
17, 44	V_{G2}
23, 38	V_{D2}
30, 31	RF Output
1-5, 8-12, 14, 16, 18-22, 24-29, 32-37, 39-43, 45, 47, 49	GND

Ordering Information

Part	ECCN	Description
TGA2817-SM	3A001.b.2.a	S-Band 60 W GaN Power Amplifier
TGA2817-SM_EVB	EAR99	TGA2817-SM Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40 V
Drain Current (I_{D1}/I_{D2})	1.4/5.8 A
Gate Current (I_G)	See graph
Dissipated Power (P_{DISS})	92 W
Input Power: 50 Ω , 85 °C ¹	30 dBm
Input Power: 3:1 VSWR, 85 °C ¹	28 dBm
Channel Temperature, T_{CH}	275 °C
Storage Temperature	-55 to 150 °C

¹ Based on die performance

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Value
Drain Voltage	28 V
Drain Current (quiescent, I_{DQ})	200 mA
Drain Current (under drive, I_D)	4.6 A
Gate Voltage	-2.8 V
Operating Temperature	-40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions, unless otherwise noted: 25 °C, $V_D = 28$ V, $I_{DQ} = 200$ mA, Pulse Width = 100 μ s, Duty Cycle = 10%

Parameter	Min	Typical	Max	Units
Frequency	2.9		3.5	GHz
Output Power ($P_{IN} = 24$ dBm)		> 48.0		dBm
Large Signal Gain ($P_{IN} = 24$ dBm)		> 24.2		dB
Power Added Efficiency ($P_{IN} = 24$ dBm)		> 54.0		%
Input Return Loss		> 8.3		dB
Output Power Temperature Coefficient		-0.006		dBm/°C

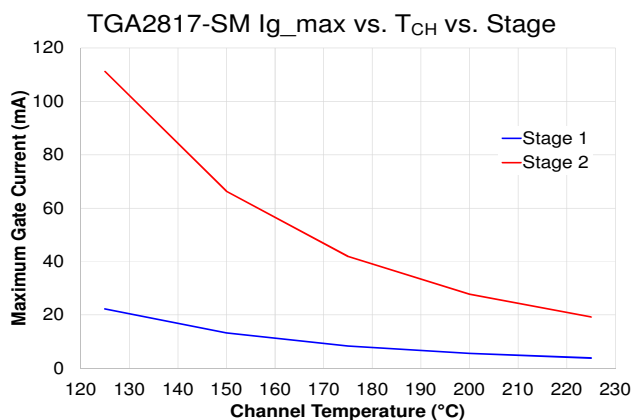
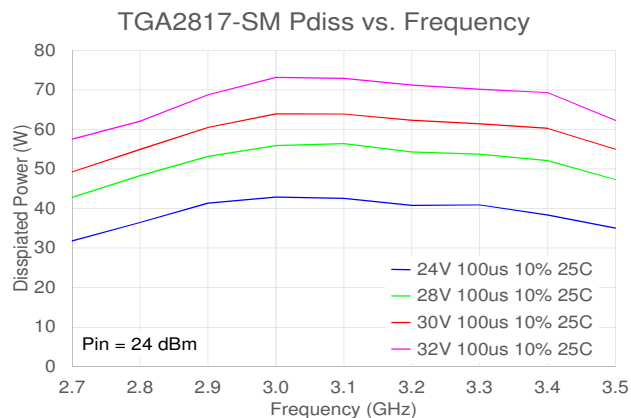
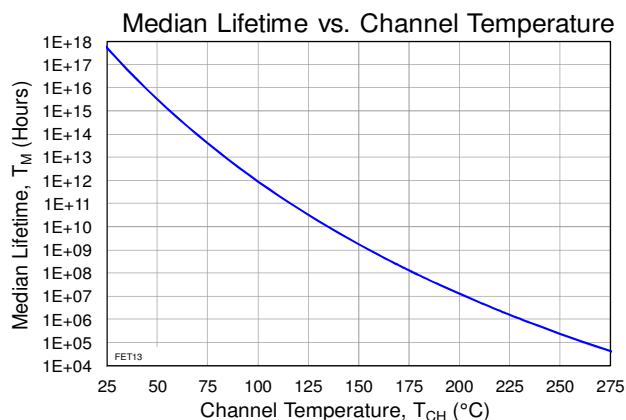
Specifications

Thermal and Reliability Information

Parameter	Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_D = 200\text{ mA}$ (quiescent DC, small signal), $P_{DISS} = 6.4\text{ W}$	1.094	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH})		92.0	$^{\circ}\text{C}$
Median Lifetime (T_M)		2.90E+12	Hrs
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_D = 4.5\text{ A}$, $P_{IN} = 24\text{ dBm}$, $P_{OUT} = 48.5\text{ dBm}$, $PW = 100\text{ us}$, DC = 10%, $P_{DISS} = 53\text{ W}$	0.698	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH})		122.0	$^{\circ}\text{C}$
Median Lifetime (T_M)		4.79E+10	Hrs
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85^{\circ}\text{C}$, $V_D = 32\text{ V}$, $I_D = 5.1\text{ A}$, $P_{IN} = 24\text{ dBm}$, $P_{OUT} = 49.4\text{ dBm}$, $PW = 100\text{ us}$, DC = 10%, $P_{DISS} = 74\text{ W}$	0.716	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH})		138.0	$^{\circ}\text{C}$
Median Lifetime (T_M)		6.85E+09	Hrs

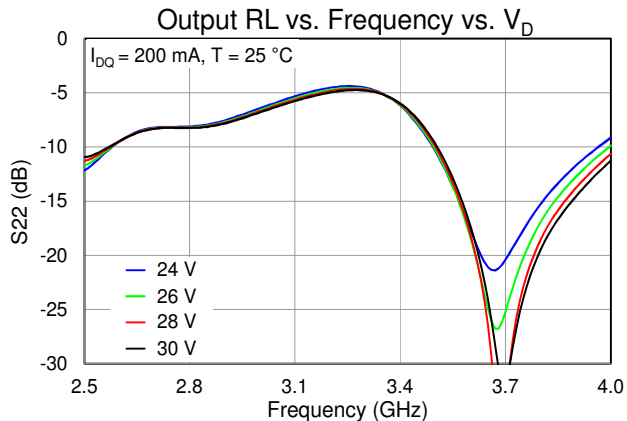
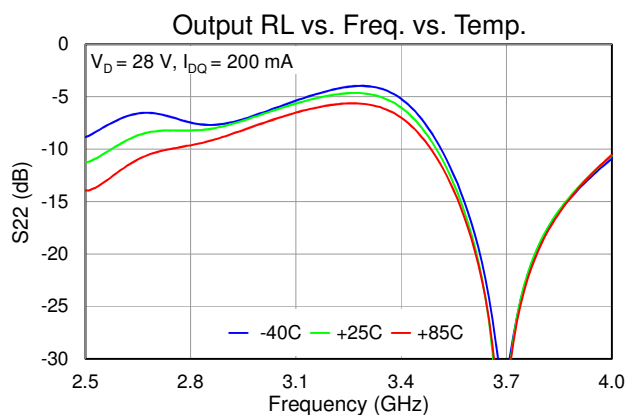
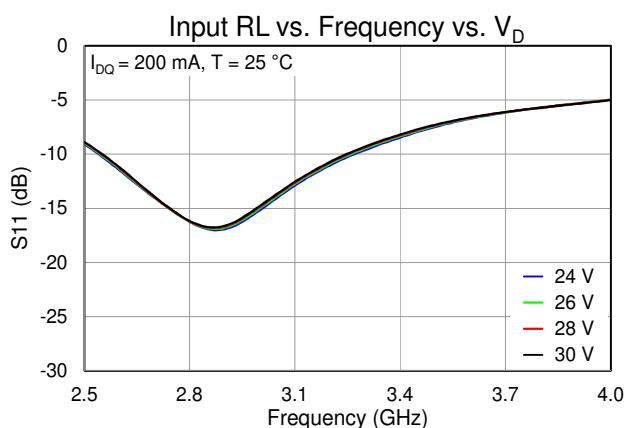
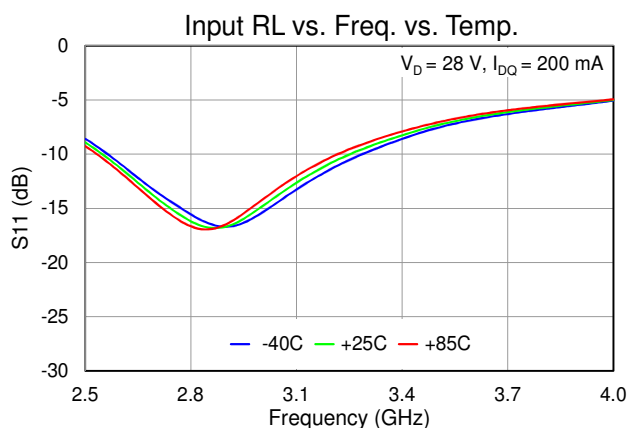
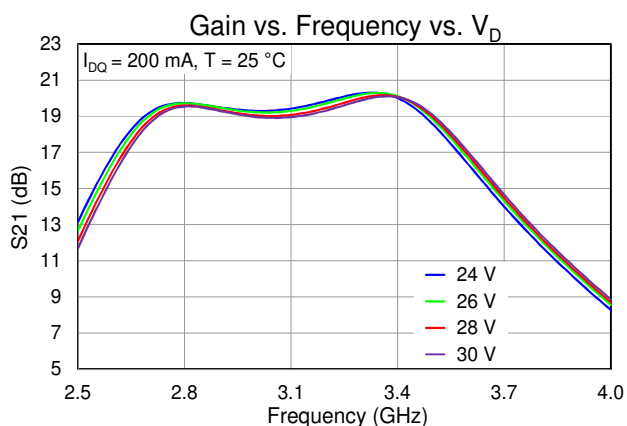
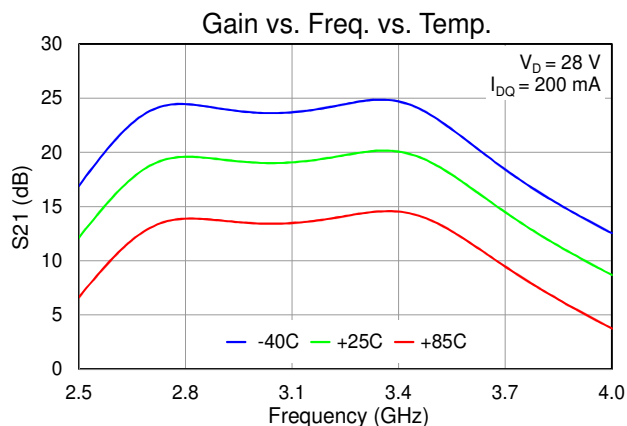
Median Lifetime

Test Conditions: 40 V
Failure Criterion = 10% reduction in $I_{D\text{ MAX}}$



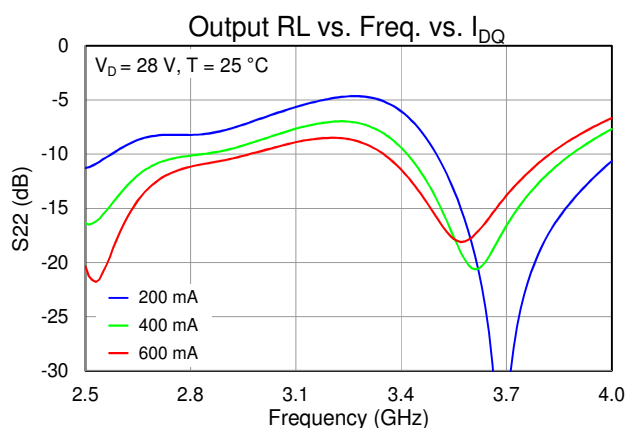
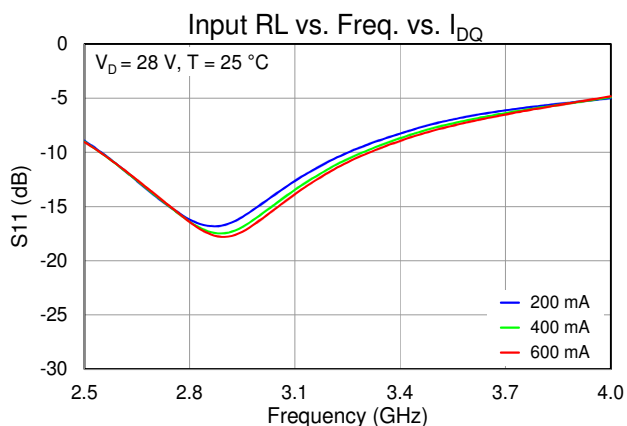
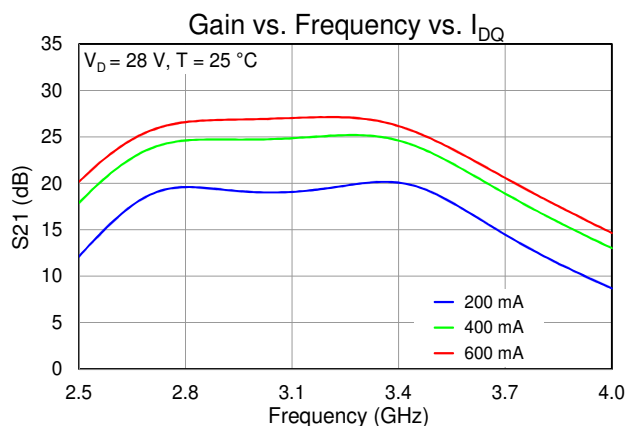
Typical Performance

Test conditions unless otherwise noted: Temp. = 25 °C



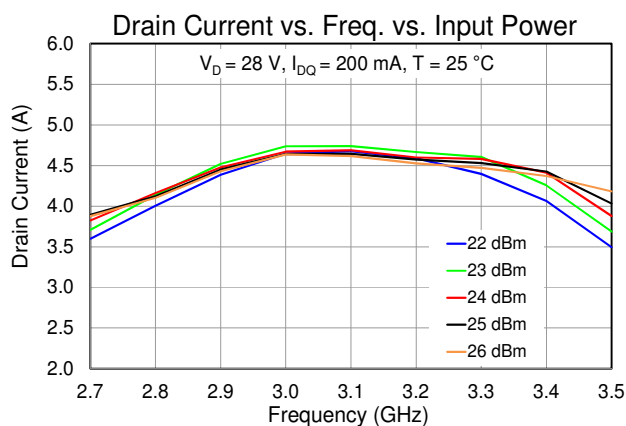
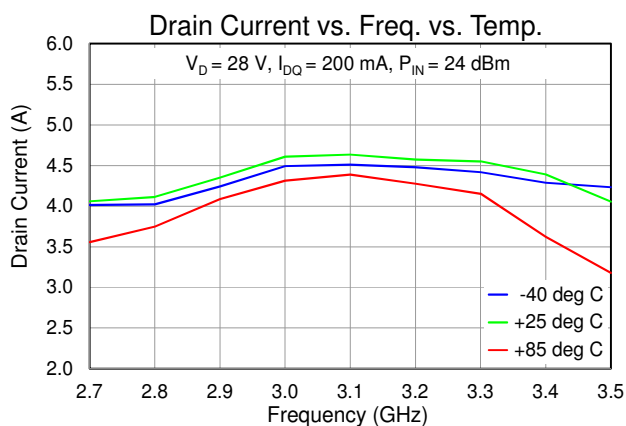
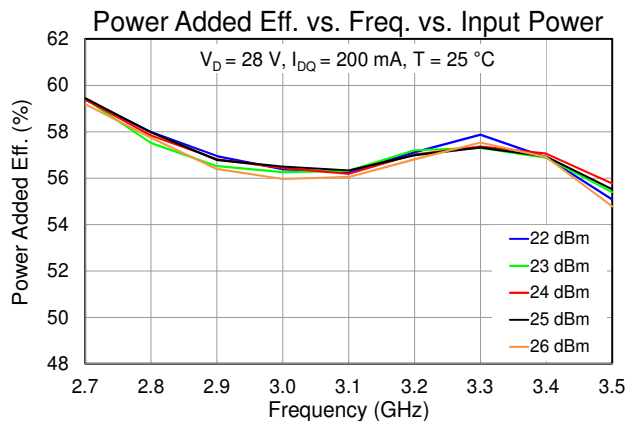
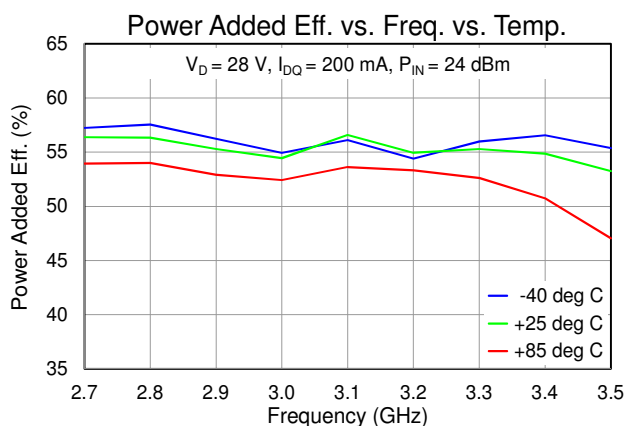
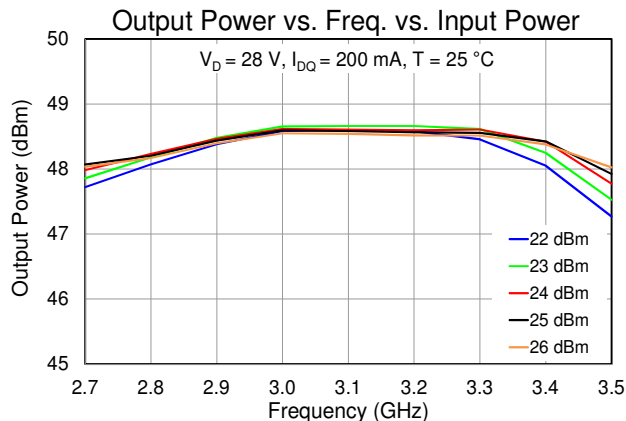
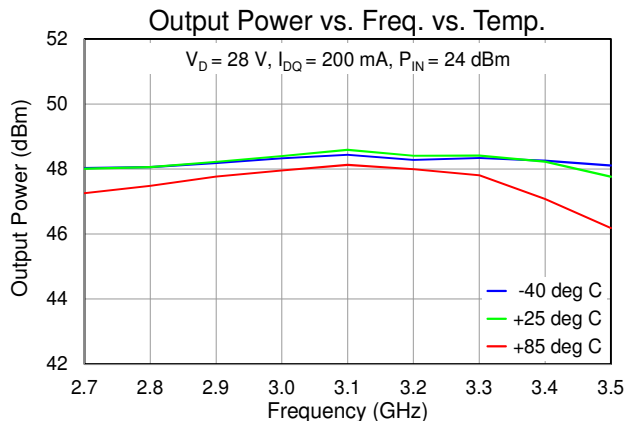
Typical Performance

Test conditions unless otherwise noted: Temp. = 25 °C



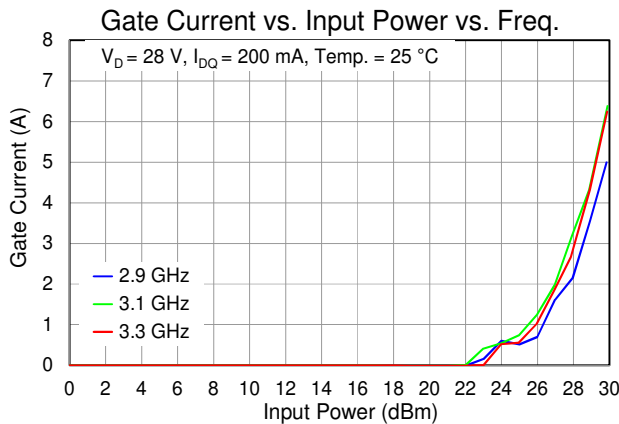
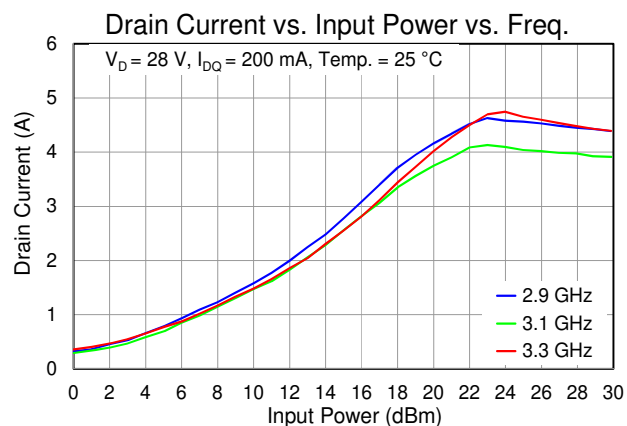
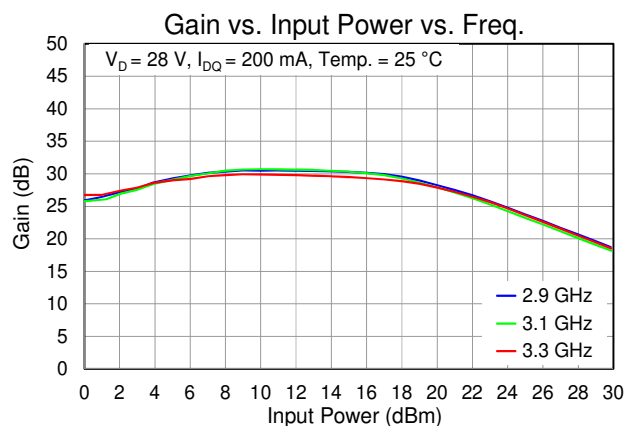
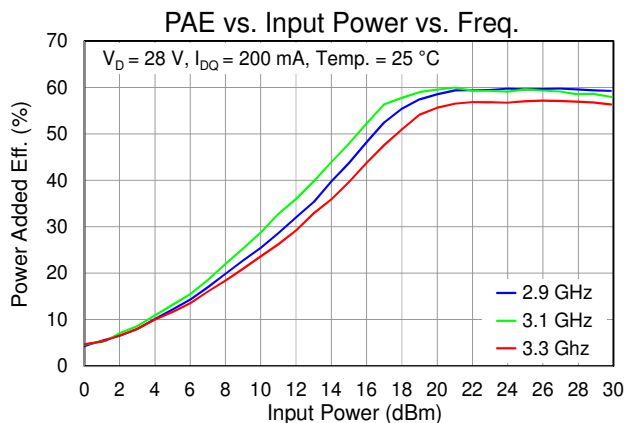
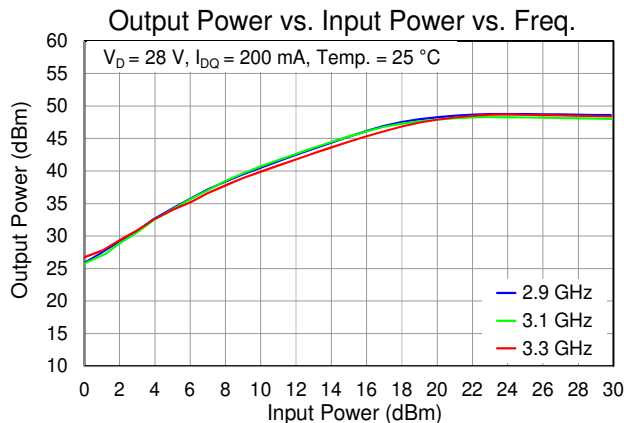
Typical Performance

Test conditions unless otherwise noted: Temp. = 25 °C, Pulsed input power PW = 100 us, Duty Cycle = 10%



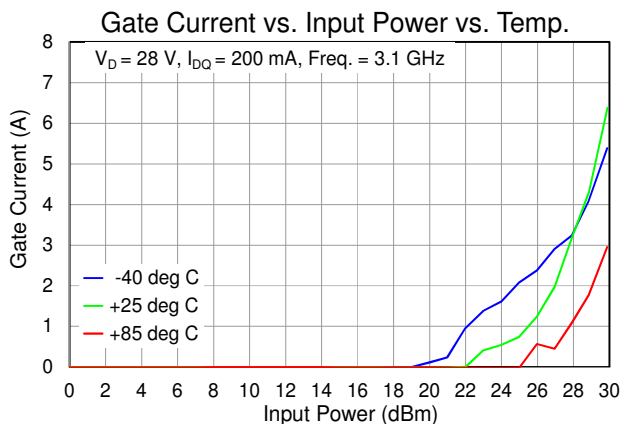
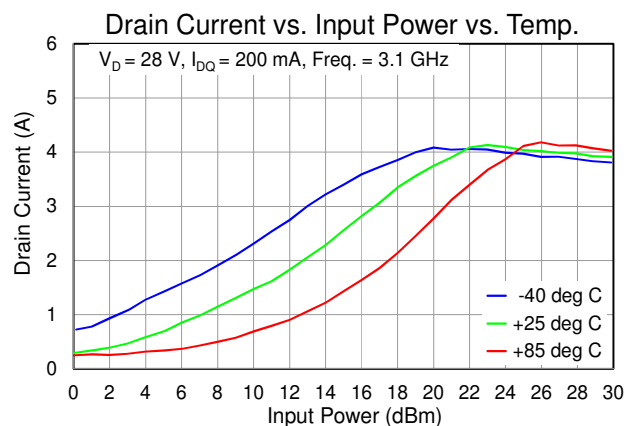
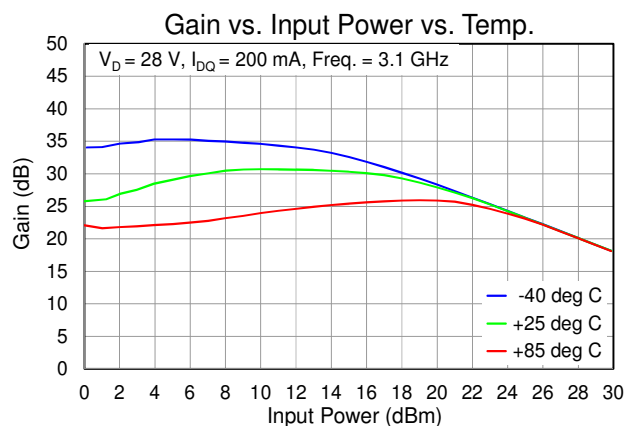
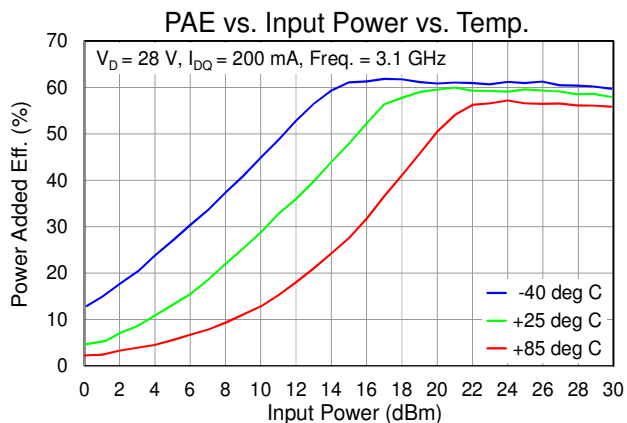
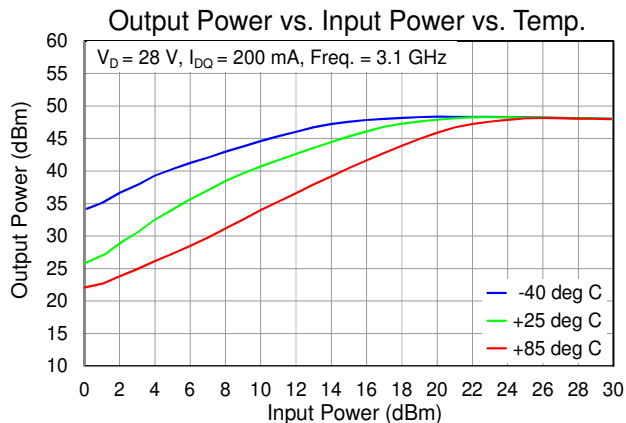
Typical Performance

Test conditions unless otherwise noted: Pulsed input power PW = 100 us, Duty Cycle = 10%

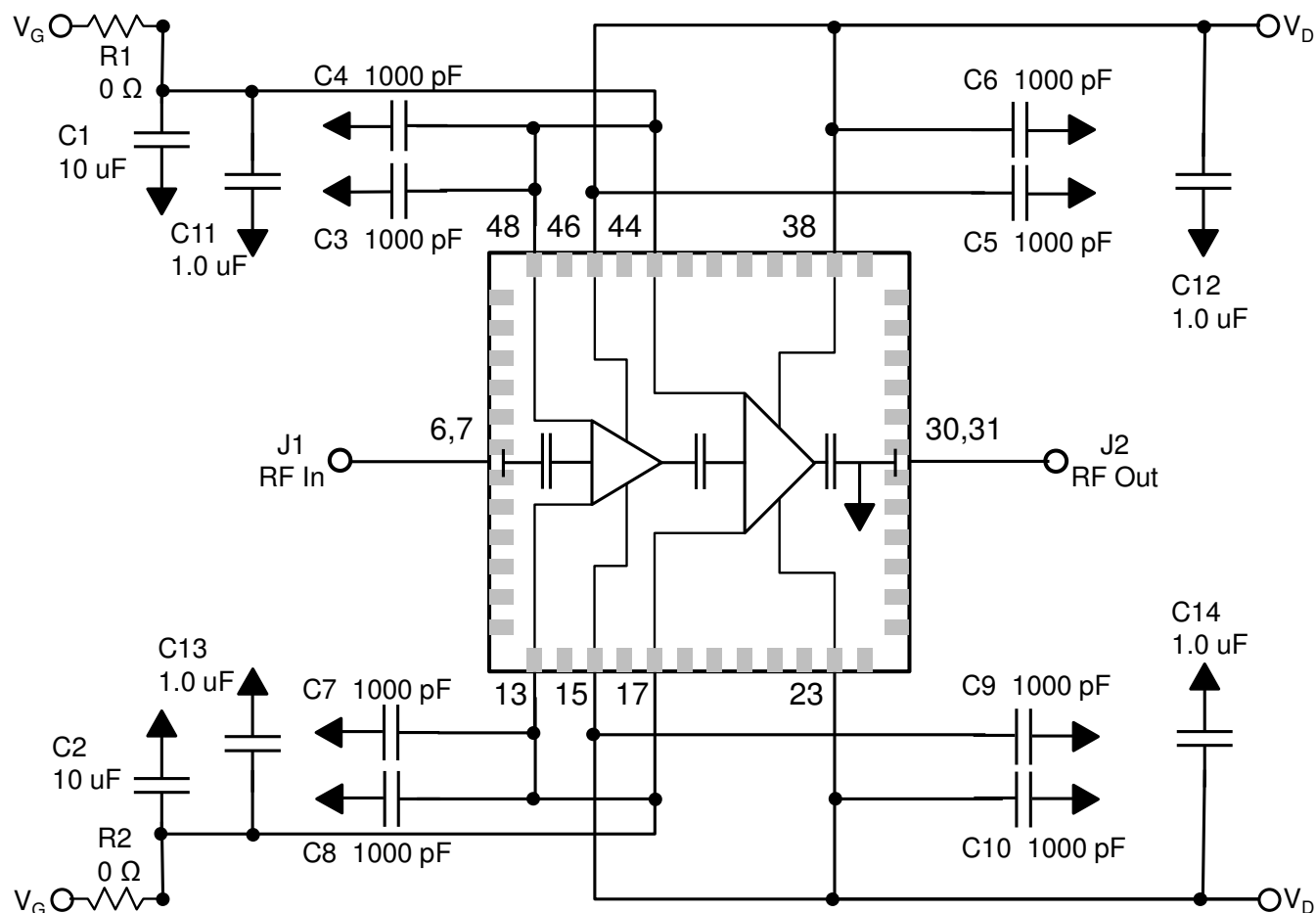


Typical Performance

Test conditions unless otherwise noted: Pulsed input power PW = 100 us, Duty Cycle = 10%



Application Circuit



Notes:

1. V_G and V_D must be biased from both sides (top and bottom).

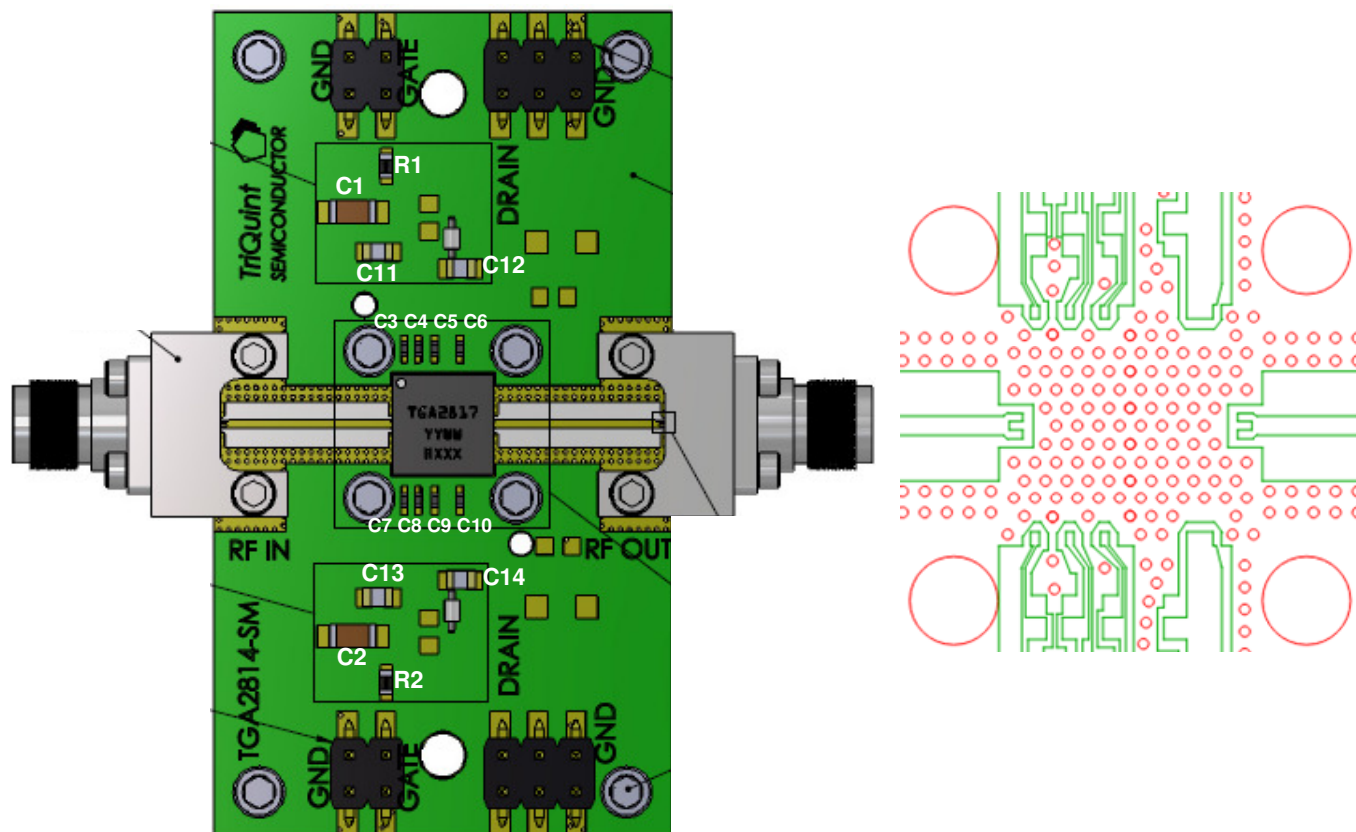
Bias-up Procedure

1. Set I_D limit to 6000mA, I_G limit to 40mA
2. Set V_G to -6.0 V
3. Set V_D +28 V
4. Adjust V_G more positive until $I_{DQ} = 200mA$ ($V_G \sim -2.8$ V Typical)
5. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_G to -6.0V. Ensure $I_{DQ} \sim 0mA$
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

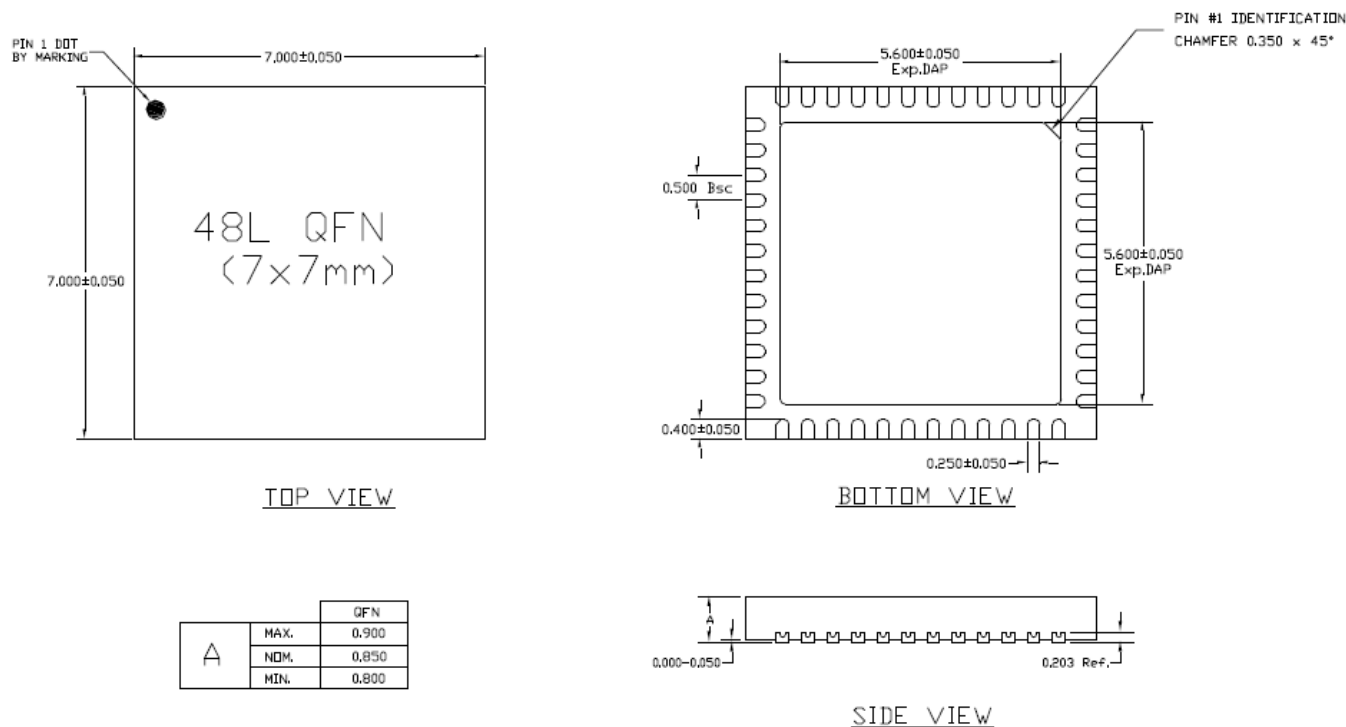
Evaluation Board and Mounting Detail



RF Layer is 0.008" thick Rogers Corp. RO40003C ($\epsilon_r = 3.35$). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-02A-5.

Reference	Des.	Component	Value	Manuf.	Part Number
C1, C2		Surface Mount Cap	10 uF, 20 %, 50 V (1206), X5R	Various	
C3 – C10		Surface Mount Cap	1000 pF, 10 %, 50 V (0402), X7R	Various	
C11 – C14		Surface Mount Cap	1.0 uF, 10 %, 25 V (0402), X7R	Various	
R1, R2		Surface Mount Res	0 Ohm, 5 % (0603)	Various	

Mechanical Drawing and Pad Description



Dimensions are in mm.

Pad No.	Symbol	Description
1-5, 8-12, 14, 16, 18-22, 24-29, 32-37, 39-43, 45, 47, 49	GND	Ground connection.
6, 7	RF Input	50 Ohm RF input. Pad is capacitively coupled to block on-chip DC voltages.
13, 48	V _{G1}	1 st Stage Gate Voltage; bias network is required; must be biased from both sides (V _{G1} and V _{G2} can be tied together in application)
15, 46	V _{D1}	1 st Stage Drain Voltage; bias network is required; must be biased from both sides (V _{D1} and V _{D2} can be tied together in application)
17, 44	V _{G2}	2 nd Stage Gate Voltage; bias network is required; must be biased from both sides (V _{G1} and V _{G2} can be tied together in application)
23, 38	V _{D2}	2 nd Stage Drain Voltage; bias network is required; must be biased from both sides (V _{D1} and V _{D2} can be tied together in application)
30, 31	RF Output	50 Ohm RF output. Pad is capacitively coupled to block on-chip DC voltages. Pad is DC grounded.

Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

MSL Rating: Level 3
Test: 260 °C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

ECCN

US Department of Commerce: 3A001.b.2.a

Solderability

Compatible with the latest version of J-STD-020 Lead free solder, 260 °C.

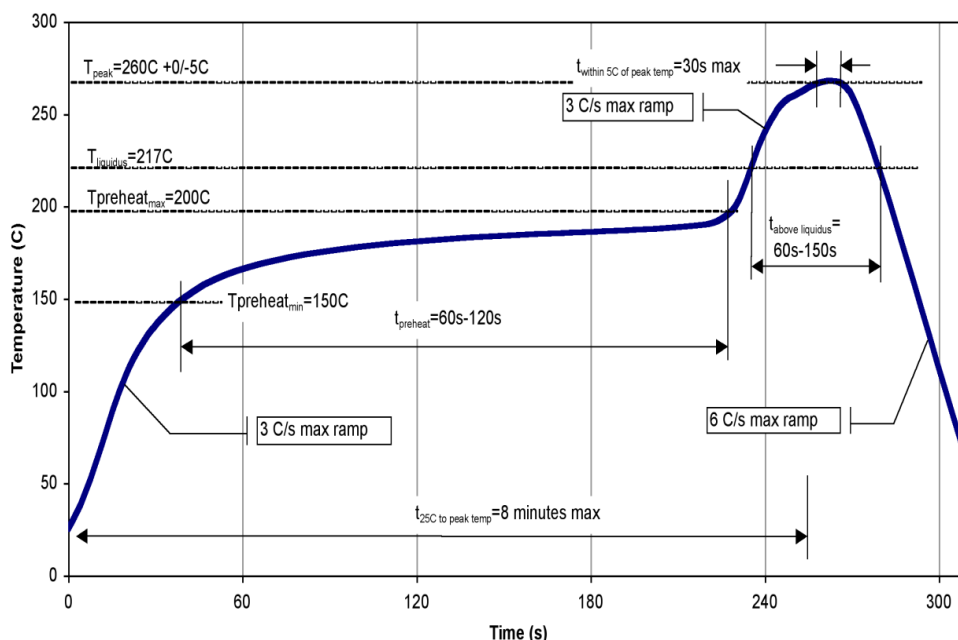
RoHS-Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br4O2) Free
- PFOS Free
- SVHC Free

Recommended Soldering Temperature Profile



Contact Information

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Fax: +1.972.994.8504

For technical questions and application information: **Email:** info-products@tqs.com

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