

7-12GHz LNA

GaAs Monolithic Microwave IC

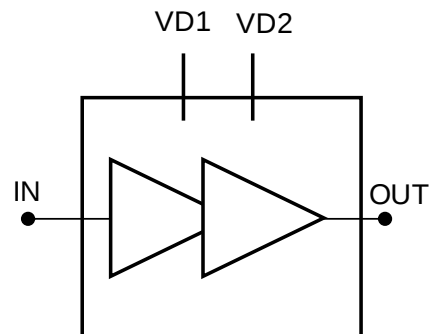
Description

The CHA2110-98F is a monolithic two-stages wide band low noise amplifier circuit. It is self-biased.

It is designed for military, space and telecommunication systems.

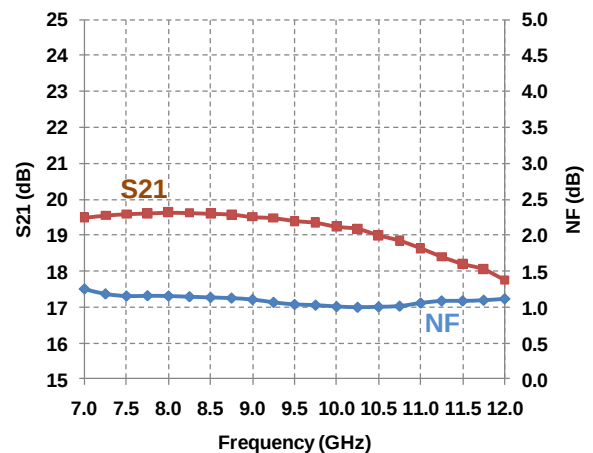
The circuit is manufactured with a pHEMT process, 0.25 μ m gate length, via holes through the substrate, and air bridges.

It is available in chip form.



Main Features

- Broadband performances: 7-12GHz
- Linear gain: 19dB
- Return Losses: 12dB
- Noise Figure: 1.2dB
- Output power @ 1dBcomp: 11dBm
- DC bias: Vd=4 Volt@Id=45mA
- Chip size 1.93x1.3x0.1mm



Gain and NF versus frequency

Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7		12	GHz
Gain	Linear Gain		19		dB
NF	Noise Figure		1.2		dB
Pout	Output Power @1dB comp (f=10GHz)		11		dBm

Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7		12	GHz
Gain	Linear Gain		19		dB
NF	Noise Figure		1.2		dB
RL_in	Input return losses		-12		dB
RL_out	Output return losses		-12		dB
P1dB	Output power at 1dB comp (f=10GHz)		11		dBm
IP3	3 rd order interception point (f=10GHz)		21		dB
Vd	Drain supply voltage (self biased)		4		V
Id	Drain supply current		45		mA

These values are representative of measurements on test fixture.

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5V	V
Id	Drain bias current	70	mA
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.⁽²⁾ Duration < 1s.**Typical Bias Conditions**

Tamb.= +25°C

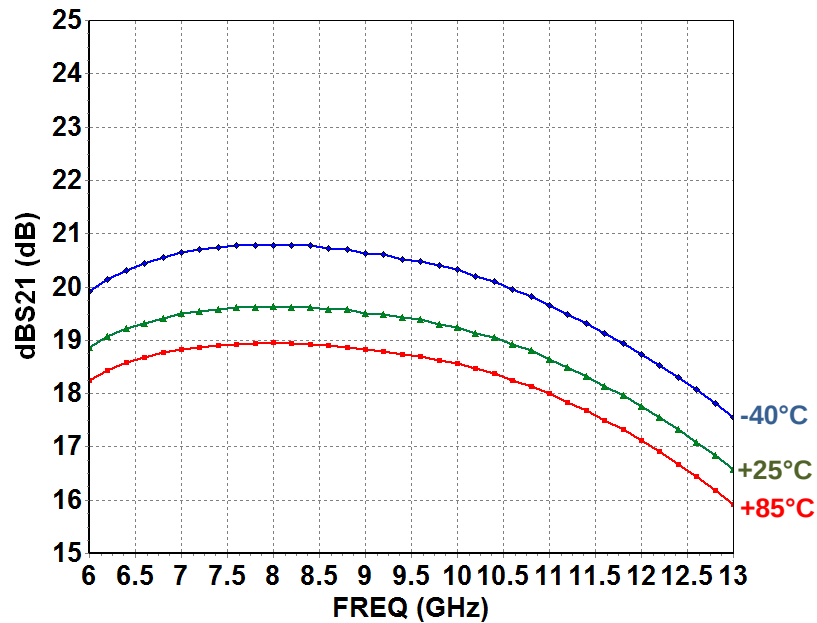
Symbol	Pad N°	Parameter	Values	Unit
Vd	VD1, VD2	Drain supply voltage	4	V

The circuit is self-biased.

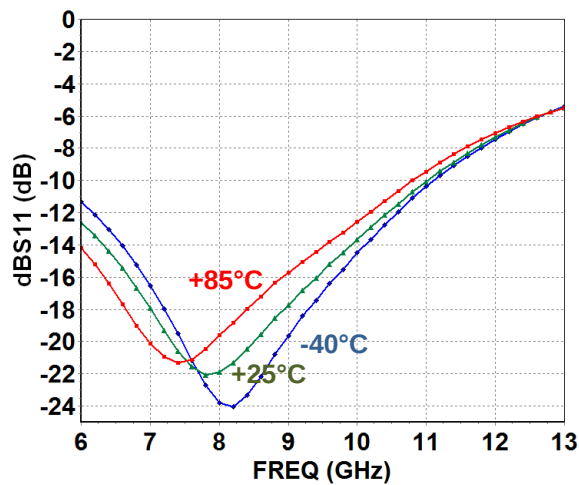
Test fixture Measurements

T=[-40°C ; +25°C ; +85°C], Vd = +4V, Id = 45mA

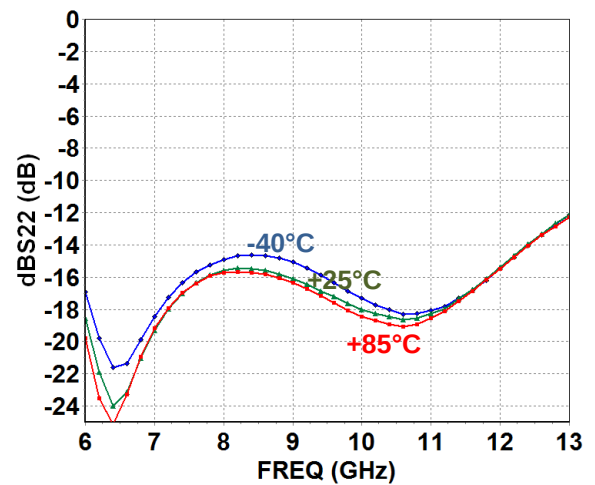
S21 versus frequency



Input return loss



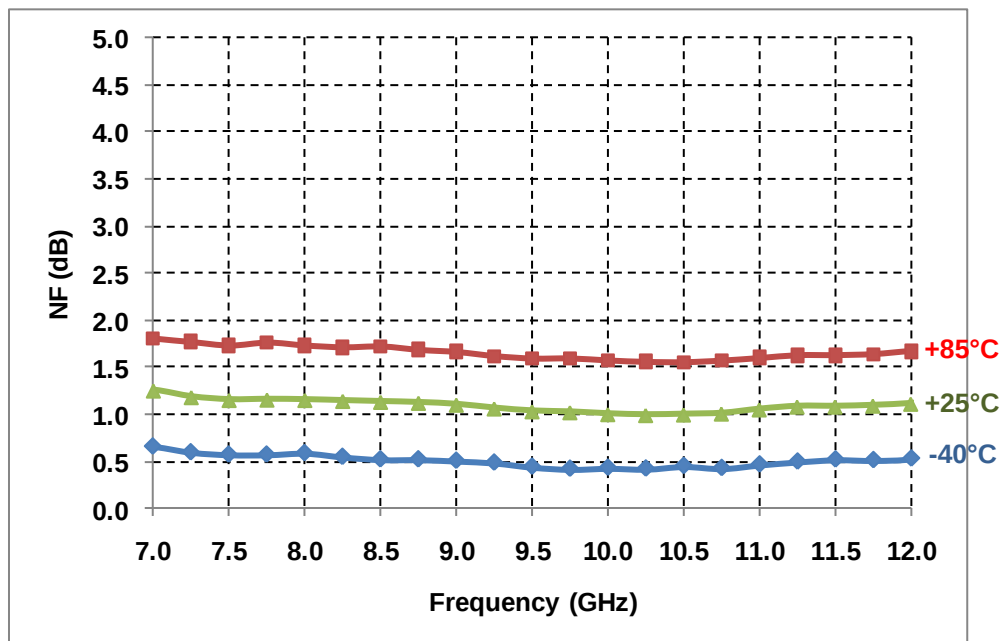
Output Return loss



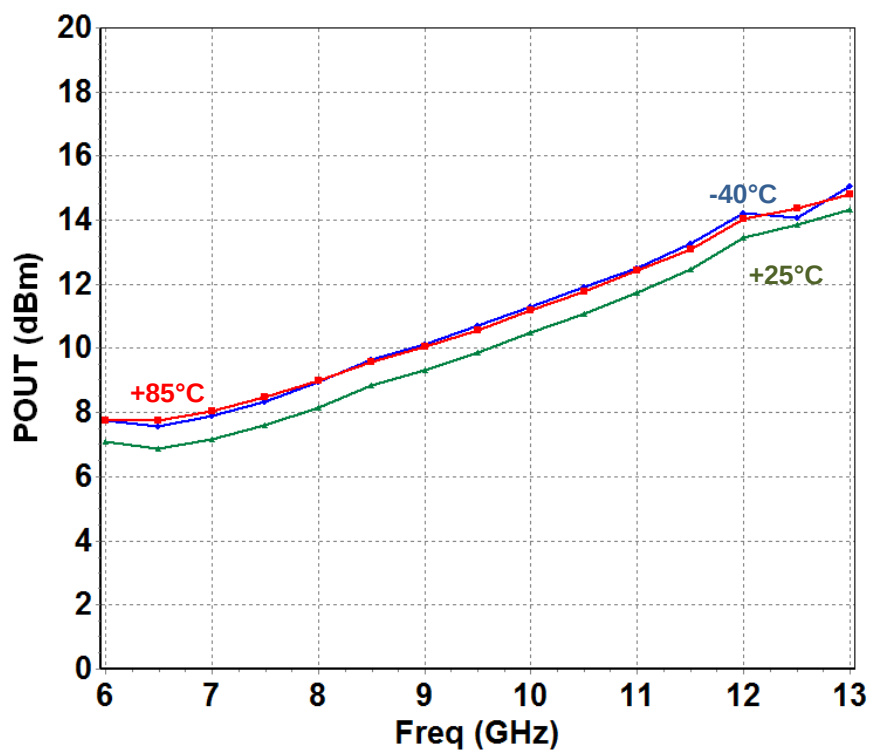
Test fixture Measurements

$T = [-40^{\circ}\text{C} ; +25^{\circ}\text{C} ; +85^{\circ}\text{C}]$, $V_d = +4\text{V}$, $I_d = 45\text{mA}$

Noise Figure versus frequency

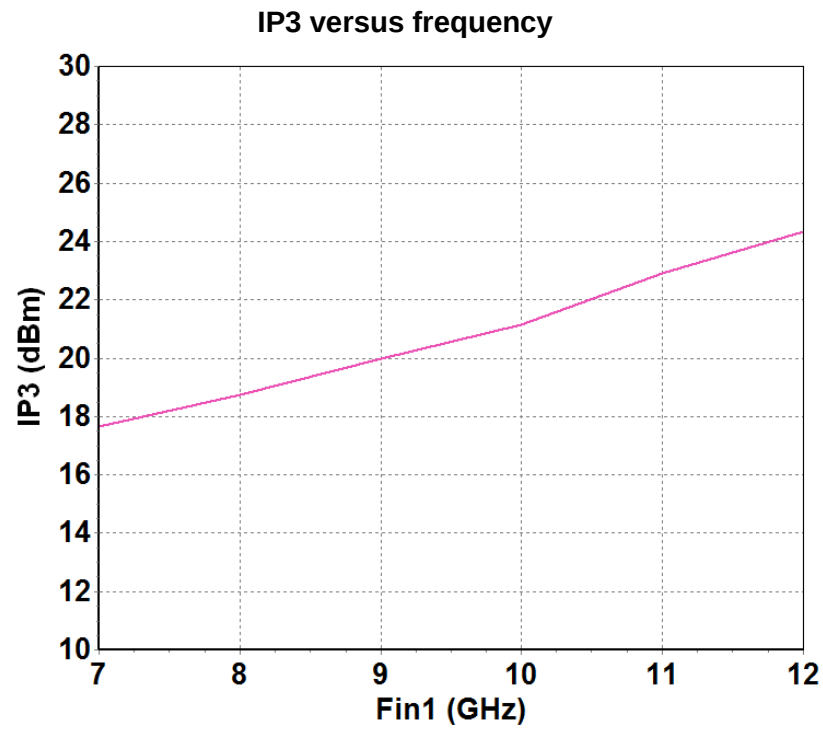


P1dB versus frequency

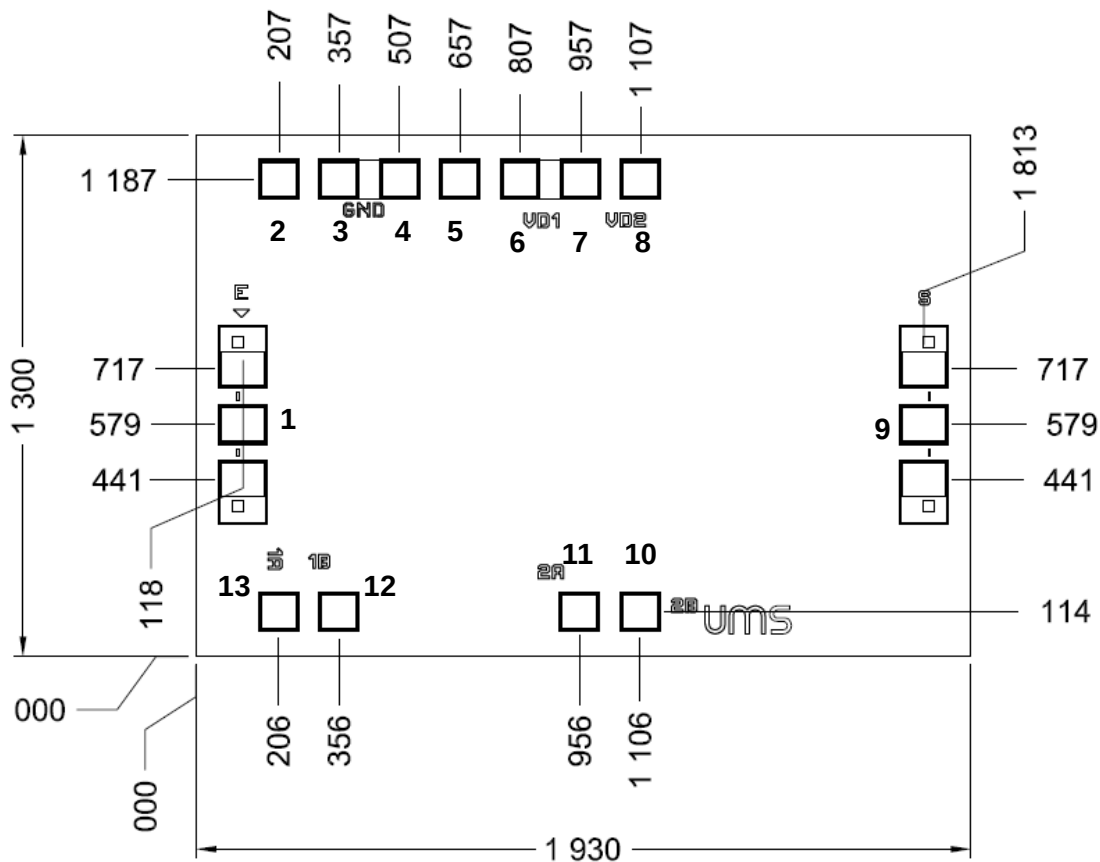


Test fixture Measurements

Tamb=+25°C, Vd = +4V, Id = 45mA



Mechanical data

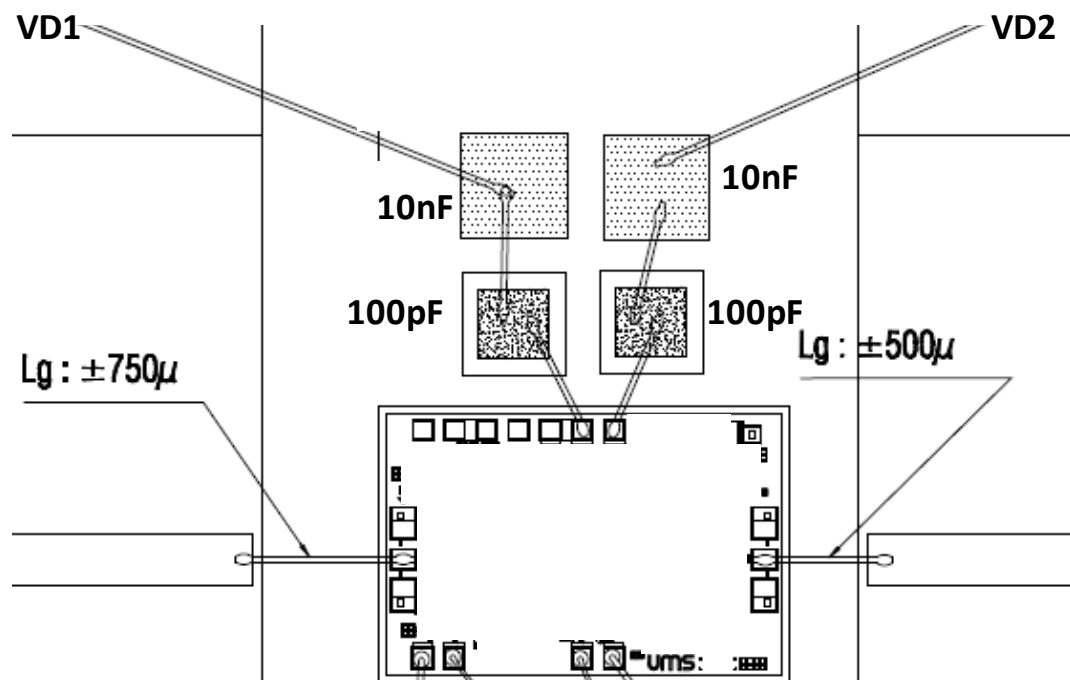


Chip thickness: 100μm.
Chip size: 1300x1930 ±35μm
All dimensions are in micrometers

RF pads (1, 9)	= 100x120 μ m ²
DC pads (2,3,4,5,6,7,8,10,11,12,13)	= 100x100 μ m ²

Pin number	Pin name	Description
1	E	Input RF
2	none	NC
3, 4	GND	NC
5	none	NC
6, 7	VD1	Vd
8	VD2	Vd
9	S	Output RF
10	2B	NC
11	2A	NC
12	1B	NC
13	1A	NC

Recommended assembly plan



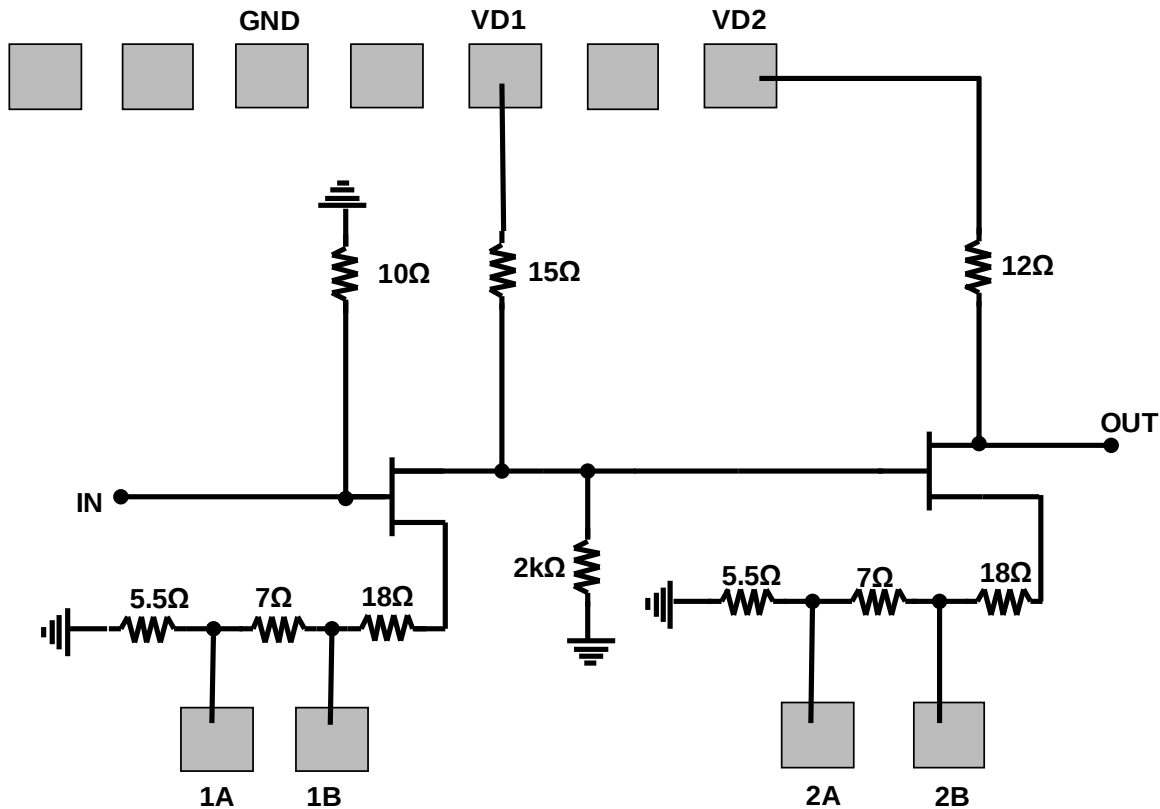
Note: Supply feed should be bypassed. 25μm diameter gold wire is to be preferred.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
E	Input RF	N/A	Inductance ($L_{\text{bonding}} \approx 750\mu\text{m}$) = 0.6nH, 1 gold wire with diameter of 25μm
Vd1, Vd2	Vd	100pF & 10nF	Drain Supply Inductance $\leq 1\text{nH}$
S	Output RF	N/A	Inductance ($L_{\text{bonding}} \approx 500\mu\text{m}$) = 0.4nH, 1 gold wire with diameter of 25μm

Chip biasing options

This chip is self-biased, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



The requirement is :

Not to exceed $V_{ds} = 3.5\text{V}$ (internal Drain to Source voltage).

We propose three standard biasing :

Low Noise and low consumption:

$V_d = 4\text{V}$.

The pads 1A, 1B, 2A and 2B are non-connected (NC).

$I_{dd} = 45\text{mA}$ & $P_{out-1dB} = +11\text{dBm}$ Typical ($f=10\text{GHz}$).

Low Noise and higher gain:

$V_d = 4\text{V}$ and 1A or 1B grounded.

All the other pads non connected (NC).

$I_{dd} = 55\text{mA}$ & $P_{out-1dB} = +11\text{dBm}$ Typical ($f=10\text{GHz}$)

Low Noise and higher output power:

$V_d = 4\text{V}$ and 2A or 2B grounded.

All the other pads non connected (NC).

$I_{dd} = 55\text{mA}$ & $P_{out-1dB} = +13\text{dBm}$ Typical ($f=10\text{GHz}$)

Note

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Ordering Information

Chip form:

CHA2110-98F/00

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.**. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**