

## FEATURES

- InGaP HBT Technology
- -47 dBc ACPR @  $\pm 10$  MHz, +27 dBm
- 29 dB Gain
- High Efficiency
- Low Transistor Junction Temperature
- Matched for a  $50\ \Omega$  System
- Low Profile Miniature Surface Mount Package; RoHS Compliant
- Multi-Carrier Capability

## APPLICATIONS

- LTE, WCDMA and HSDPA Air Interfaces
- FDD and TDD Systems
- Picocell, Femtocell, Home Nodes
- Customer Premises Equipment (CPE)
- Data Cards and Terminals

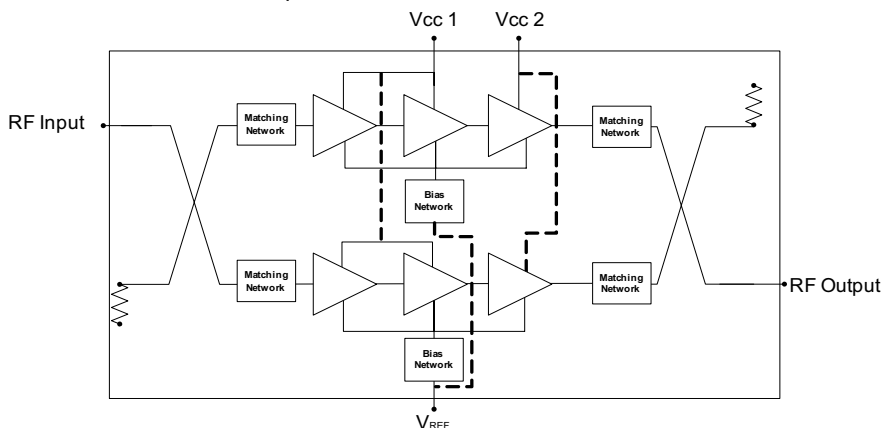


**14 Pin 7 mm x 7 mm x 1.3 mm  
Surface Mount Module**

## PRODUCT DESCRIPTION

The AWB7231 is a fully matched, Multi-Chip-Module (MCM) designed for picocell, femtocell, and customer premises equipment (CPE) applications. Its high linearity and efficiency meet the extremely demanding needs of small cell infrastructure architectures. Designed for LTE, WCDMA and HSDPA air interfaces operating in the 2.01 to 2.025 GHz band, the AWB7231 delivers up to +27 dBm of LTE (E-TM1.1) power with an ACPR of -47 dBc. It operates from

a convenient +4.5 V supply and provides 29 dB of gain. The device is manufactured using an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness. The self-contained 7 mm x 7 mm x 1.3 mm surface mount package incorporates RF matching networks optimized for output power, efficiency, and linearity in a  $50\ \Omega$  system.



**Figure 1: Block Diagram**

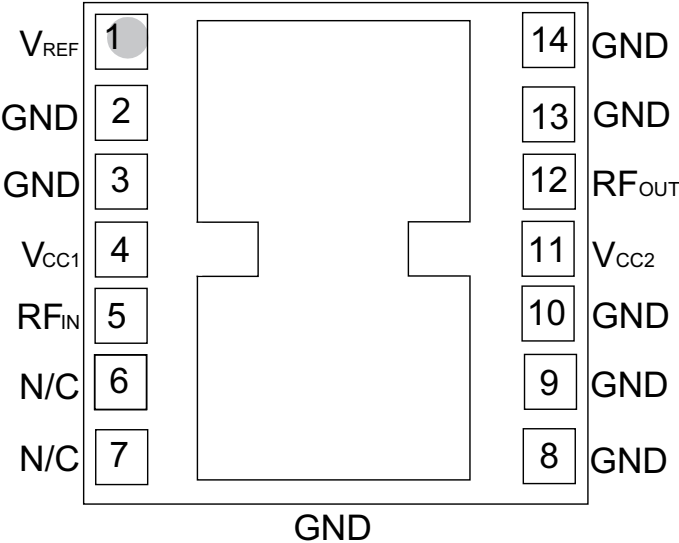


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V <sub>REF</sub>	Reference Voltage
2	GND	Ground
3	GND	Ground
4	V <sub>CC1</sub>	Supply Voltage
5	RF <sub>IN</sub>	RF Input
6	N/C	No Connection
7	N/C	No Connection
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	V <sub>CC2</sub>	Supply Voltage
12	RF <sub>OUT</sub>	RF Output
13	GND	Ground
14	GND	Ground

## ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage ( $V_{CC}$ )	0	+5	V
Reference Voltage ( $V_{REF}$ )	0	+3.5	V
RF Output Power ( $P_{OUT}$ )	-	+30	dBm
ESD Rating			
Human Body Model <sup>(1)</sup>	TBD	-	
Charged Device Model <sup>(2)</sup>	TBD	-	
MSL Rating <sup>(3), (4)</sup>	4	-	
Junction Temperature ( $T_J$ )	-	+150	°C
Storage Temperature ( $T_{STG}$ )	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:

(1) JEDEC JS-001-2010.

(2) JEDEC JESD22-C101D.

(3) 260 °C peak reflow.

(4) Pending qualification results.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	2010	-	2025	MHz	
Supply Voltage ( $V_{CC}$ )	+3.6	+4.5	+4.65	V	
Reference Voltage ( $V_{REF}$ )	+2.75 0	+2.85 -	+2.95 +0.5	V	PA "on" PA "shut down"
RF Output Power ( $P_{OUT}$ )	-	+27	-	dBm	
Case Temperature ( $T_C$ )	-40	-	+85	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

**Table 4: Electrical Specifications**  
**(T<sub>C</sub> = +25 °C, V<sub>CC</sub> = +4.5 V, V<sub>REF</sub> = +2.85 V, 50 Ω system)**

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain <sup>(2)</sup>	-	29	-	dB	
ACPR <sup>(1), (2), (3)</sup> @ 10 MHz @ 20 MHz	- -	-47 -57	- -	dBc	
Power-Added Efficiency <sup>(1), (2), (3)</sup>	-	14	-	%	
Thermal Resistance (R <sub>JC</sub> ) <sup>(4)</sup>	-	TBD	-	°C/W	Junction to Case
Supply Current <sup>(1), (2), (3)</sup>	-	795	-	mA	total through V <sub>CC</sub> pins
Quiescent Current (I <sub>cq</sub> )	-	275	-	mA	
Reference Current	-	14	-	mA	through V <sub>REF</sub> pin
Leakage Current	-	3	10	μA	V <sub>CC</sub> = +4.65 V, V <sub>REF</sub> = 0 V
Harmonics 2f <sub>o</sub> 3f <sub>o</sub> , 4f <sub>o</sub>	- -	-40 -45	- -	dBc	
Input Return Loss	-	18	-	dB	
Output Return Loss	-	18	-	dBm	
RF Switching Time <sup>(5)</sup> Rise Time (PA “off” to “on”) Fall Time (PA “on” to “off”)	- -	- -	12 4	μs	V <sub>CC</sub> = +4.5 V, V <sub>REF</sub> switched between 0 V and +2.85 V
Spurious Output Level (all spurious outputs)	-	-	-60	dBc	P <sub>OUT</sub> ≤ +27 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all voltage and temperature operating ranges
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	V <sub>CC</sub> = +4.5 V, P <sub>OUT</sub> = +27 dBm Applies over full operating temperature range

Notes:

(1) Measured at 2017.5 MHz.

(2) P<sub>OUT</sub> = +27 dBm.

(3) E-TM1.1 LTE 10 MHz BW.

(4) Use only V<sub>CC2</sub> (pin 11) current when calculating device junction temperature.

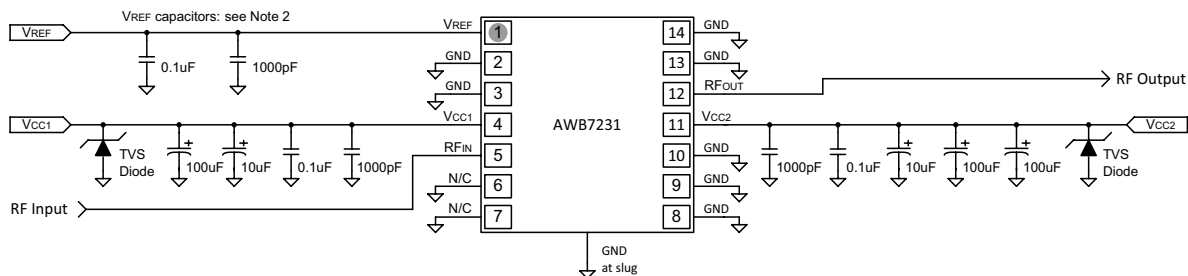
(5) Rise Time defined from time at which V<sub>REF</sub> is switched from 0 V to +2.85 V, to time at which the RF output power achieves 90% of the average steady-state “on” level; Fall Time defined from time at which V<sub>REF</sub> is switched from +2.85 V to 0 V, to time at which the RF output power decreases to 10% of the average steady-state “on” level.

## APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site:  
<http://www.anadigics.com>

### Shutdown Mode

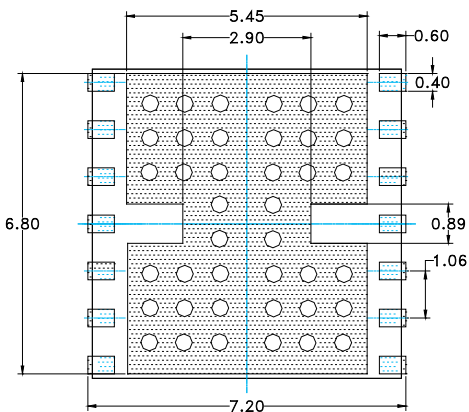
The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the  $V_{REF}$  voltage.



#### Notes:

1. Applications that have large supply voltage transients may benefit from the use of TVS diodes. For such applications, recommended TVS diodes are SM05T1G or SMJ5.0A.
2. To achieve the RF Switching Time specifications listed in Table 4, the maximum recommended capacitance on the  $V_{REF}$  line is  $0.01\mu\text{F}$ . The noise on the  $V_{REF}$  line should be kept as low as possible to minimize required capacitance.

**Figure 3: Application Circuit Schematic**

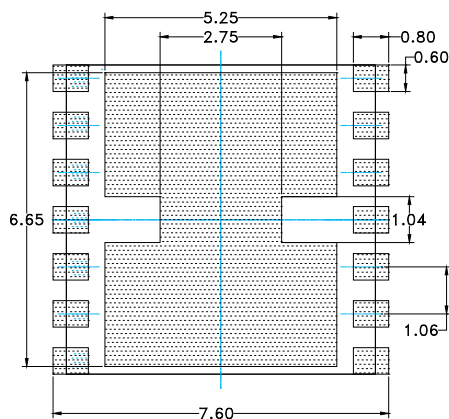


PCB METAL  
TOP (X-RAY) VIEW

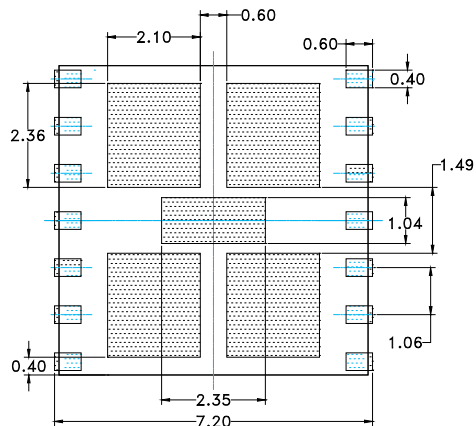
ONLY PACKAGE I/O's AND  
GROUND REQUIREMENTS  
SHOWN.

**NOTES:**

- (1) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
- (2) DIMENSIONS IN MILLIMETERS.
- (3) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.



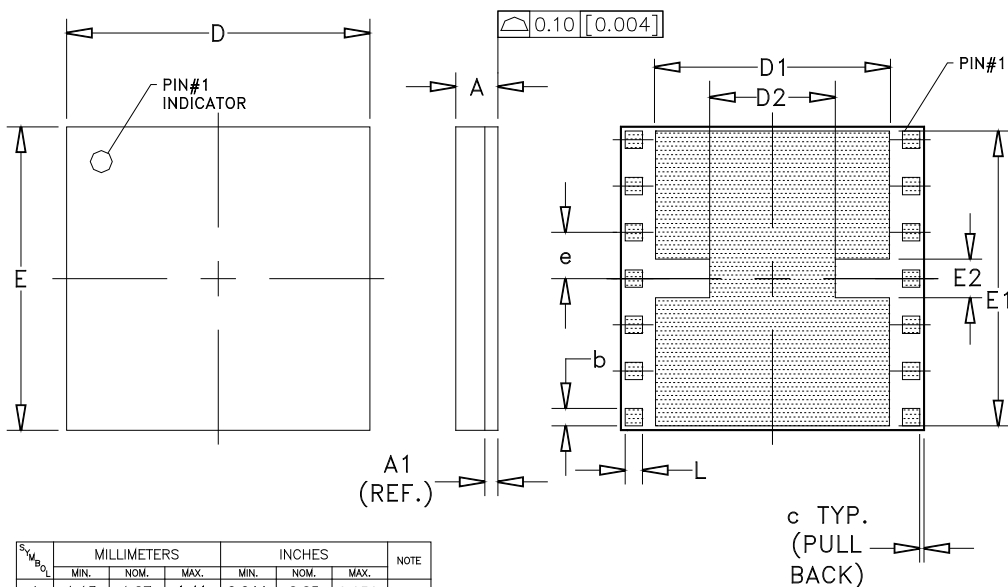
PCB SOLDER MASK  
TOP (X-RAY) VIEW



STENCIL APERTURE  
TOP (X-RAY) VIEW

**Figure 4: PCB Footprint**

## PACKAGE OUTLINE



## NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN  
UNIFORM SIZE FOR REFERENCE ONLY.  
ACTUAL PAD SIZE AND LOCATION WILL  
VARY WITHIN MIN. AND MAX. DIMENSIONS  
ACCORDING TO SPECIFIC LAMINATE DESIGN.

Figure 5: Package Outline - 14 Pin 7 mm x 7 mm x 1.3 mm Surface Mount Module

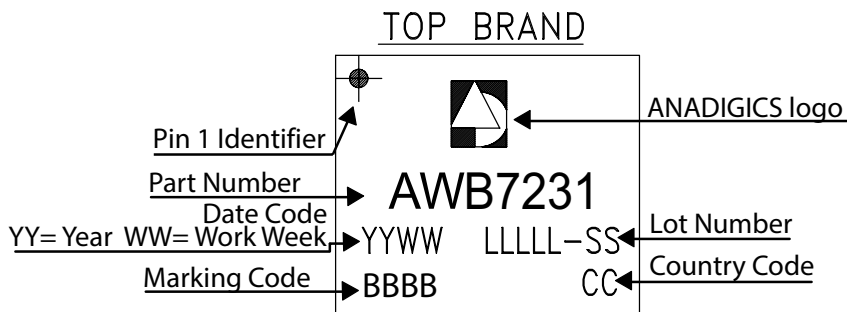


Figure 6: Branding Specification



### Table 5: Tape & Reel Dimensions

PACKAGE TYPE	TAPE WIDTH	POCKET PITCH	REEL CAPACITY	MAX REEL DIA
7 mm x 7 mm x 1.3 mm	16 mm	12 mm	2500	13"





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