AWC6323

HELP3E™ Dual-band Cellular & PCS CDMA
3.4 V Linear Power Amplifier Module

Data Sheet - Rev 2.0

FEATURES

- InGaP HBT Technology
- High Efficiency:
  37 % @ +27.6 dBm
  22 % @ +16 dBm
  11 % @ +10 dBm
- Low Quiescent Current: <4 mA
- Internal Voltage Regulation
- Built-in Directional Coupler
- Common V_{MODE} Control Line
- Simplified V_{CC} Bus PCB routing
- Reduced External Component Count
- Low Profile Surface Mount Package: 1 mm
- RoHS Compliant Package, 260 °C MSL-3

M47 Package
14 Pin 3 mm x 5 mm x 1 mm
Surface Mount Module

APPLICATIONS

- Cell & PCS Dual-band Wireless Handsets and Data Devices for CDMA/EVDO networks.

PRODUCT DESCRIPTION

AWC6323 addresses the demand for increased integration in dual-band handsets for CDMA networks. The small footprint 3 mm x 5 mm x 1 mm surface-mount RoHS compliant package contains independent RF PA paths to ensure optimal performance in both frequency bands, while achieving a 25% PCB space savings compared with solutions requiring two single-band PAs. The package pinout was chosen to enable handset manufacturers to easily route bias to both power amplifiers and simplify control with common mode pins. The device is manufactured on an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness. The AWC6323 is part of ANADIGICS' High-Efficiency-at-Low-Power (HELP™) family of CDMA power amplifiers, which deliver low quiescent currents and significantly greater efficiency without the need of an external DC-DC converter. Through selectable bias modes, the AWC6323 achieves optimal efficiency, specifically at low- and mid-range power levels where the PA typically operates, thereby dramatically increasing handset talk-time. Its built-in voltage regulator eliminates the need for external switches. This PA has built-in directional couplers for each band, with a common coupler output port CPL_OUT. The 3 mm x 5 mm x 1 mm surface mount package incorporates matching networks optimized for output power, efficiency and linearity in a 50 Ω system.

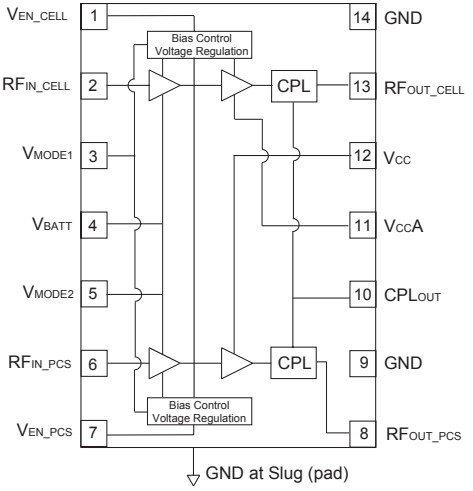


Figure 1: Block Diagram

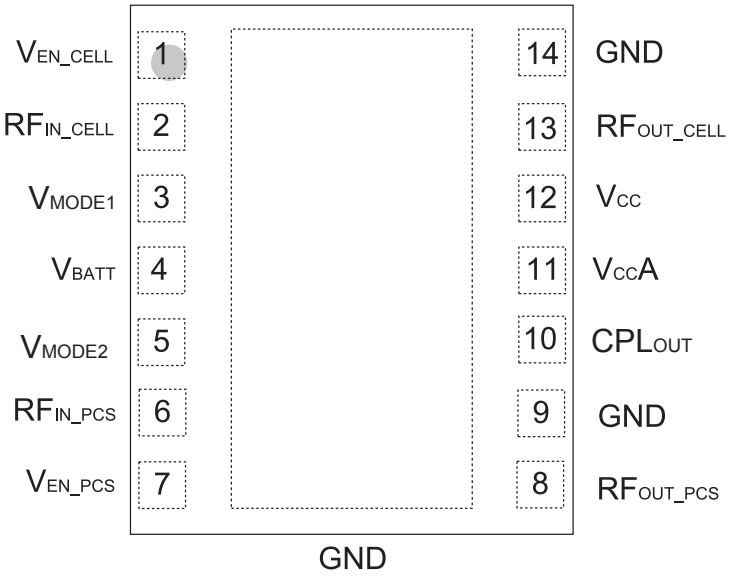


Figure 2: Pinout

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V_{EN_CELL}	Enable Voltage for Cell Band
2	RF_{IN_CELL}	RF Input for Cell Band
3	V_{MODE1}	Mode Control Voltage 1
4	V_{BATT}	Battery Voltage
5	V_{MODE2}	Mode Control Voltage 2
6	RF_{IN_PCS}	RF Input for PCS Band
7	V_{EN_PCS}	Enable Voltage for PCS Band
8	RF_{OUT_PCS}	RF Output for PCS Band
9	GND	Ground
10	CPL_{OUT}	Coupler Output Port
11	$V_{CC}A$	Battery Voltage A
12	V_{CC}	Supply Voltage
13	RF_{OUT_CELL}	RF Output for Cell Band
14	GND	Ground

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (V_{BATT}, V_{CC}, $V_{CC}A$)	0	+5	V
Mode Control Voltage (V_{MODE1}, V_{MODE2})	0	+3.5	V
Enable Voltage (V_{EN_CELL}, V_{EN_PCS})	0	+3.5	V
RF Input Power (P_{IN})	-	+10	dBm
Storage Temperature (T_{STG})	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	824 1850	-	849 1910	MHz	Cellular PCS
Supply Voltage (V_{CC} and V_{BATT})	+3.2	+3.4	+4.2	V	
Enable Voltage (V_{EN})	+1.35 0	+1.8 -	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage (V_{MODE1}, V_{MODE2})	+1.35 0	+1.8 -	+3.1 +0.5	V	High State Voltage Low State Voltage
Cellular RF Output Power (P_{OUT}) CDMA, HPM CDMA, MPM CDMA, LPM	 +27.1 (1) - -	 27.6 16 10	 - - -	dBm	CDMA 2000, RC-1
PCS RF Output Power (P_{OUT}) CDMA, HPM CDMA, MPM CDMA, LPM	 +27.4 (1) - -	 +27.9 16 10	 - - -	dBm	CDMA 2000, RC-1
Case Temperature (T_C)	-30	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

(1) For operation at V_{CC} = +3.2 V, P_{OUT} is derated by 0.5 dB.

Table 4a: Electrical Specifications - Cellular Band (BC 0)
(T_C = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{EN_CELL} = +1.8 V, 50 Ω system, CDMA2000 RC-1 waveform)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					V_{MODE1}	V_{MODE2}	P_{OUT}
Gain	25 14 8	27 17 11.5	30 19 14	dB	0 V 1.8 V 0/1.8 V	1.8 V 1.8 V 0 V	+27.6 dBm +16 dBm +10 dBm
Adjacent Channel Power at ±885 kHz offset (1) Primary Channel BW = 1.23 MHZ Adjacent Channel BW = 30 kHz	 - - -	 -51 -52 -50	 -46.5 -46.5 -46.5	dBc	 0 V 1.8 V 0/1.8 V	 1.8 V 1.8 V 0 V	 +27.6 dBm +16 dBm +10 dBm
Alternate Channel Power at ±1.98 MHz offset (1) Primary Channel BW = 1.23 MHZ Adjacent Channel BW = 30 kHz	 - - -	 -61 -63 <-68	 -57 -57 -57	dBc	 0 V 1.8 V 0/1.8 V	 1.8 V 1.8 V 0 V	 +27.6 dBm +16 dBm +10 dBm
Power-Added Efficiency (1)	34 18 8	37.5 23 11.5	- - -	%	0 V 1.8 V 0/1.8 V	1.8 V 1.8 V 0 V	+27.6 dBm +16 dBm +10 dBm
Quiescent Current (Icq)	-	3.5	6	mA	through V_{CC} pins, V_{MODE1} = 0/1.8 V, V_{MODE2} = 0 V		
Mode Control Current	-	<0.05	0.1	mA	through V_{MODE} pins, V_{MODE1}= 0/1.8 V, V_{MODE2} = 0 V		
Battery Current	-	1	2	mA	through V_{BATT} pin, V_{MODE1} = 0/1.8 V, V_{MODE2} = 0 V		
Enable Current	-	<0.1	0.15	mA	through V_{EN_CELL} pin		
Noise in Receive Band(2)	-	-133 -138	-131 -135	dBm/Hz	V_{MODE1} = 0 V, V_{MODE2} = 1.8 V, V_{MODE1} = V_{MODE2} = 1.8 V		
Harmonics 2fo 3fo, 4fo	 - -	 -43 -50	 -30 -30	dBc	$P_{OUT} \leq$ +27.6 dBm		
Input Impedance	-	-	2:1	VSWR			
Coupling Factor	-	22	-	dB			

Table 4b: Electrical Specifications - Cellular Band (BC 0)
(T_C = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{EN_CELL} = +1.8 V, 50 Ω system, CDMA2000 RC-1 waveform)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					V_{MODE1}	V_{MODE2}	P_{OUT}
Spurious Output Level (all spurious outputs)	-	-	-65	dBc	$P_{OUT} \leq$ +27.6 dBm In-band Load VSWR < 5:1 Out-of-band Load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating conditions		

Notes:
(1) PAE and ACP measured at 836.5 MHz.
(2) 869 MHz to 894 MHz.

Table 5a: Electrical Specifications - PCS Band (BC 1)
(T_C = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{EN_PCS} = +1.8 V, 50 Ω system, CDMA2000 RC-1 waveform)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					V_{MODE1}	V_{MODE2}	P_{OUT}
Gain	24.5 10 7	26.5 13.5 10	30 16 13	dB	0 V 1.8 V 0/1.8 V	1.8 V 1.8 V 0 V	+27.9 dBm +16 dBm +10 dBm
Adjacent Channel Power at ±1.25 MHz offset (1) Primary Channel BW = 1.23 MHZ Adjacent Channel BW = 30 kHz	- - -	-51 -52 -52	-46.5 -46.5 -46.5	dBc	0 V 1.8 V 0/1.8 V	1.8 V 1.8 V 0 V	+27.9 dBm +16 dBm +10 dBm
Alternate Channel Power at ±1.98 MHz offset (1) Primary Channel BW = 1.23 MHZ Adjacent Channel BW = 30 kHz	- - -	-56 -59 -63	-54 -54 -54	dBc	0 V 1.8 V 0/1.8 V	1.8 V 1.8 V 0 V	+27.9 dBm +16 dBm +10 dBm
Power-Added Efficiency (1)	33 18 8	36.5 21 11	- - -	%	0 V 1.8 V 0/1.8 V	1.8 V 1.8 V 0 V	+27.9 dBm +16 dBm +10 dBm
Quiescent Current (Icq)	-	3.5	6	mA	through V_{BATT} and V_{CC} pins, V_{MODE1} = 0/1.8 V, V_{MODE2} = 0 V		
Mode Control Current	-	0.05	0.1	mA	tthrough V_{MODE} pins, V_{MODE1} = 0/1.8 V, V_{MODE2} = 0 V		
Battery Current	-	1	2	mA	through V_{BATT} pin, V_{MODE1} = 0/1.8 V, V_{MODE2} = 0 V		
Enable Current	-	<0.1	0.15	mA	through V_{EN_CELL} pin		
Total Decoder Current on V_{BATT} (in Shutdown mode)	-	7	16	µA	V_{BATT} = +4.2 V, V_{CC} = +4.2 V, V_{EN_CELL} = 0 V, V_{MODE1} = 0 V, V_{MODE2} = 0 V		
Total PA Leakage Current on V_{CC} (in Shutdown mode)	-	1	5	µA	V_{BATT} = +4.2 V, V_{CC} = +4.2 V, V_{EN_CELL} = 0 V, V_{MODE1} = 0 V, V_{MODE2} = 0 V		
Noise in Receive Band(2)	- -	-133 -137	-131 -134	dBm/Hz	V_{MODE1} = 0 V, V_{MODE2} = 1.8 V V_{MODE1} = V_{MODE2} = 1.8 V		
Harmonics 2fo 3fo, 4fo	- -	-41 -50	-30 -30	dBc	P_{OUT} ≤ +27.9 dBm		
Input Impedance	-	-	2:1	VSWR			
Coupling Factor	-	22	-	dB			

Table 5b: Electrical Specifications - PCS Band (BC 1)
(T_C = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{EN_PCS} = +1.8 V, 50 Ω system, CDMA2000 RC-1 waveform)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					V_{MODE1}	V_{MODE2}	P_{OUT}
Spurious Output Level (all spurious outputs)	-	-	-65	dBc	$P_{OUT} \leq$ +27.9 dBm In-band Load VSWR < 5:1 Out-of-band Load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating conditions		

Notes:
(1) ACPRs and Efficiency measured at 1880 MHz.
(2) 1930 MHz to 1990 MHz.

APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: http://www.anadigics.com

Shutdown Mode

The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the V_{ENABLE} and V_{MODE} voltages.

Bias Modes

The power amplifier may be placed in Low, Medium or High Bias modes by applying the appropriate logic level (see Operating Ranges table) to the $V_{MODE1,}$ and V_{MODE2} pins. The Bias Control table lists the recommended modes of operation for various applications.

Table 6: Bias Control

APPLICATION	P_{OUT} LEVELS	BIAS MODE	V_{EN}	V_{MODE1}	V_{MODE2}	V_{CC}	V_{BATT}
CDMA - low power (Low Bias Mode)	≤ +10 dBm	Low	+1.8 V	-	0 V	3.2 - 4.2 V	≥ 3.2 V
CDMA - med power (Medium Bias Mode)	> 8 dBm ≤ +16 dBm	Med	+1.8 V	+1.8 V	+1.8 V	3.2 - 4.2 V	≥ 3.2 V
CDMA - high power (High Bias Mode)	> +16 dBm	High	+1.8 V	0 V	+1.8 V	3.2 - 4.2 V	≥ 3.2 V
Shutdown	-	Shutdown	0 V	0 V	0 V	3.2 - 4.2 V	≥ 3.2 V

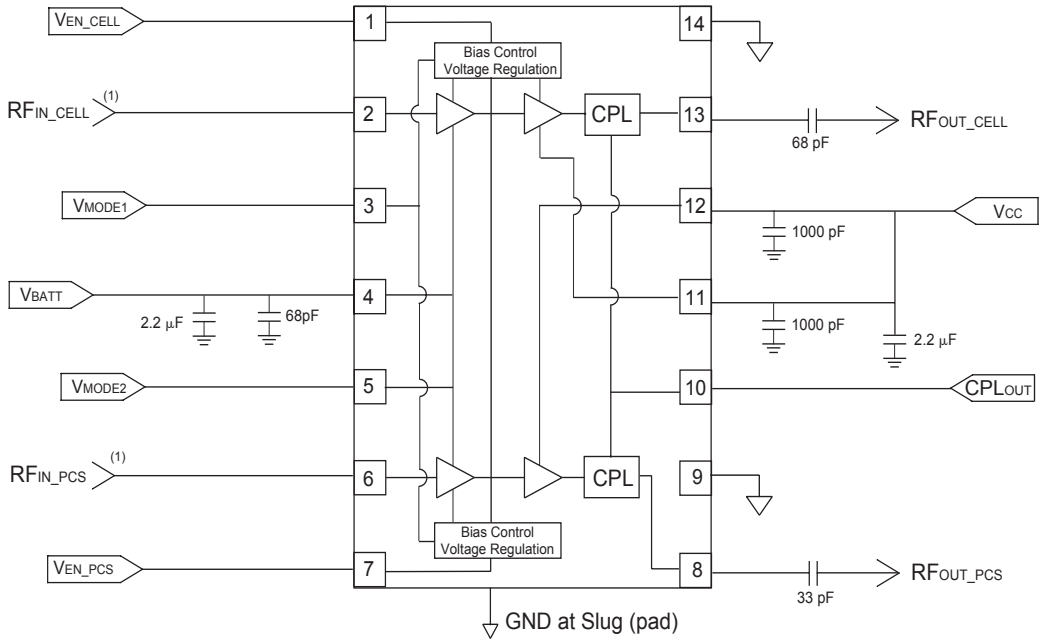
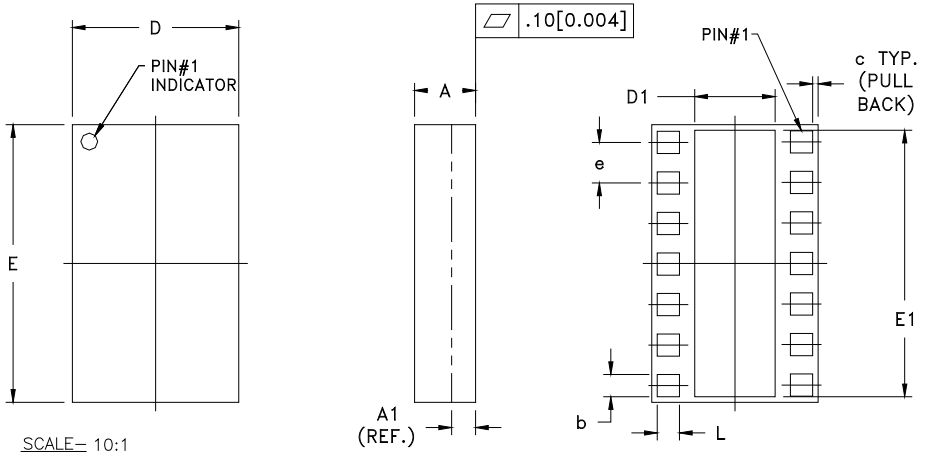


Figure 3: Application Circuit

Note:
(1) Add blocking cap if DC voltage is present on input pin.

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.91	1.03	1.13	0.035	0.041	0.044	–
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						–
b	0.32	0.37	0.41	0.013	0.015	0.016	3
c	–	0.10	–	–	0.004	–	–
D	2.88	3.00	3.12	0.113	0.118	0.123	–
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	4.88	5.00	5.12	0.192	0.197	0.202	–
E1	4.70	4.75	4.80	0.185	0.187	0.189	3
e	–	0.73	–	–	0.029	–	4
L	0.32	0.37	0.41	0.013	0.015	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. PITCH MEASUREMENT (e) TAKEN CENTERLINE TO CENTERLINE OF SOLDER MASK OPENINGS.
5. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

Figure 4: Package Outline - 14 Pin 3 mm x 5 mm x 1 mm Surface Mount Module

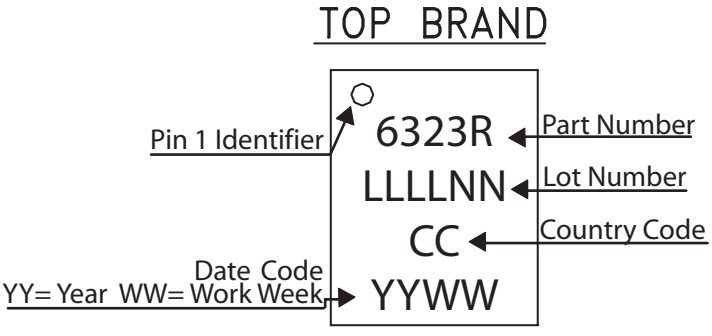


Figure 5: Branding Specification

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWC6323RM47Q7	-30 °C to +90 °C	RoHS Compliant 14 Pin 3 mm x 5 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
AWC6323RM47P9	-30 °C to +90 °C	RoHS Compliant 14 Pin 3 mm x 5 mm x 1 mm Surface Mount Module	Partial Tape and Reel

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