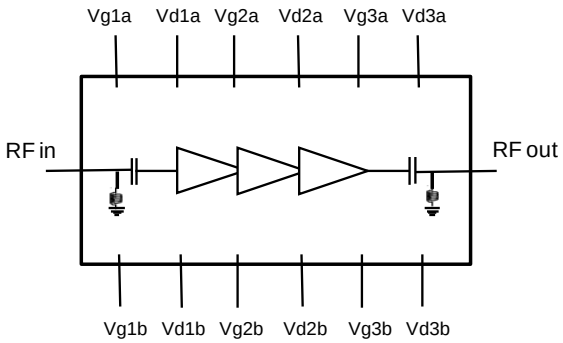
27-31.5GHz High Power Amplifier

GaAs Monolithic Microwave IC

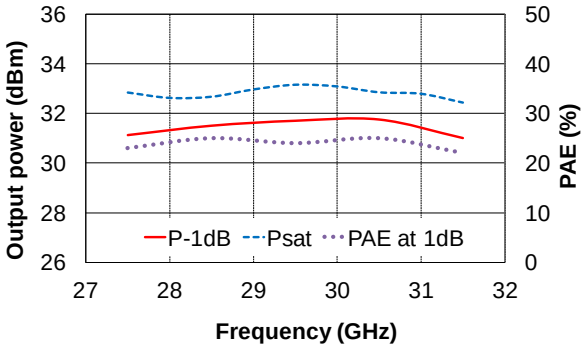
Description

The CHA6358-99F is a three stages monolithic HPA that typically provides an output power of 31dBm at 1dB gain compression associated to a high IP3 output of 38.5dBm.
It is designed for a wide range of applications, from professional to commercial communication systems
The circuit is manufactured with a pHEMT process, 0.15µm gate length.
It is available in chip form.



Main Features

- Broadband performances: 27-31.5GHz
- Pout: 31dBm at 1dB compression
- OIP3: 38.5dBm
- Linear gain: 22dB
- DC bias: Vd=6.0Volt@Id=750mA
- Chip size: 2.5x2.5x0.1mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.0		31.5	GHz
Gain	Linear Gain		22		dB
OIP3	Output third order interception point		38.5		dBm
Pout	Output Power @1dB comp.		31		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	27		31.5	GHz
G	Small Signal Gain		22		dB
ΔG	Gain variation in temperature		0.03		dB/°C
P1dB	Output power @1dB compression		31		dBm
Psat	Saturated output power		32.5		dBm
PAE	Power Added Efficiency at P-1dB		25		%
OIP3	Output IP3		38.5		dBm
Rlin	Input Return Loss		10		dB
Rlout	Output Return Loss		14		dB
Idq	Total quiescent drain current		750		mA

These values are representative of on test fixture measurements with a bonding wire of typically 0.2nH at the RF ports.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6.5V	V
Id	Drain bias current	1	A
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd	3, 5, 7, 9,11,13	DC drain voltage	6	V
Vg	2, 4, 6, 10,12,14	DC gate voltage (1)	-0.7	V

(1) To be adjusted in order to achieve Id: 750mA

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Typical on-wafer Sij parameters

Tamb.= +25°C, Vd = +6.0V, Id = 750mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
1.0	-0.551	158.5	-93.379	40.7	-86.551	-113.2	-0.111	172.1
2.0	-2.421	134.6	-80.802	36.0	-86.900	-144.4	-0.162	164.2
3.0	-6.244	50.0	-95.935	177.7	-88.285	109.0	-0.225	155.8
4.0	-5.974	-111.6	-87.556	47.8	-87.589	-66.7	-0.324	146.0
5.0	-3.426	-152.9	-66.555	100.3	-92.067	-61.2	-0.546	133.3
6.0	-2.867	-170.4	-52.616	75.1	-102.38	-144.5	-1.250	114.0
7.0	-2.828	178.8	-40.621	23.8	-91.666	2.1	-4.534	78.4
8.0	-3.021	171.3	-33.067	-52.5	-72.837	-56.7	-20.496	-78.2
9.0	-3.327	166.3	-31.038	-118.3	-69.331	-95.6	-5.781	-168.9
10.0	-3.589	163.4	-31.395	-163.1	-62.180	-125.4	-3.241	166.1
11.0	-3.635	162.0	-32.037	178.0	-59.603	-163.8	-2.554	150.2
12.0	-3.368	160.6	-28.808	178.5	-59.104	172.9	-2.487	138.1
13.0	-2.893	157.9	-21.731	162.5	-59.194	155.3	-2.776	128.3
14.0	-2.393	153.4	-14.255	123.8	-56.373	137.4	-3.230	122.2
15.0	-1.991	147.7	-8.702	66.2	-55.750	115.9	-2.989	118.4
16.0	-1.682	141.4	-6.401	7.2	-56.274	102.9	-2.480	109.1
17.0	-1.442	134.5	-5.552	-39.1	-57.430	96.8	-2.621	98.0
18.0	-1.264	127.2	-4.341	-76.3	-54.554	88.8	-2.979	88.5
19.0	-1.149	119.2	-2.418	-111.8	-54.508	73.7	-3.261	79.6
20.0	-1.061	110.9	-0.318	-147.2	-55.451	65.1	-3.435	70.0
21.0	-0.918	101.7	2.131	178.1	-51.757	56.1	-3.561	59.1
22.0	-0.803	90.7	5.002	143.2	-51.993	28.0	-3.748	46.3
23.0	-0.658	78.0	8.590	106.8	-52.168	10.5	-4.052	31.5
24.0	-0.451	61.5	12.909	65.5	-54.026	-22.3	-4.595	14.1
25.0	-0.388	37.6	17.935	14.9	-56.156	-52.4	-5.716	-6.8
26.0	-1.662	0.7	22.522	-52.5	-66.692	-122.4	-8.214	-28.5
27.0	-6.795	-39.2	24.359	-129.3	-56.327	50.9	-11.960	-42.7
28.0	-14.855	-60.3	24.154	160.6	-52.705	-4.2	-17.273	-46.0
29.0	-25.338	-66.4	23.474	97.1	-50.758	-62.8	-18.844	7.9
30.0	-26.446	-4.4	22.423	38.1	-50.015	-118.0	-11.658	4.0
31.0	-21.698	-80.9	22.228	-17.1	-50.967	-173.5	-9.521	-23.2
32.0	-20.535	-144.6	21.813	-82.9	-47.172	114.4	-8.751	-45.9
33.0	-14.861	-154.9	20.492	-145.5	-46.708	41.9	-6.933	-63.9
34.0	-8.473	155.7	18.753	143.5	-52.160	-40.9	-5.818	-99.1
35.0	-7.509	105.6	14.728	76.2	-56.905	-61.2	-5.726	-130.4
36.0	-8.251	64.3	10.002	19.2	-63.017	-116.2	-5.949	-161.3
37.0	-9.279	25.2	5.374	-30.8	-62.276	-88.4	-5.786	167.6
38.0	-9.981	-15.4	1.158	-77.1	-58.178	-159.0	-5.520	138.3
39.0	-9.806	-55.2	-2.819	-123.3	-64.498	99.0	-4.647	110.3
40.0	-8.620	-91.1	-7.022	-168.7	-63.483	-43.2	-3.614	82.0
41.0	-7.246	-120.3	-11.373	146.9	-55.962	-162.4	-2.604	55.0
42.0	-5.933	-145.4	-16.083	103.7	-56.607	166.0	-1.859	29.8
43.0	-4.769	-167.5	-20.978	64.5	-55.999	144.9	-1.434	6.3
44.0	-3.968	172.7	-26.079	30.1	-55.080	133.1	-1.322	-14.6
45.0	-3.215	156.1	-31.492	-1.9	-51.391	144.6	-1.471	-32.5

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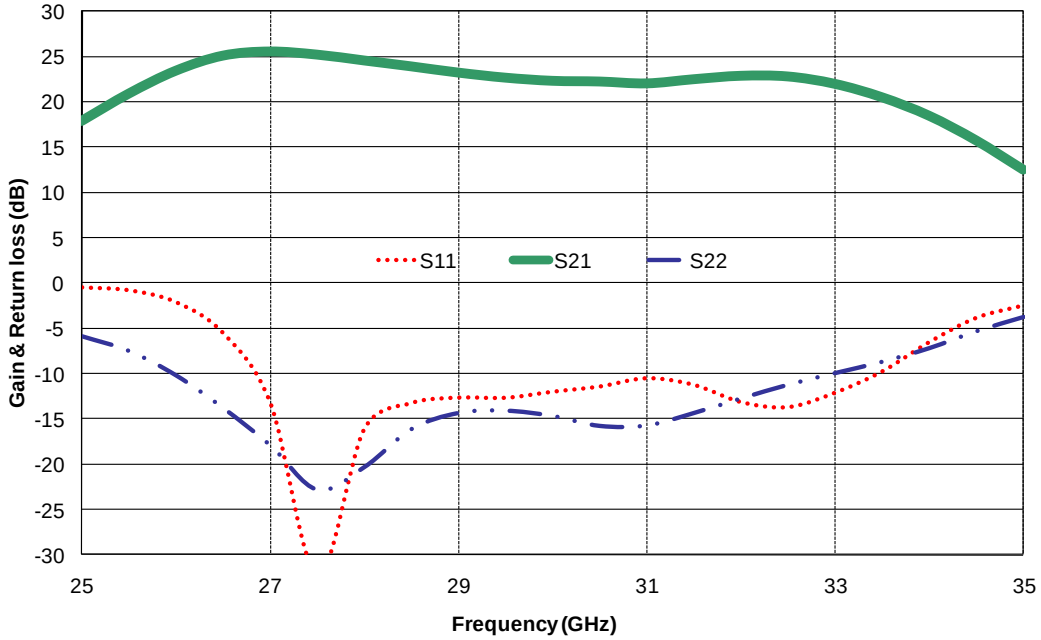
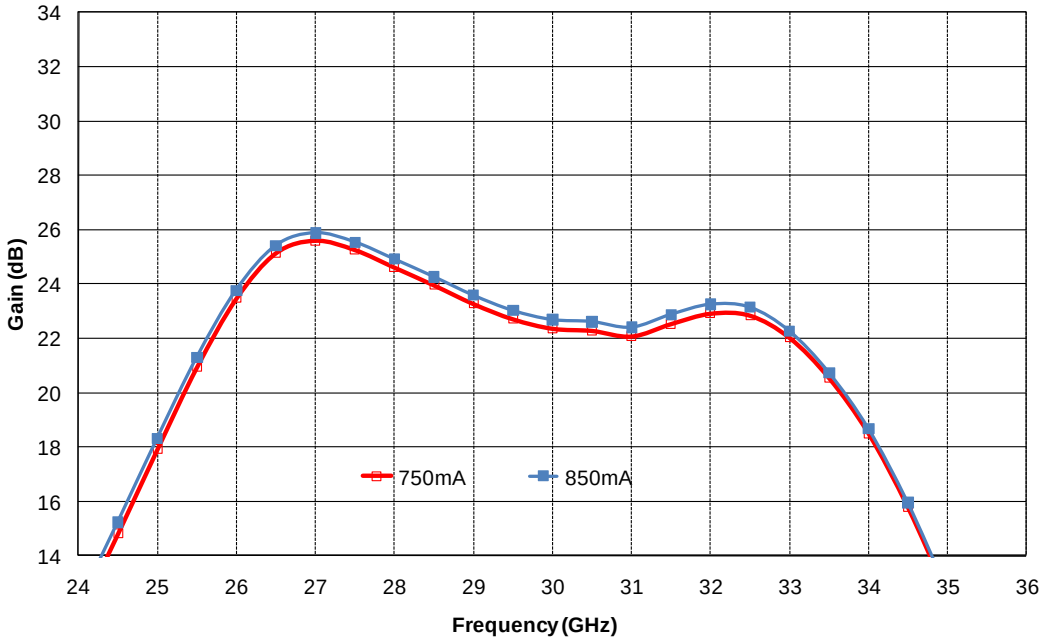
Typical Test fixture Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 750mA
These values are representative of on test fixture measurements with a bonding wire of typically 0.2nH at the RF ports.

Linear Gain & Return losses versus Frequency



Linear Gain versus Frequency & Idq



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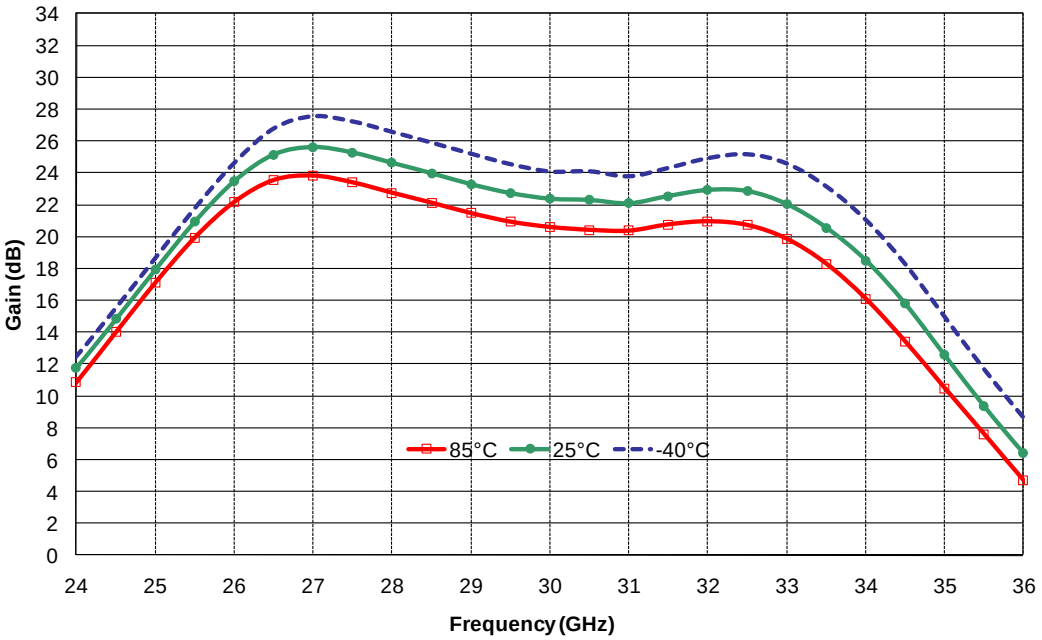
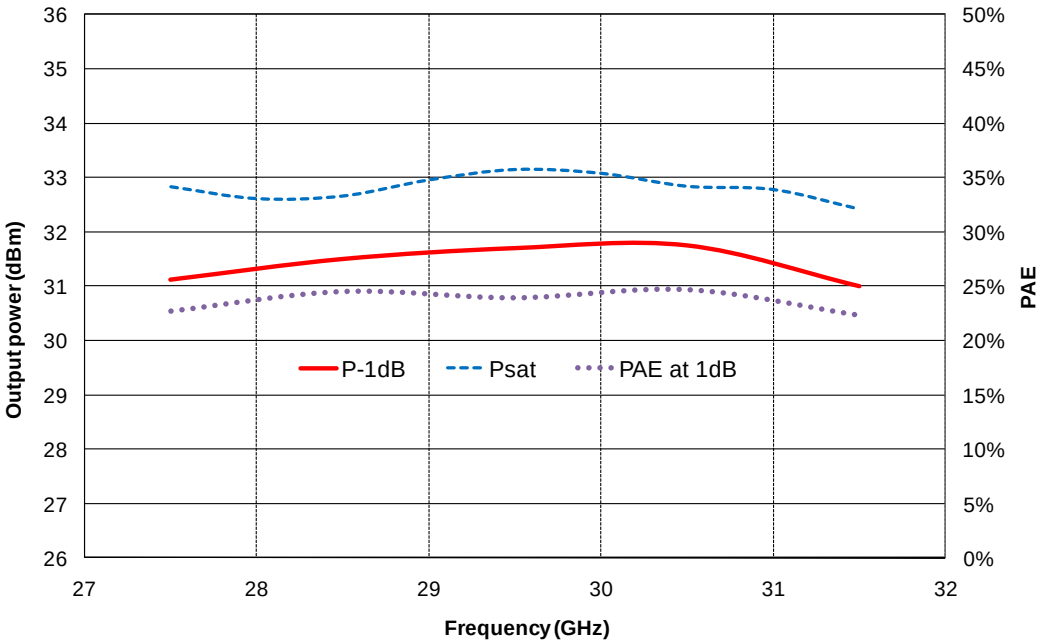
Typical Test fixture Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 750mA

Linear Gain versus Frequency &Temperature



Output Power & PAE versus Frequency



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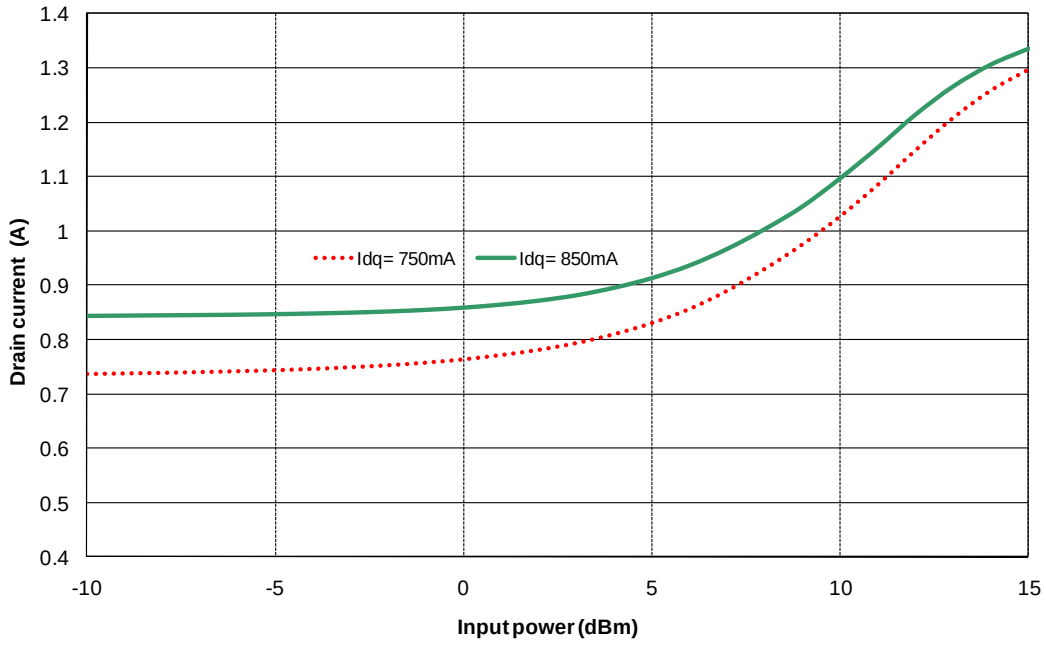
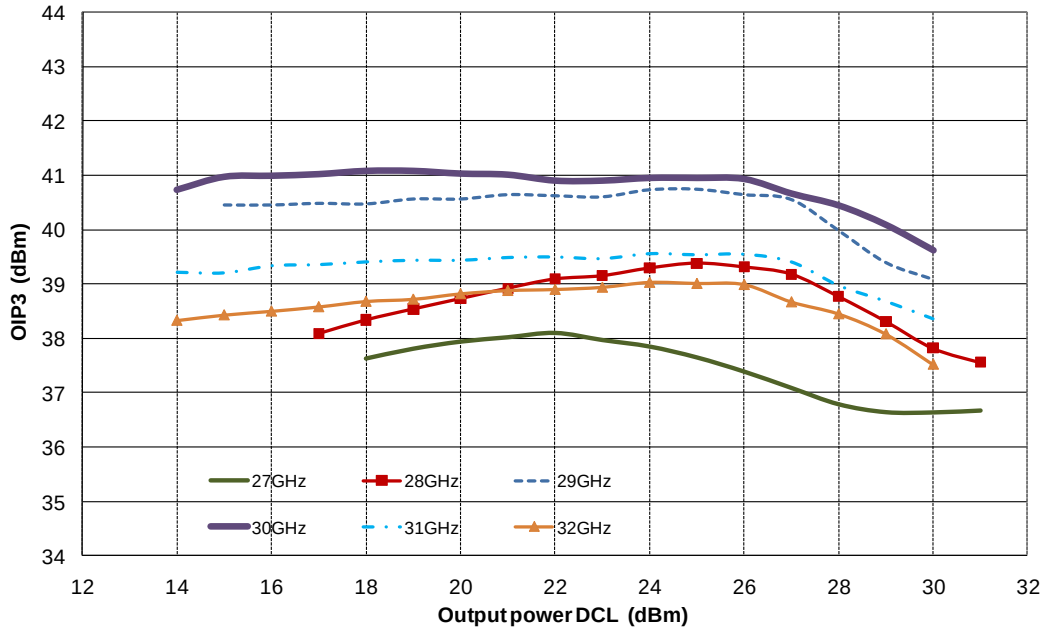
Typical Test fixture Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 750mA

Drain current versus input Power & Id quiescent



Output IP3 versus Pout DCL & Frequency



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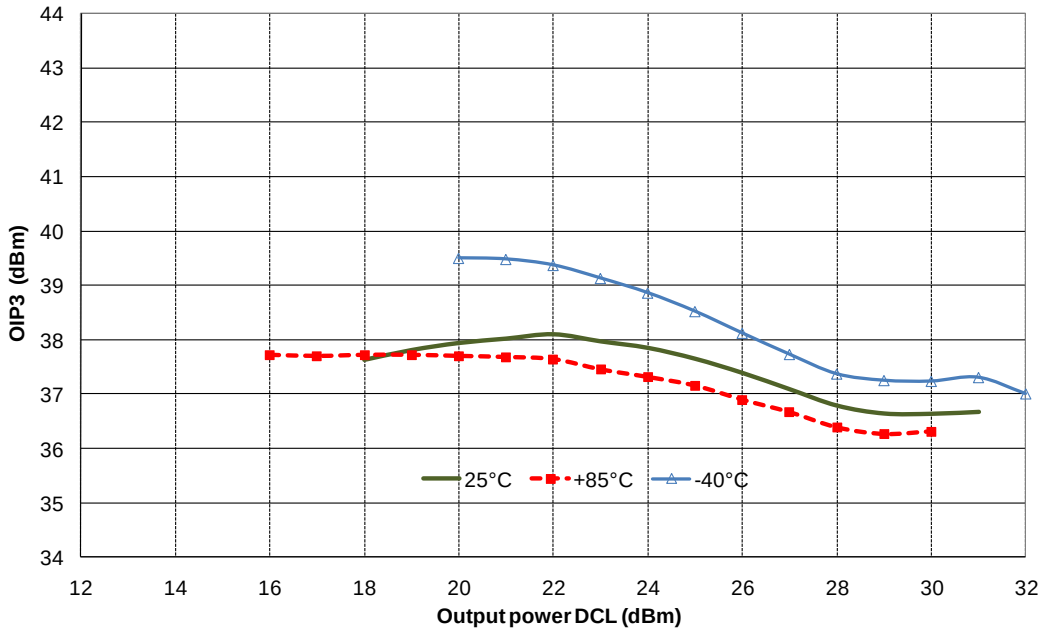
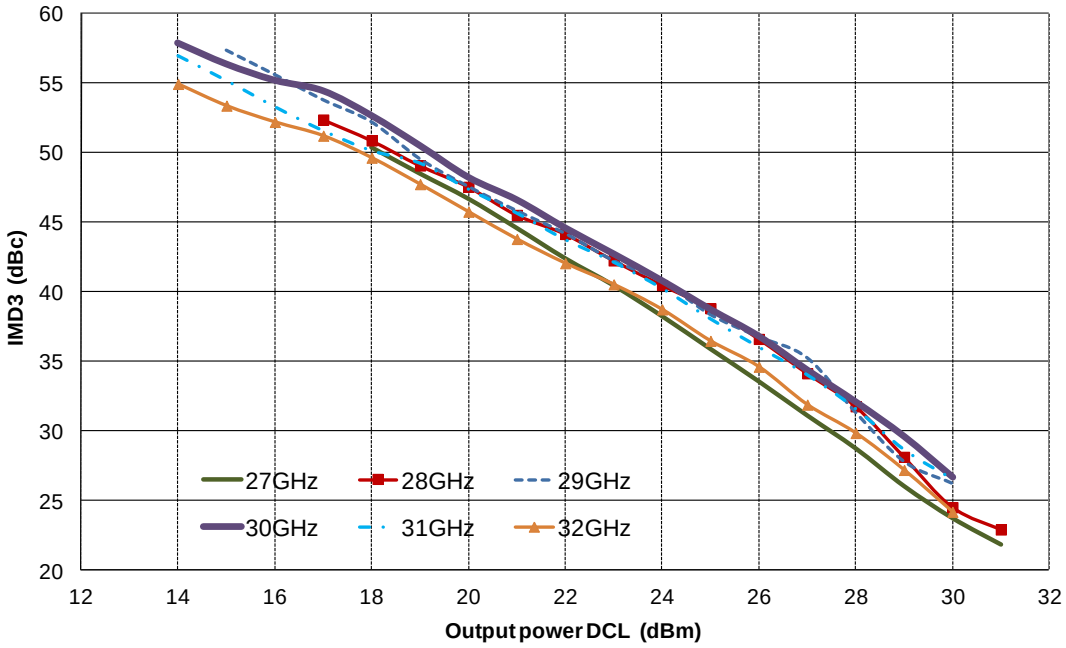
Typical Test fixture Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 750mA

Output IP3 versus Pout DCL & Temperature
Freq = 27GHz



IMD3 versus Pout DCL & Frequency



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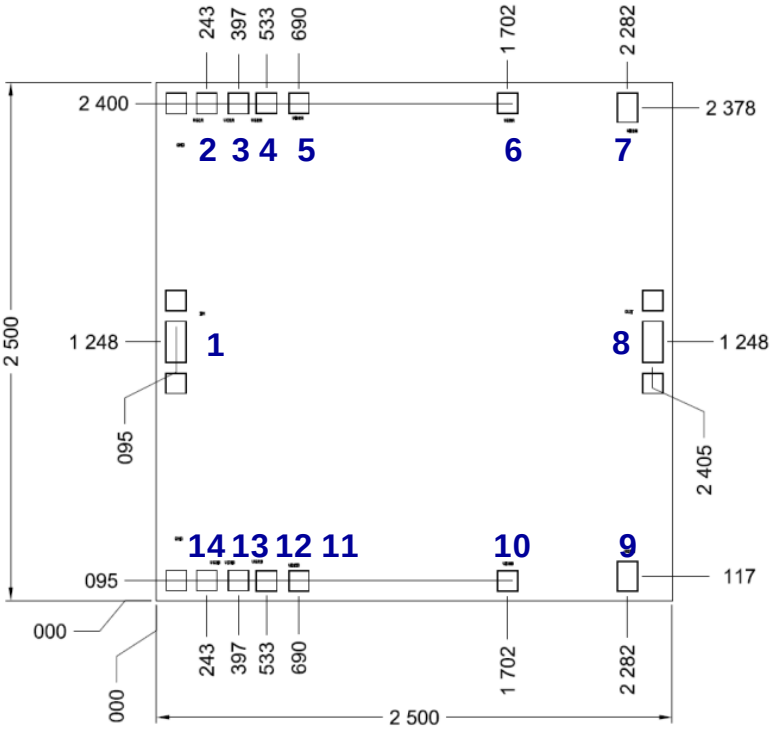
Mechanical data



Chip thickness: 100µm.
Chip size: 2500x2500 ±35µm
All dimensions are in micrometers

Pin number	Pin name	Description
1	IN	RF in
2,14	VG1A, VG1B	Gate Stage1
3,13	VD1A, VD1B	Drain stage1
4,12	VG2A, VG2B	Gate Stage2
5, 11	VD2A, VD2B	Drain stage2
6, 10	VG3A, VD3B(1)	Gate Stage3
7, 9	VD3A, VG3B(2)	Drain stage3
8	OUT	RF out

(1) *VD3B is the label on the die pad, corresponding to gate access on the 3rd stage*
(2) *VG3B is the label on the die pad, corresponding to drain access on the 3rd stage*

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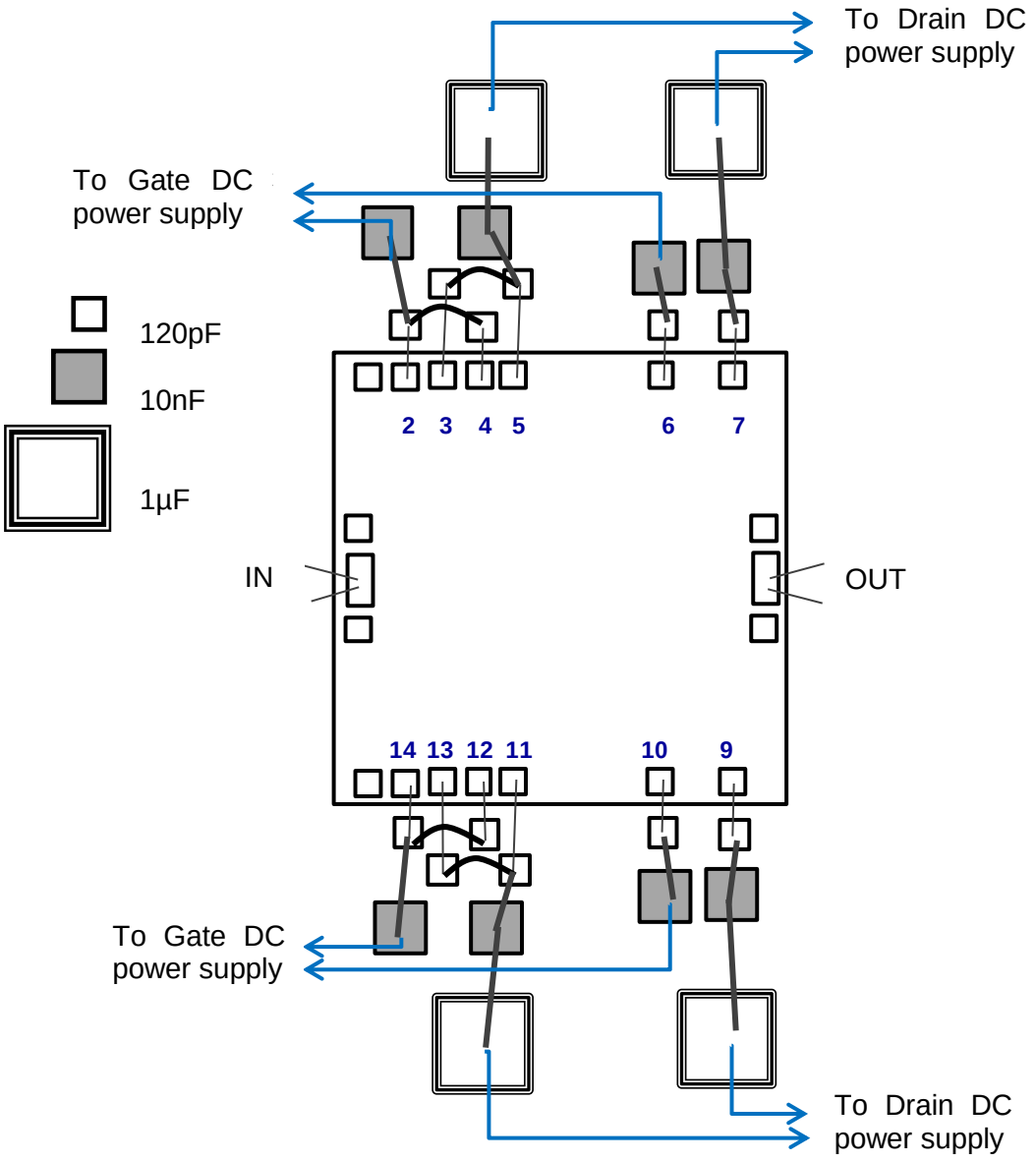
Recommended assembly plan



- For best thermal and electrical performances, chip should be brazed on a metal base plate.
- 2 wedge bonding, 25µm diameter, is preferred, with a maximum length of 300µm for RF IN and OUT.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
IN, OUT	RF	Not required	Maximum 300µm length with a wire diameter of 25 µm
VDxy	Vd	120pF, 10nF, 1µF	Drain Supply
VGxy	Vg	120pF, 10nF, 1µF	Gate Supply

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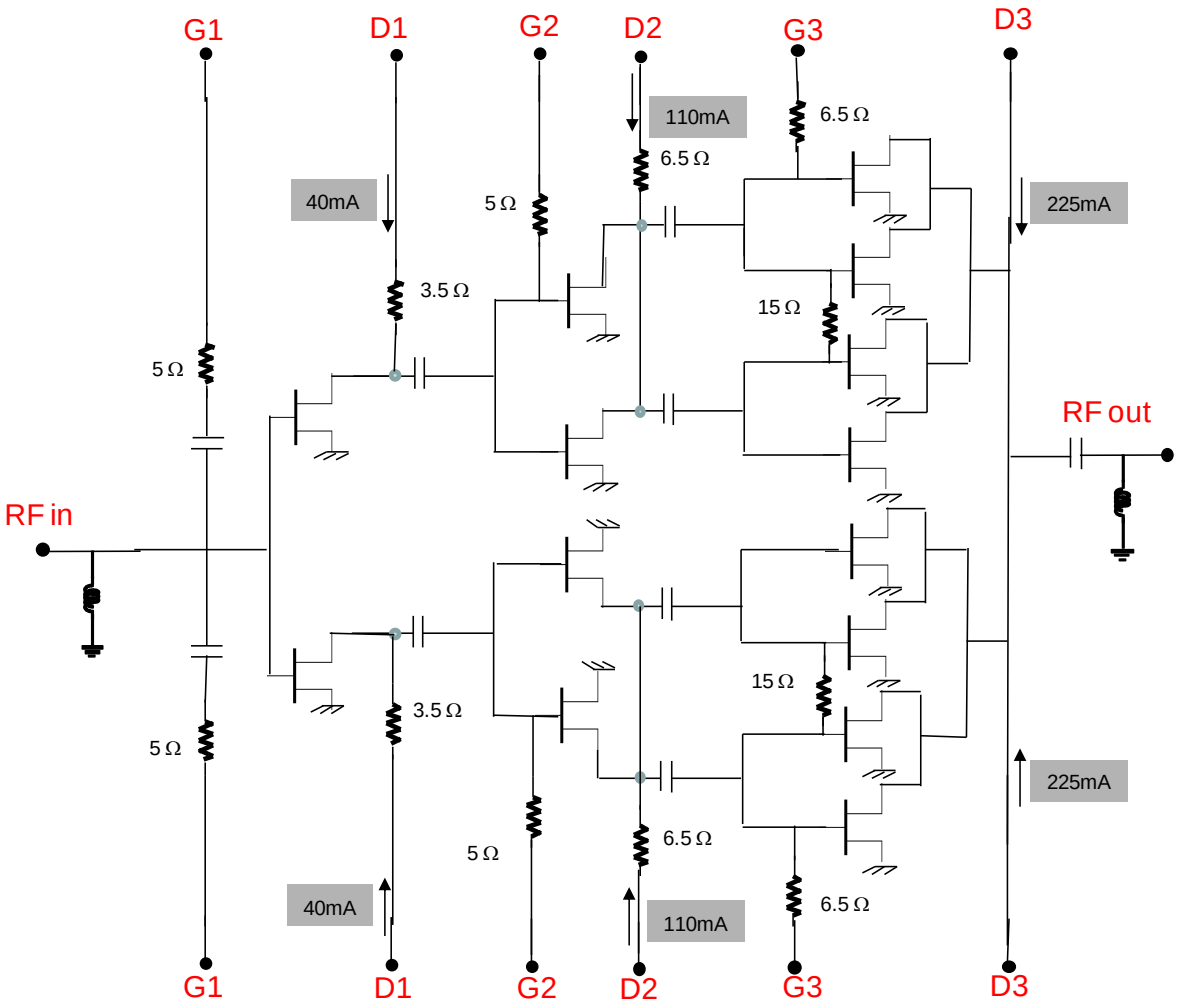
DC Schematic

6V, 750mA



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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Chip form:	CHA6358-99F/00

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