TGA2595-CP

27.5 to 31 GHz, 8 W GaN Power Amplifier

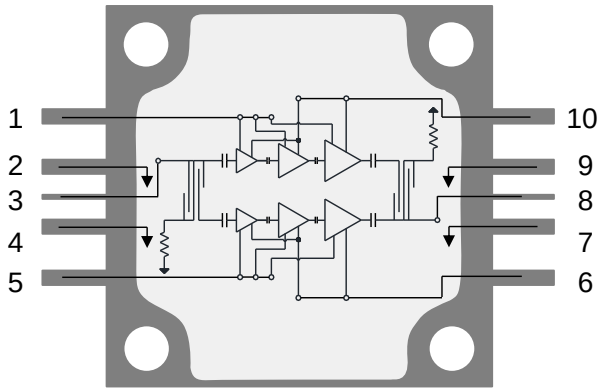
Applications

- Satellite Communications

Product Features

- Frequency Range: 27.5 - 31 GHz
- Pout: 39 dBm (P_{IN} = 18 dBm)
- PAE: > 22 % (P_{IN} = 18 dBm)
- Power Gain: 21 dB (P_{IN} = 18 dBm)
- IM3 @ 30 dBm/Tone = −27 dBc
- IM5 @ 30 dBm/Tone = −46 dBc
- Bias: V_D = 20 V, I_{DQ} = 560 mA, V_G = −2.5 V typical
- Package Dimensions: 15.2 x 15.2 x 5.2 mm
- Package base is pure Cu offering superior thermal management

Functional Block Diagram



General Description

TriQuint's TGA2595-CP is a balanced Ka-Band power amplifier fabricated on TriQuint's TQGaN15 0.15 um GaN on SiC process. The balanced configuration supports low return loss and improves robustness into non-ideal loads. Operating from 27.5 to 31 GHz, the TGA2595-CP achieves 39 dBm saturated output power with power-added efficiency of > 22 % and power gain of 21 dB.

The TGA2595-CP is packaged in a 10-lead 15x15 mm bolt-down package with a Cu base for superior thermal management. To simply system integration, the TGA2595-CP is fully matched to 50 ohms with integrated DC blocking capacitors on both I/O ports.

The TGA2595-CP is ideally suited for both commercial and defense satellite communications.

Lead free and RoHS compliant.

Evaluation Boards are available upon request.

Pin Configuration

Pad No.	Symbol
1, 5	V_G
2, 4, 7, 9	GND
3	RF_{IN}
6, 10	V_D
8	RF_{OUT}

Ordering Information

Part	ECCN	Description
TGA2595-CP	3A001.b.2.c	27.5 - 31 GHz, 8 W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	23 V
Gate Voltage Range (V_G)	−5 to 0 V
Drain Current (I_D)	2.8 A
Gate Current (I_G)	−6 to 34 (1) mA
Power Dissipation (P_{DISS}), 85°C	48 W
Input Power, CW, 50 Ω, (P_{IN})	30 dBm
Input Power, CW, VSWR 6:1, V_D = 22 V, 85 °C, (P_{IN})	25 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

(1) Max rating for I_G is at Channel Temperature (T_{CH}) of 200 °C .

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D): Pulsed	20 V
Drain Current (I_{DQ})	560 mA
Drain Current Under RF Drive (I_{D_DRIVE})	See plots p. 6
Gate Voltage (V_G)	−2.5 V (Typ.)
Gate Current Under RF Drive (I_{G_DRIVE})	See plots p. 6
Temperature (T_{BASE})	−40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25 °C, V_D = 20 V, I_{DQ} = 560 mA, V_G = -2.5 V typical.

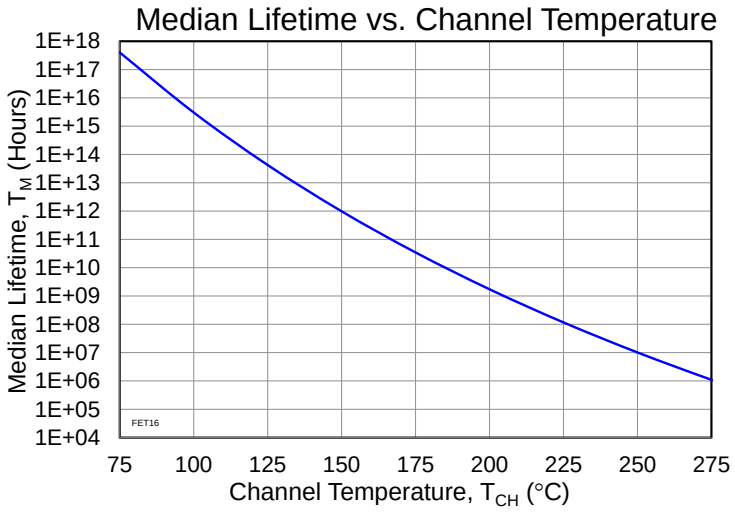
Parameter	Min	Typical	Max	Units
Operational Frequency Range	27.5		31	GHz
Small Signal Gain		> 25		dB
Input Return Loss		> 12		dB
Output Return Loss		> 13		dB
Output Power (at P_{IN} = 18 dBm)		39		dBm
Power Added Efficiency (at P_{IN} = 18 dBm)		> 22		%
Power Gain (at P_{IN} = 18 dBm)		21		dB
IM3 @ 30 dBm/Tone		−27		dBc
IM5 @ 30 dBm/Tone		−46		dBc
Output Power Temperature Coefficient (25 °C to 85 °C only)		−0.01		dBm/°C
Recommended Operating Voltage		20	22	V

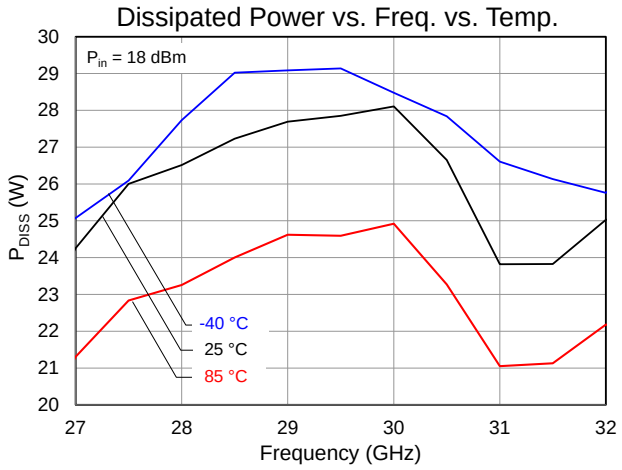
Thermal and Reliability Information

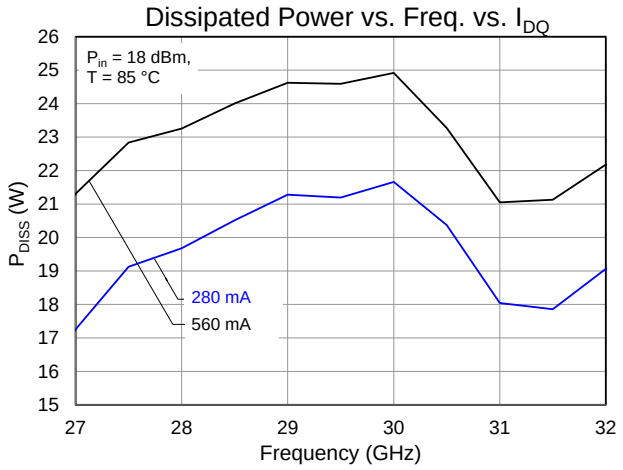
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	CW, V_D = 20 V, I_{DQ} = 560 mA, T_{BASE} = 85°C P_{DISS} =11.2 W	3.3	°C/W
Channel Temperature (T_{CH}) (Quiescent)		125	°C
Median Lifetime (T_M)		4.0E+13	Hrs
Thermal Resistance (θ_{JC}) (1)	V_D = 20 V, I_{DQ} = 280 mA, T_{BASE} = 85°C, Freq = 29 GHz, P_{IN} = 18 dBm, P_{OUT} = 37.9 dBm, P_{DISS} =21.2 W, I_{D_Drive} = 1.37 A	3.61	°C/W
Channel Temperature (T_{CH}) (under RF drive)		170	°C
Median Lifetime (T_M)		5.9E+10	Hrs
Thermal Resistance (θ_{JC}) (1)	V_D = 20 V, I_{DQ} = 560 mA, T_{BASE} = 85°C, Freq = 29 GHz, P_{IN} = 18 dBm, P_{OUT} = 39.4 dBm, P_{DISS} =27.6 W, I_{D_Drive} = 1.81 A	3.76	°C/W
Channel Temperature (T_{CH}) (under RF drive)		197	°C
Median Lifetime (T_M)		2.2E+9	Hrs

Notes:
1. Thermal resistance measured to back of package.

Test Conditions: V_D = 22 V; Failure Criteria = 10% reduction in I_{D_MAX}



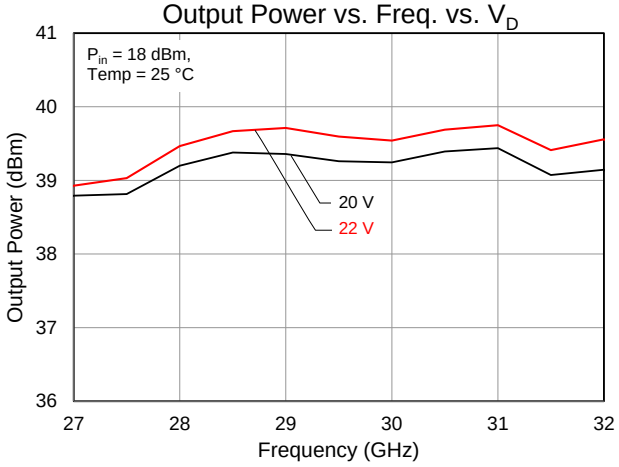




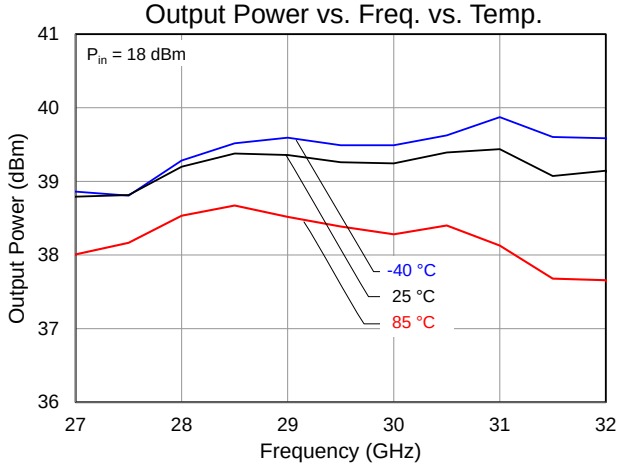
Typical Performance: Large Signal

Conditions unless otherwise specified: V_D = 20 V, I_{DQ} = 560 mA, V_G = -2.5 V typical, CW.

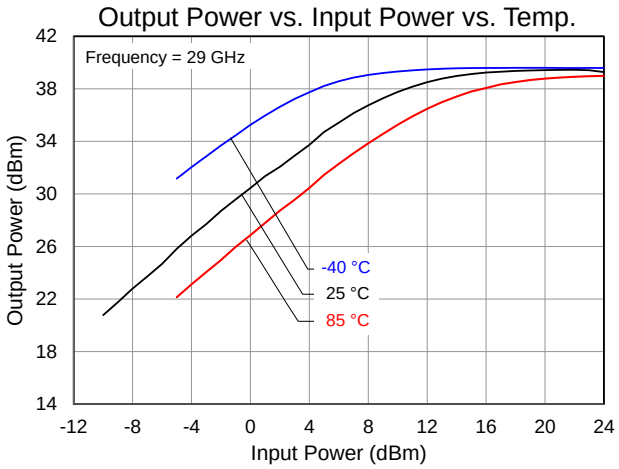
Output Power vs. Freq. vs. V_D



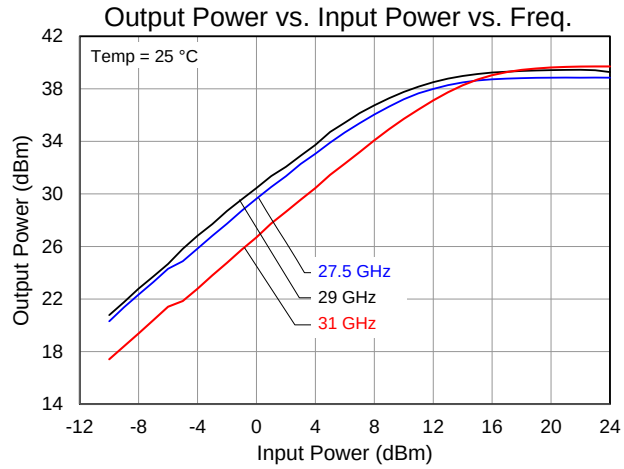
Output Power vs. Freq. vs. Temp.



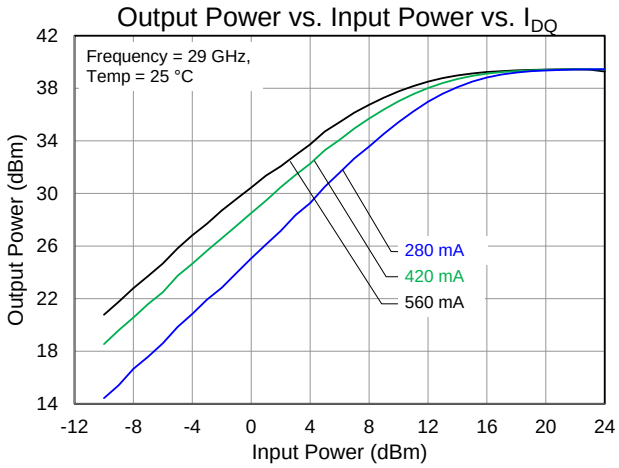
Output Power vs. Input Power vs. Temp.



Output Power vs. Input Power vs. Freq.



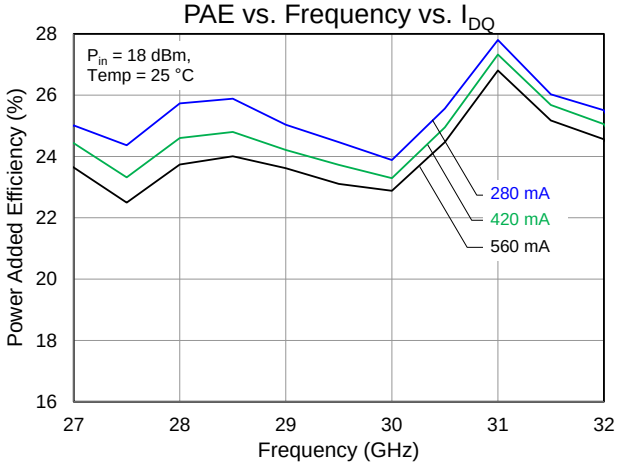
Output Power vs. Input Power vs. I_{DQ}



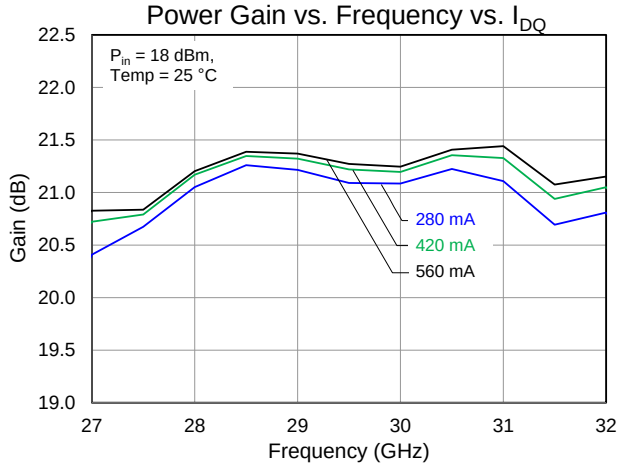
Typical Performance: Large Signal

Conditions unless otherwise specified: V_D = 20 V, I_{DQ} = 560 mA, V_G = -2.5 V typical, CW.

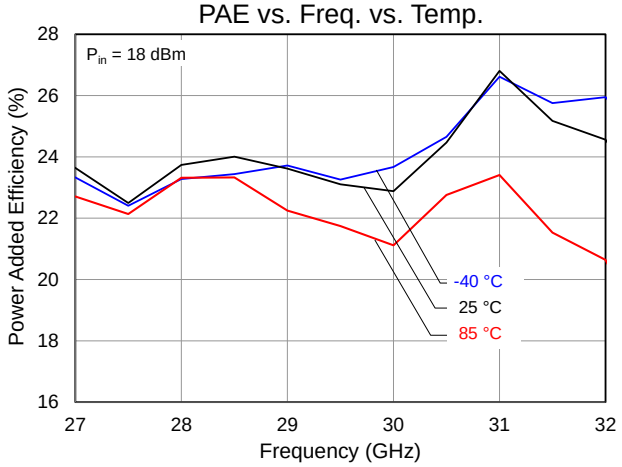
PAE vs. Frequency vs. I_{DQ}



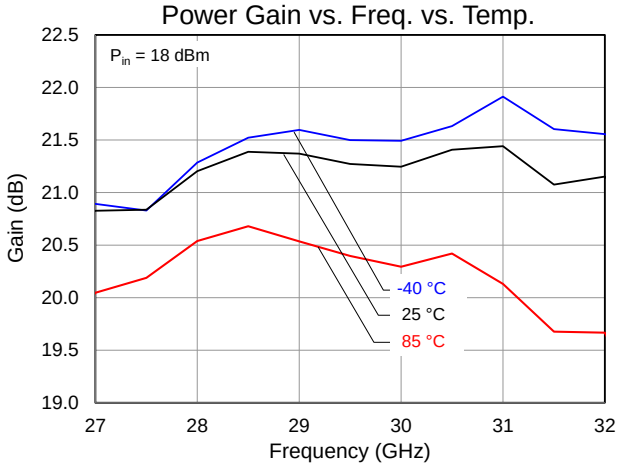
Power Gain vs. Frequency vs. I_{DQ}



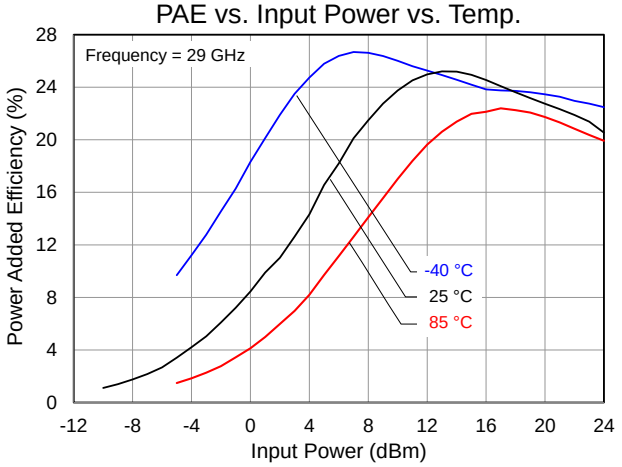
PAE vs. Freq. vs. Temp.



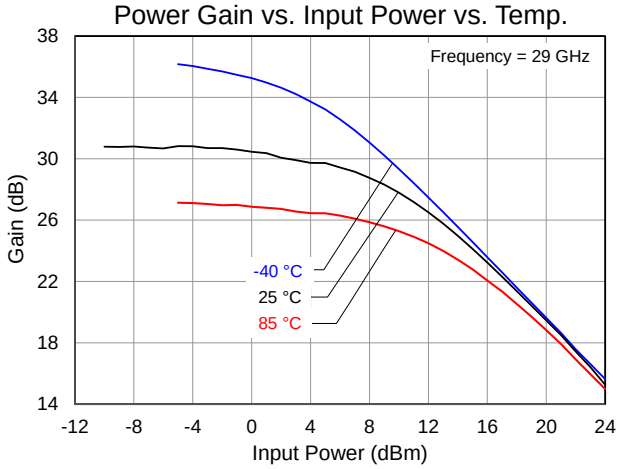
Power Gain vs. Freq. vs. Temp.



PAE vs. Input Power vs. Temp.



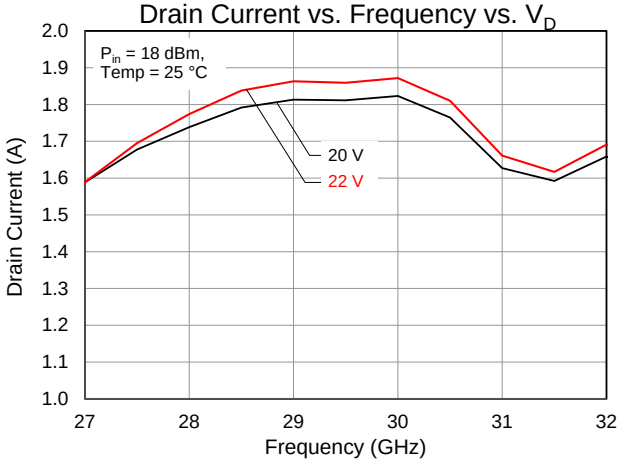
Power Gain vs. Input Power vs. Temp.



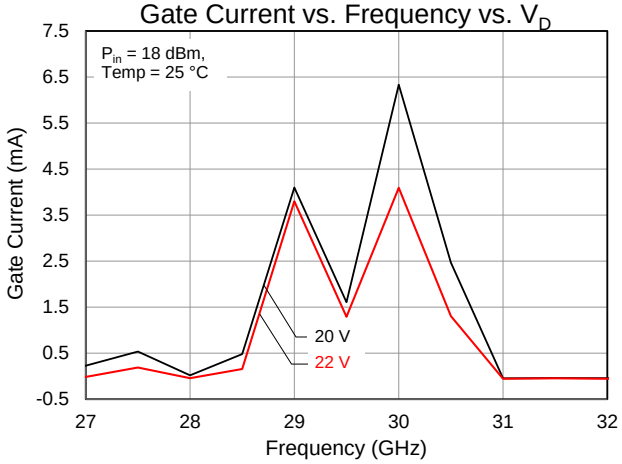
Typical Performance: Large Signal

Conditions unless otherwise specified: V_D = 20 V, I_{DQ} = 560 mA, V_G = -2.5 V typical, CW.

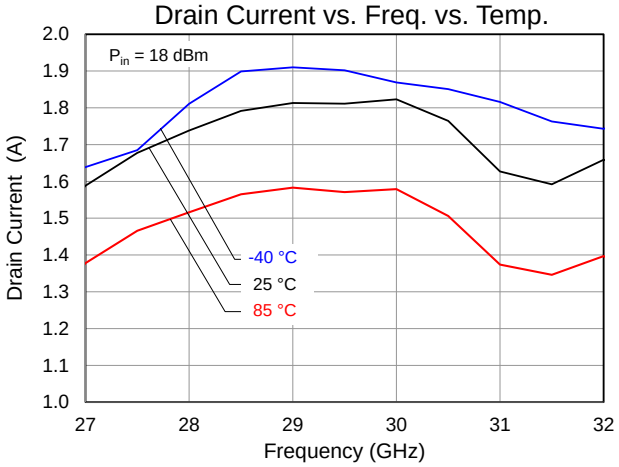
Drain Current vs. Frequency vs. V_D



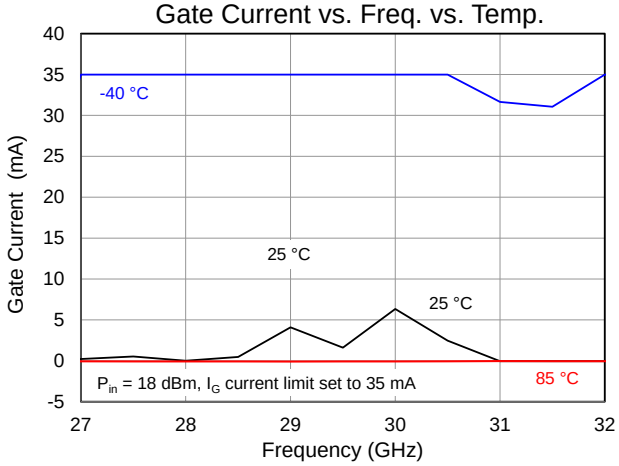
Gate Current vs. Frequency vs. V_D



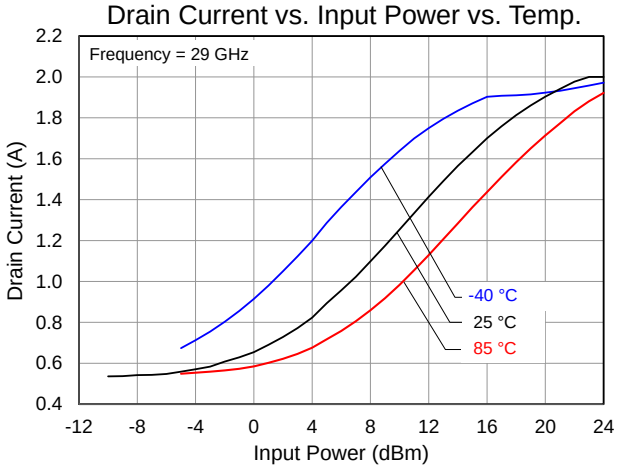
Drain Current vs. Freq. vs. Temp.



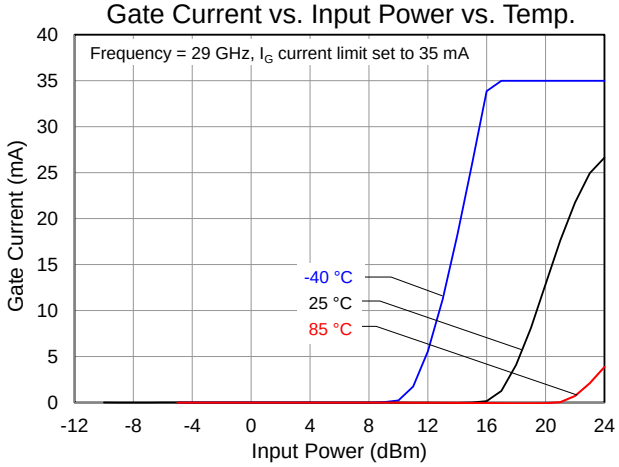
Gate Current vs. Freq. vs. Temp.



Drain Current vs. Input Power vs. Temp.



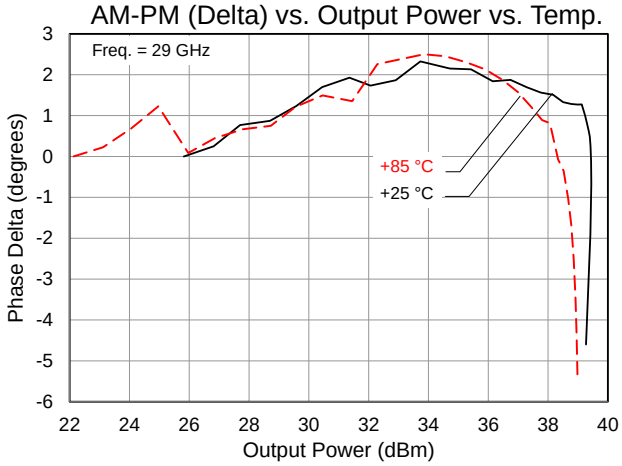
Gate Current vs. Input Power vs. Temp.



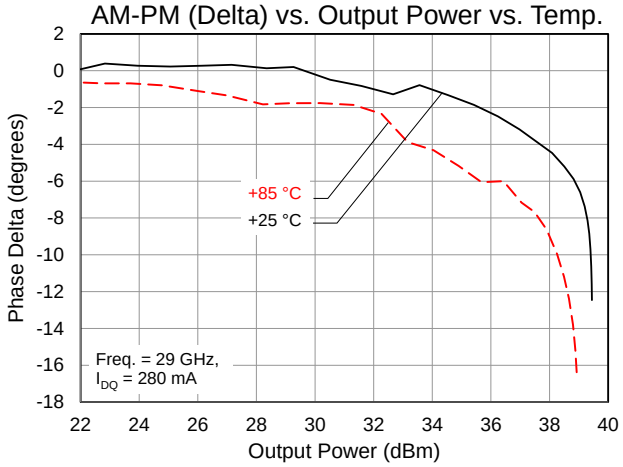
Typical Performance: Large Signal

Conditions unless otherwise specified: V_D = 20 V, I_{DQ} = 560 mA, V_G = -2.5 V typical, CW.

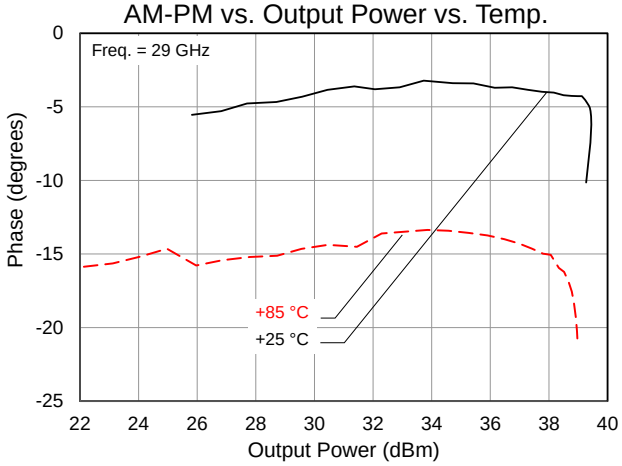
AM-PM (Delta) vs. Output Power vs. Temp.



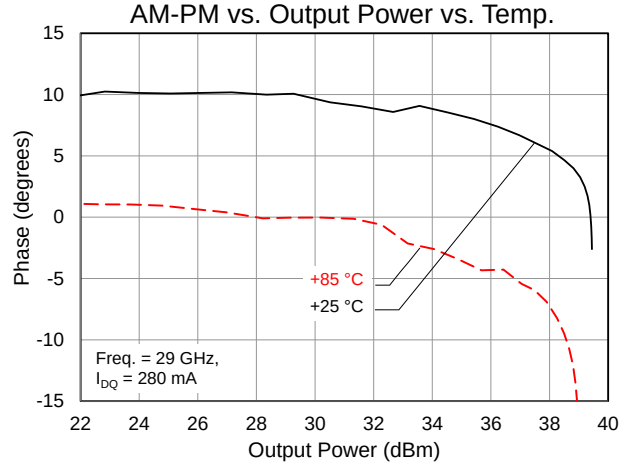
AM-PM (Delta) vs. Output Power vs. Temp.



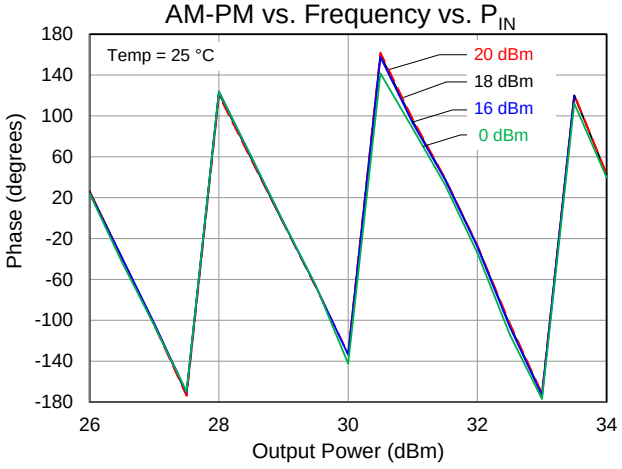
AM-PM vs. Output Power vs. Temp.



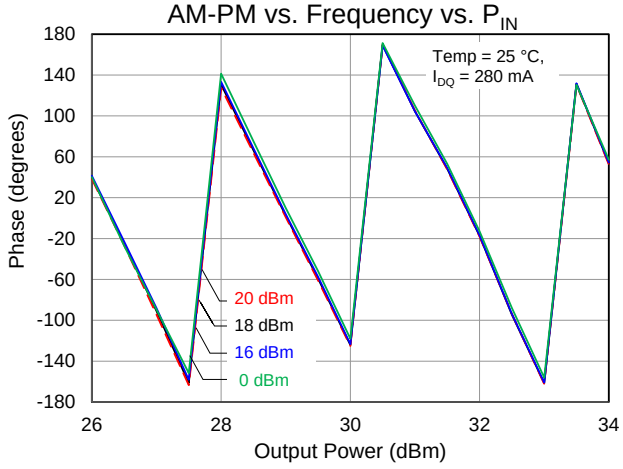
AM-PM vs. Output Power vs. Temp.



AM-PM vs. Frequency vs. P_{IN}



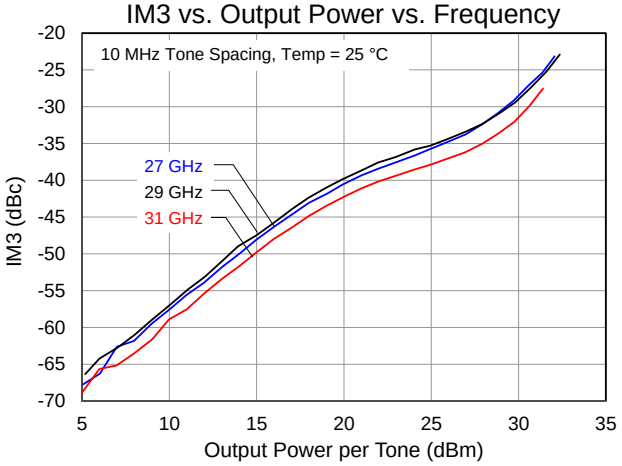
AM-PM vs. Frequency vs. P_{IN}



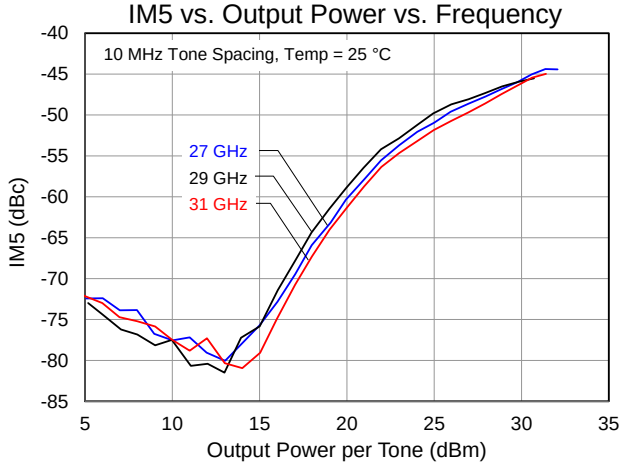
Typical Performance: Linearity

Conditions unless otherwise specified: V_D = 20 V, I_{DQ} = 560 mA, V_G = -2.5 V typical, CW.

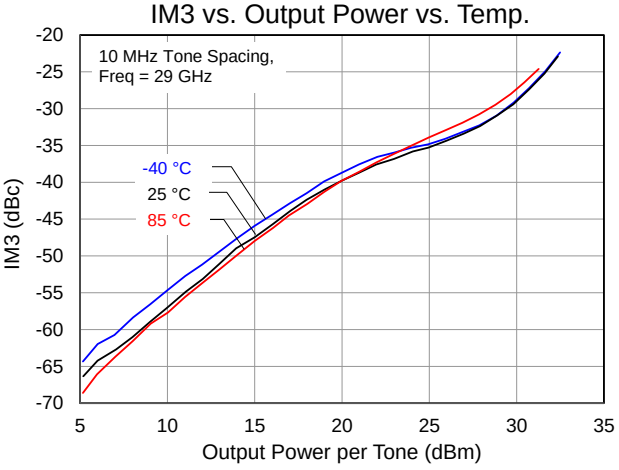
IM3 vs. Output Power vs. Frequency



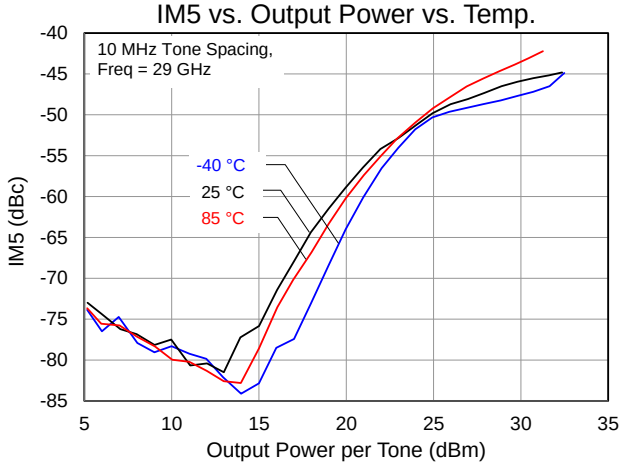
IM5 vs. Output Power vs. Frequency



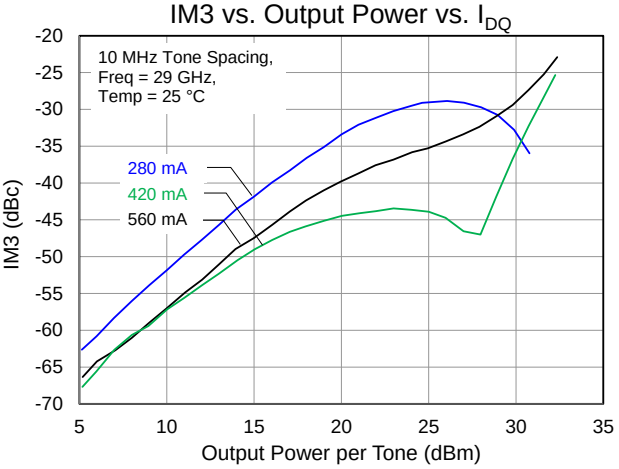
IM3 vs. Output Power vs. Temp.



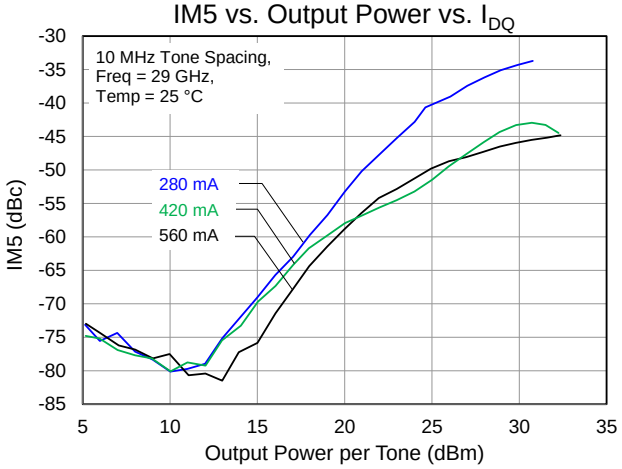
IM5 vs. Output Power vs. Temp.



IM3 vs. Output Power vs. I_{DQ}



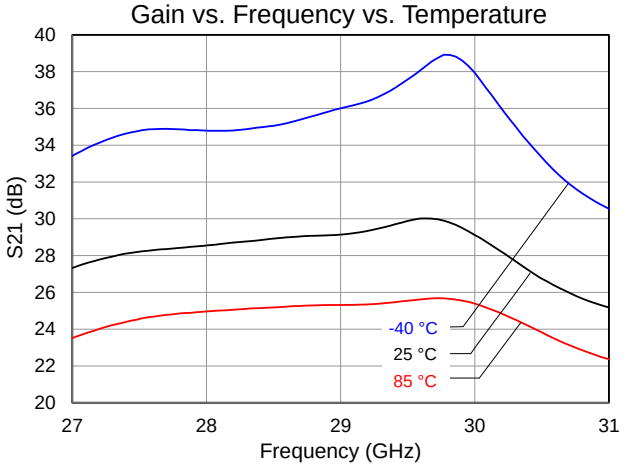
IM5 vs. Output Power vs. I_{DQ}



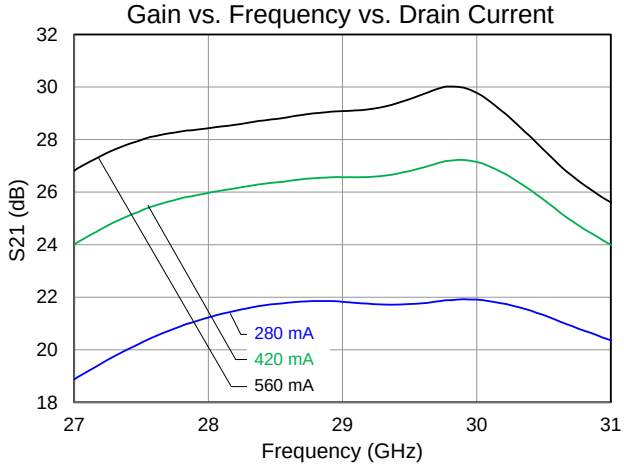
Typical Performance: Small Signal

Conditions unless otherwise specified: V_D = 20 V, I_{DQ} = 560 mA, V_G = -2.5 V typical, CW.

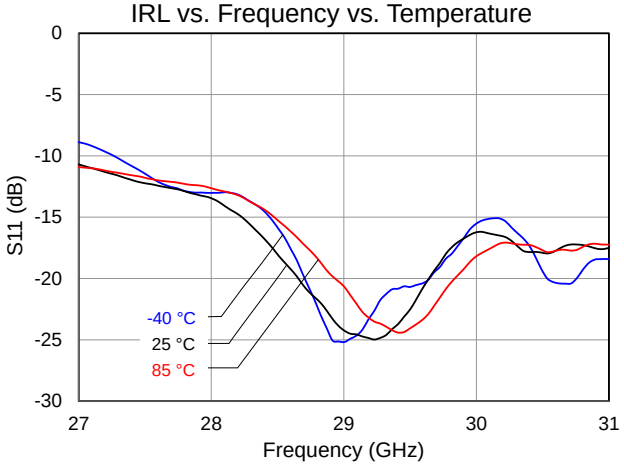
Gain vs. Frequency vs. Temperature



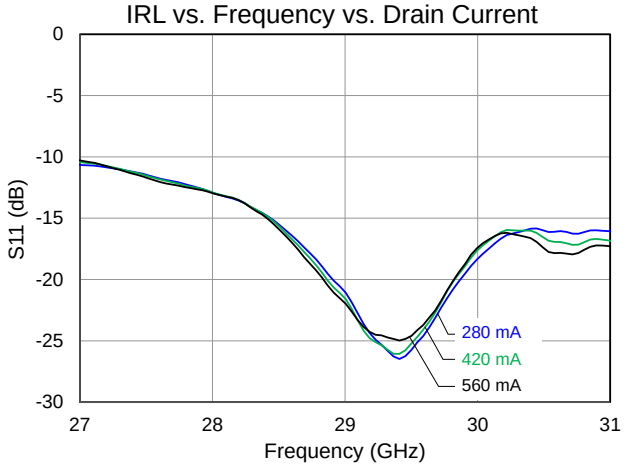
Gain vs. Frequency vs. Drain Current



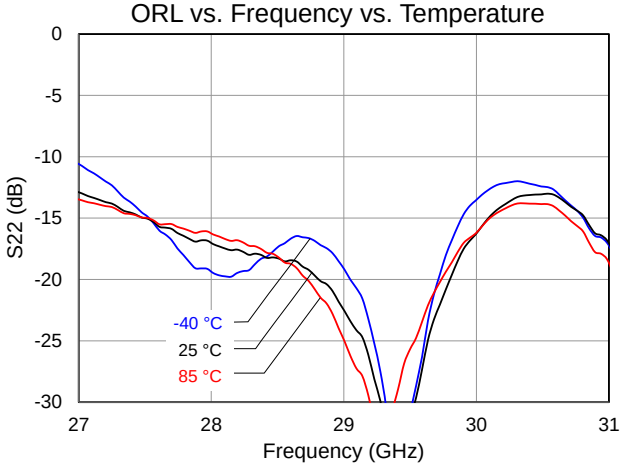
IRL vs. Frequency vs. Temperature



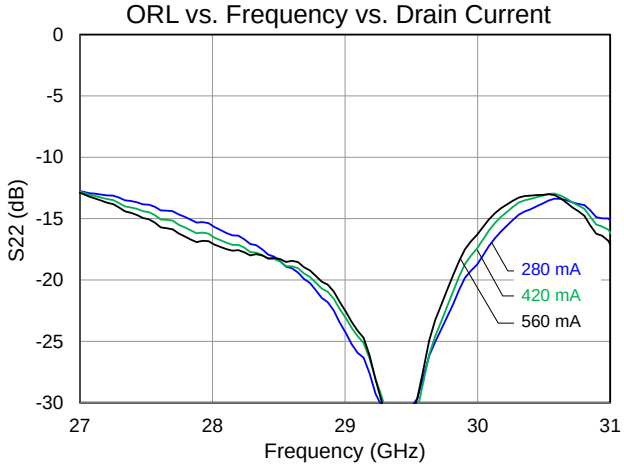
IRL vs. Frequency vs. Drain Current



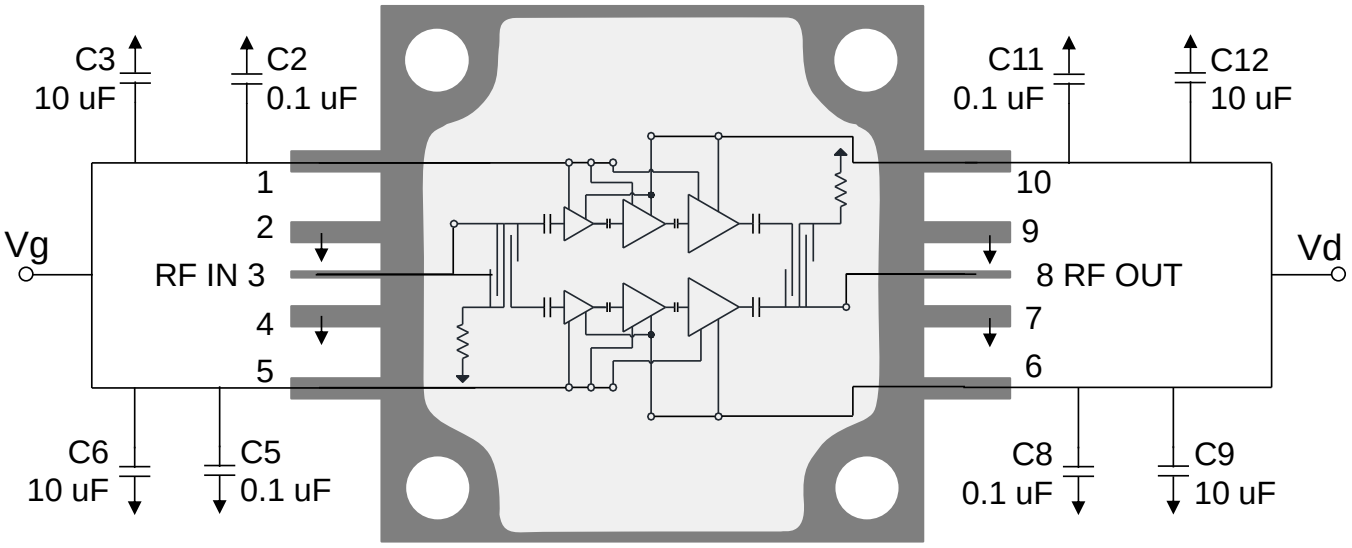
ORL vs. Frequency vs. Temperature



ORL vs. Frequency vs. Drain Current



Applications Information and Pin Layout



Bias-up Procedure

1. Set I_D limit to 2 A, I_G limit to 35 mA
2. Apply −5 V to V_G
3. Apply +20 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 560 mA (V_G ~ −2.5 V Typical).
5. Turn on RF supply

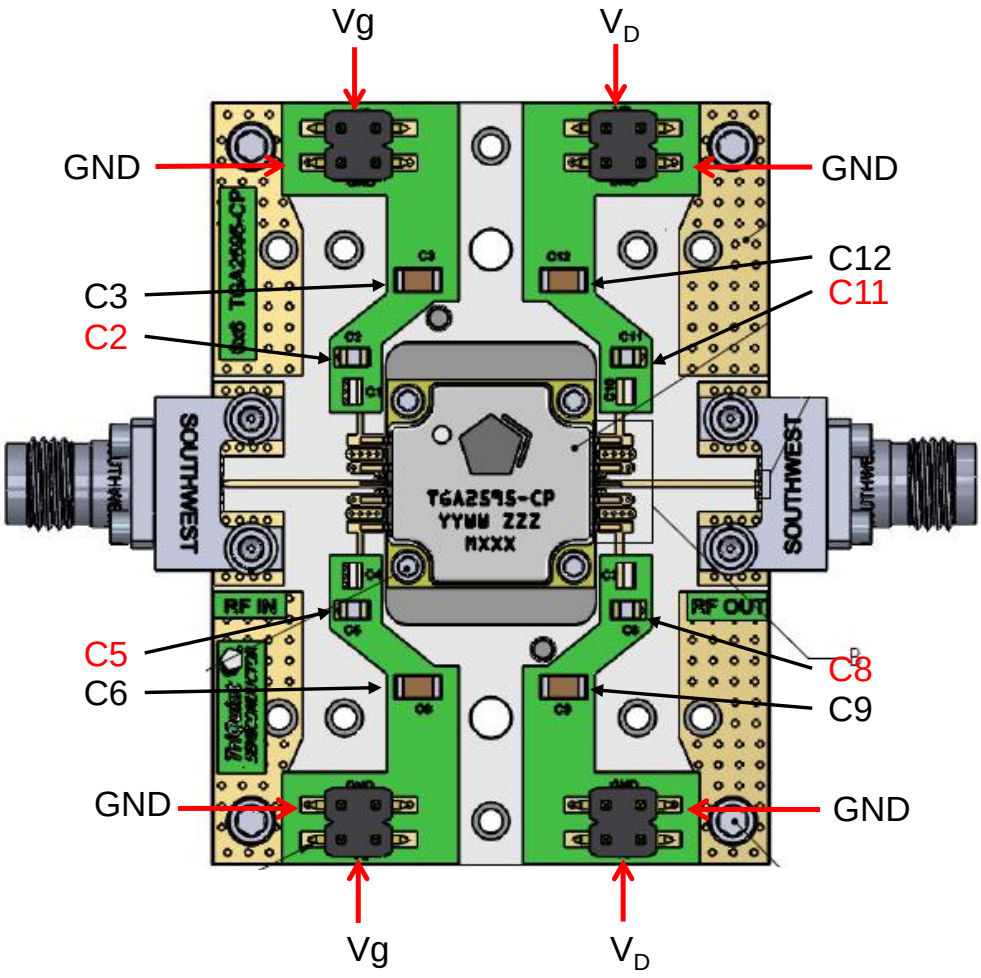
Bias-down Procedure

1. Turn off RF supply
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Pin Description

Pin No.	Symbol	Description
1,5	V_G	Gate Voltage; Bias network is required; must be biased from both sides; see recommended Application Information above.
3	RF_{IN}	Input; matched to 50 Ω; DC blocked
2,4,7,9	GND	Must be grounded on the PCB.
6,10	V_D	Drain voltage; Bias network is required; must be biased from both sides; see recommended Application Information above.
8	RF_{OUT}	Output; matched to 50 Ω; DC blocked

Evaluation Board



PCB NOTES:

(1) Both Top and Bottom Vd and Vg must be biased.

(2) This PCB is non-standard, and requires PCB trace modification for 30GHz performance optimization. See Gerber files for detailed information.

Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
C2, C5, C8, C11	0.1 µF	Cap, 0603, 50 V, 10%, X7R	Various	
C3, C6, C9, C12 (1)	10 µF	Cap, 1206, 50 V, 20%, X5R	Various	

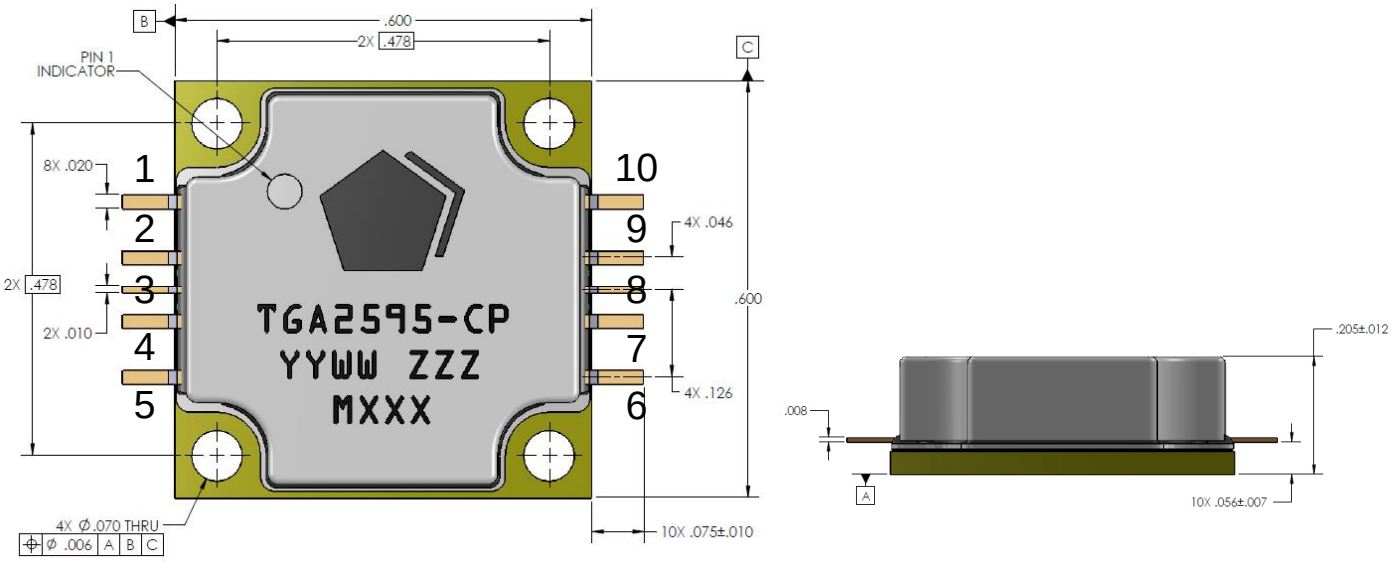
Notes:

(1) Capacitors in drain path should be removed for pulsed operation.

Assembly Notes

1. Clean the board or module with alcohol. Allow it to dry fully.
2. Nylock screws are recommended for mounting the TGA2595-CP to the board.
3. To improve the thermal and RF performance, we recommend the following:
   a. Apply thermal compound or 4 mils indium shim between the package and the board.
   b. Attach a heat sink to the bottom of the board and apply thermal compound or 4 mils indium shim between the heat sink and the board.
4. Apply solder to each pin of the TGA2595-CP.
5. Clean the assembly with alcohol.

Mechanical Information



Units: inches

Tolerances: unless specified

x.xx = ± 0.01

x.xxx = ± 0.005

Materials:

Base: Copper

Lid: Plastic

All metalized features are gold plated

Part is epoxy sealed

Marking:

2595: Part number

YY: Part Assembly year

WW: Part Assembly week

ZZZ: Serial Number

MXXX: Batch ID

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

Level 5A at 260 °C convection reflow.
The part is rated Moisture Sensitivity Level 5A at 260 °C per JEDEC standard IPC/JEDEC J-STD-020.

ECCN

US Department of Commerce: 3A001.b.2.c

Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260°C

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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