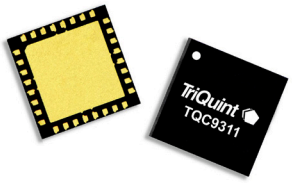
TQC9311

0.4-3.6 GHz Dual Channel DVGA

Applications

- Wireless Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- Diversity or MIMO Receivers

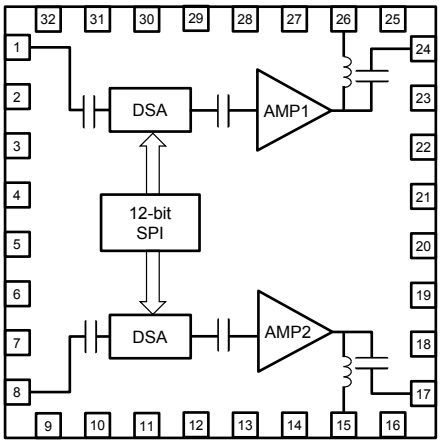


32-pin 7 x 7 mm Leadless SMT Package

Product Features

- Dual channel, integrating DSA + Amp Functionality
- 0.4 – 3.6 GHz Broadband Performance
- 13.2 dB Gain at 1.95 GHz
- 3.8 dB Noise Figure at max gain setting
- +21.1 dBm P1dB
- +36.5 dBm OIP3
- +5 V Supply Voltage
- Integrated on-chip matching and bias chokes
- 3-wire SPI Control Programming
- +1.8 V and +3.3 V logic compatible serial input

Functional Block Diagram



General Description

The TQC9311 is a dual-channel, digitally-controlled variable gain amplifier (DVGA) operating over a broadband frequency range of 400 to 3600 MHz. The DVGA features +36.5 dBm OIP3 while providing digital variable gain with 31.5 dB of gain range in 0.5 dB steps through a 12-bit serial mode control interface. This combination of performance parameters makes the DVGA ideal for diversity or MIMO receiver applications requiring gain control with high linearity and low noise figure.

The TQC9311 integrates a high performance digital step attenuator followed by a high linearity, broadband gain block in a dual-channel configuration. The dual channel DVGA is internally matched to 50 Ohms and does not require any external matching components. Bias choke inductors and bypass/blocking capacitors are also integrated into the module thereby reducing the number of external components needed.

The TQC9311 is packaged in a RoHS-compliant, compact 7 x 7 mm surface-mount leadless package.

Pin Configuration

Pin No.	Label	Pin No.	Label
1	RFIN_1	8	RFIN_2
3	VCC_SPI	15	VDD_AMP2
4	LE	17	RFOUT_2
5	DATA	24	RF_OUT1
6	CLK	26	VDD_AMP1
7, 10, 13, 28, 31	No Connect	26	VDD_AMP1

All other pins are internally grounded.

Ordering Information

Part No.	Description
TQC9311	0.4-3.6 GHz Dual-channel DVGA
TQC9311-PCB	Evaluation Board

Standard T/R size = 2500 pcs on a 13” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150 °C
RF Input Power, CW, 50Ω, 24 hr, 25°C	+24 dBm
V_{DD}, Power Supply Voltage	+6 V
Reverse Device Voltage	−0.3 V
Digital Input Voltage	V_{DD}+ 0.5 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+4.75	+5	+5.25	V
T_{ch} (for >10^6 hours MTTF)			+190	°C
Case Temperature	-40		+105	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions: V_{AMP} = V_{DD} =+5 V, T_{LEAD}=+25°C

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		400		3600	MHz
Test Frequency			1950		MHz
Gain	Max gain setting		13.2		dB
Gain Control Range			31.5		dB
Gain Control Step Size			0.5		dB
Control Interface			12		bits
Gain Accuracy	700 – 2700 MHz, major states		± (0.3 + 5% of Atten. Setting)		dB
Input Return Loss			13		dB
Output Return Loss			11.5		dB
Output P1dB			+21.1		dBm
Output IP3	Pout = +3 dBm/tone, Δf = 1MHz		+36.5		dBm
Input IP3	Pin = -8 dBm/tone, Δf = 1MHz		+23.3		dBm
Isolation	Channel-to-channel		55		dB
Noise Figure	Max gain setting		3.8		dB
Supply Current	Per channel		87		mA
Thermal Resistance (R_{th})	Channel to case				°C /W

Serial Control Interface

The TQC9311 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SID) SPI™ input compatible. At power up, the serial control interface resets the DVGA to the minimum gain state (maximum attenuation setting). The 12-bit Serial Input Data (SID) word is loaded into the register on rising edge of the CLK, MSB first. When LE is high, CLK is internally disabled in the DVGA.

Serial Control Timing Characteristics

Test conditions: V_{DD-DSA}= +5 V[1], T_{LEAD}=25°C

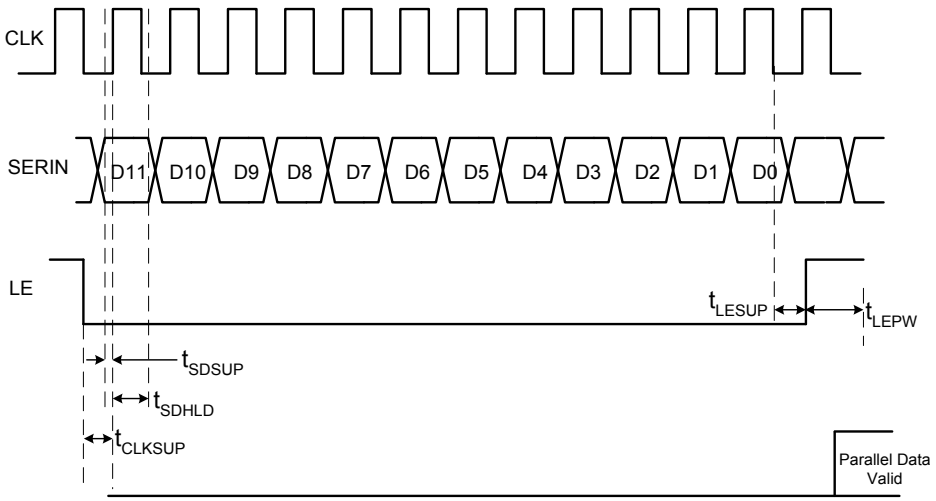
Parameter	Condition	Min	Max	Units
Clock Frequency, f_{CLK}	50% Duty Cycle,		25	MHz
LE Setup Time, t_{LESUP}	CLK to LE setup time	5		ns
CLK Setup Time, t_{CLKSUP}	LE to CLK setup time	5		ns
LE Pulse Width, t_{LEPW}		10		ns
SERIN set-up time, t_{SDSUP}	before CLK rising edge	5		ns
SERIN hold-time, t_{SDHLD}	after CLK rising edge	5		ns
Propagation Delay, t_{PLO}			20	ns

Notes:
1. Internal SPI chip compatible to +1.8 V and +3.3 V logic levels.

Serial Control DC Logic Characteristics

Test conditions: V_{DD} = +5 V, Temp.=25°C

Parameter	Condition	Min	Max	Units
Low State Input Voltage, V_{IL}		0	0.5	V
High State Input Voltage, V_{IH}		1.2	V_{DD}	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK	−10	+10	µA



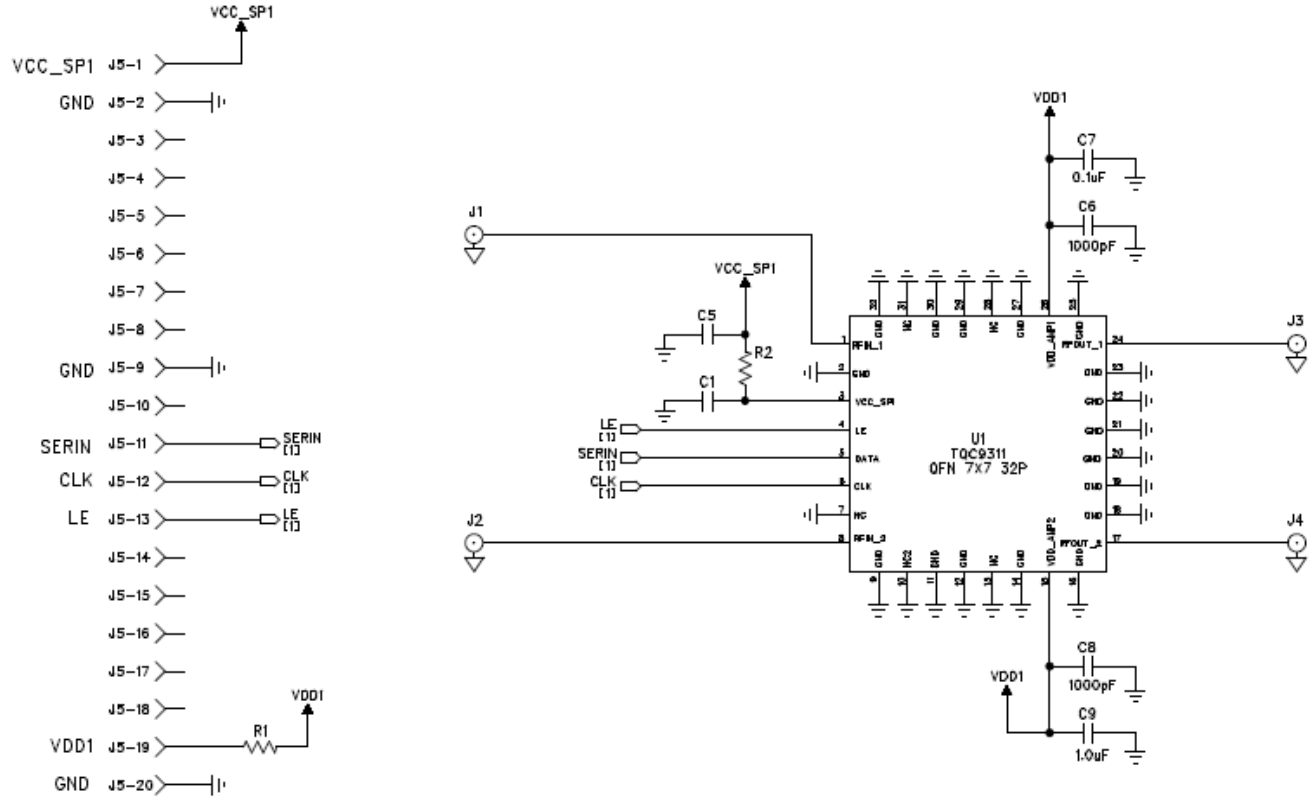
Serial Control Interface

Serial In Control Logic Truth Table, MSB in first

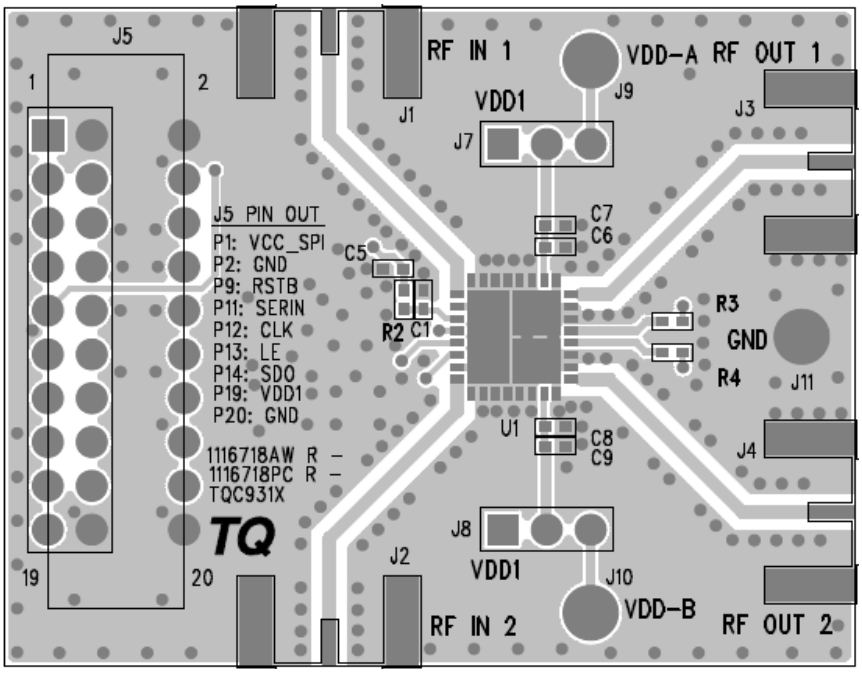
12-Bit Control Word												Attenuation
Channel 1 Control						Channel 2 Control						
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	1	1	1	1	Maximum Gain
1	1	1	1	1	0	1	1	1	1	1	0	−0.5 dB
1	1	1	1	0	1	1	1	1	1	0	1	−1 dB
1	1	1	0	1	1	1	1	1	0	1	1	−2 dB
1	1	0	1	1	1	1	1	0	1	1	1	−4 dB
1	0	1	1	1	1	1	0	1	1	1	1	−8 dB
0	1	1	1	1	1	0	1	1	1	1	1	−16 dB
0	0	0	0	0	0	0	0	0	0	0	0	−31.5 dB

Any combination of the possible 64 states will provide a reduction in gain of approximately the sum of the bits selected.

Application Board Schematic



Application Board Layout



Top RF layer is 0.014”, Dielectric Isola FR408HR, 4-layer, 0.062” overall thickness.

Bill of Material – TQC9311-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	Dual Channel DVGA	TriQuint	TQC9311
C1, C6, C8	1000 pF	CAP, 0402, 10%, 50V	various	
C5, C7, C9	0.1 uF	CAP, 0402, 10%	various	
R2	0 Ω	RES, 0402, 5%, 1/16W	Various	

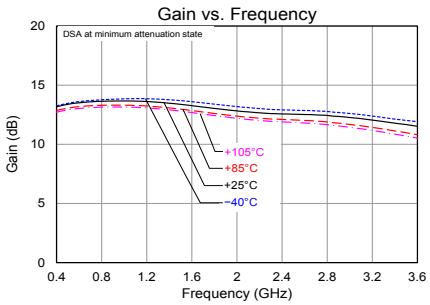
Performance Summary

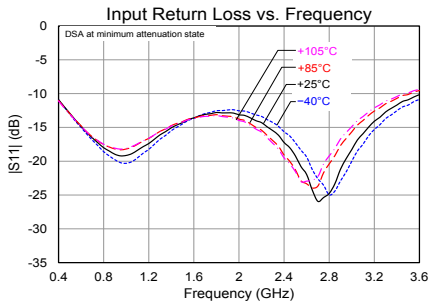
Test conditions: T_{LEAD}=+25°C, V_{DD} =+5V

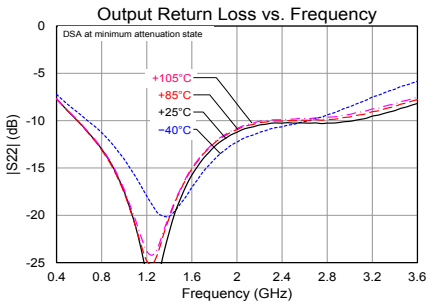
Frequency	900	1950	2700	MHz
Gain	13.8	13	12.6	dB
Input Return Loss	19	13	25	dB
Output Return Loss	15	11.7	10.5	dB
Output P1dB		+21.1		dBm
Output IP3 (Pout/tone=+3dBm, Δf=1MHz)	+37.1	+36.5	+36	dBm
Isolation (CH1 to CH2)	63	55	51	dB
Noise Figure	3.1	3.8	4.4	dB
Amplifier Current (per channel)		87		mA

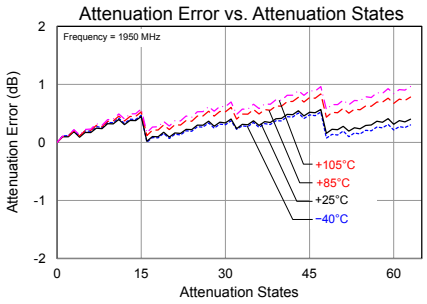
Performance Plots: Channel 1/ Channel 2

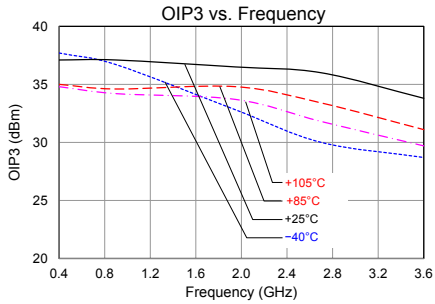
Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CQ} = 87 mA (typ.)

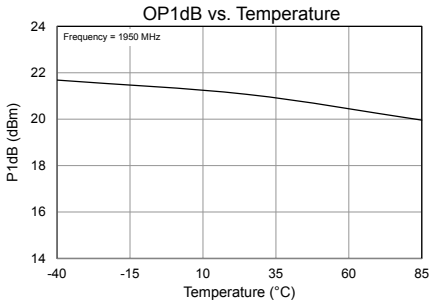


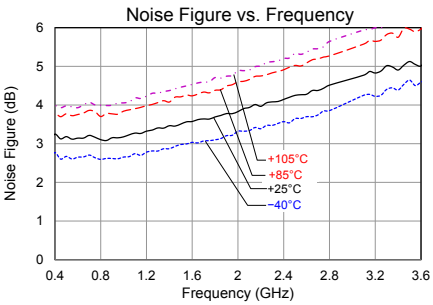


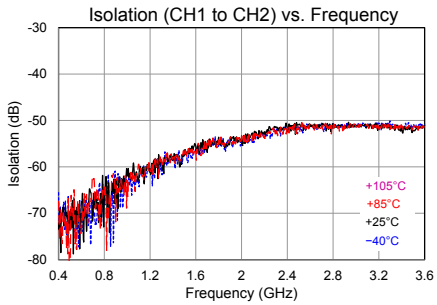


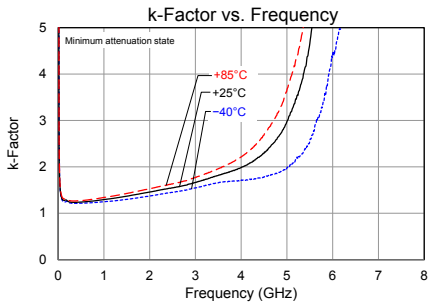




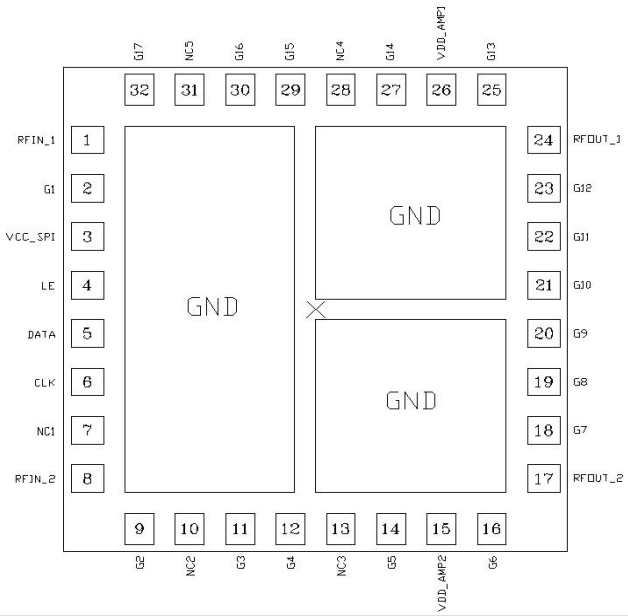








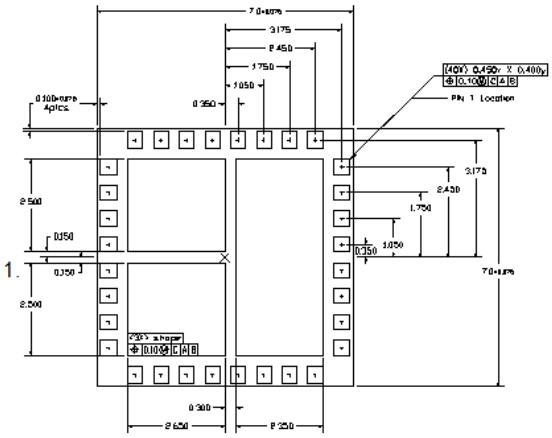
Pin Configuration and Description

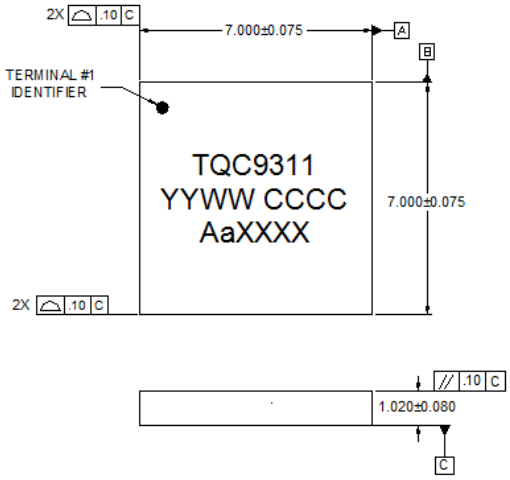


Pin No.	Label	Description
1	RFIN_1	Channel 1 RF Input. This pin is DC blocked internally.
2, 9, 11, 12, 14, 16, 18 19, 20, 21, 22, 23, 25 27, 29, 30	GND	These pins are grounded internally and should be connected to the PCB ground for good performance.
3	VCC_SPI	DC supply into SPI and DSA.
4	LE	Latch Enable
5	DATA	Serial Input Data
6	CLK	Serial Clock
7, 10, 13, 28, 31	NC	No electrical connection. Provide land pads for PCB mounting integrity. These pins can be grounded on the PCB.
8	RFIN_2	Channel 2 RF Input. This pin is DC blocked internally.
15	VDD_AMP2	DC supply into Channel 2 Amplifier. There is a RF choke and 100 pF bypass capacitor internal to the module.
17	RF_OUT_2	Channel 2 RF Output. This pin is DC blocked internally.
24	RF_OUT_1	Channel 1 RF Output. This pin is DC blocked internally.
26	VDD_AMP1	DC supply into Channel 1 Amplifier. There is a RF choke and 100 pF bypass capacitor internal to the module.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Package Dimensions and Marking

Package Marking:
Part number: TQC9311
Year/Week/country code: YYWW CCCC
Asembly code: AaXXXX



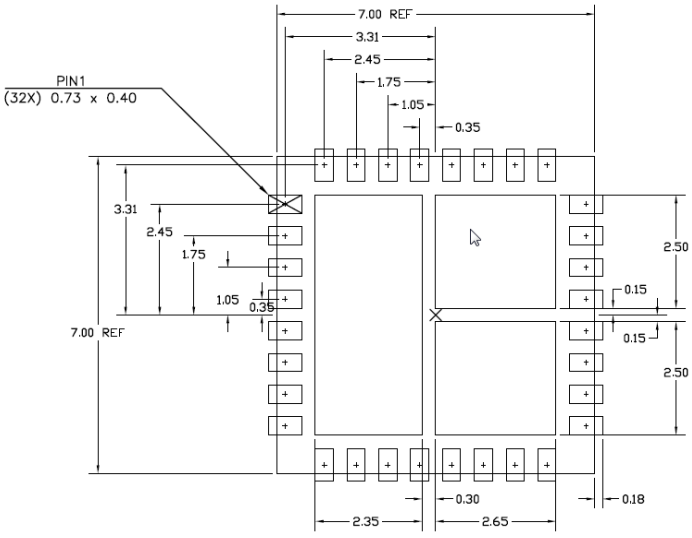


Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-270, Issue B (Variation DAE) for extra thin profile, fine pitch, internal stacking module (ISM).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
5. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.

PCB Mounting Pattern

All dimensions are in millimeters (inches).
Angles are in degrees.



Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1B
Value: ≥ 500 V to < 1000 V
Test: Human Body Model (HBM)
Standard: ESDA/JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: ≥ 1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 3
Test: +260 °C convection reflow
Standard: JEDEC standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temp.) and tin/lead (245 °C max. reflow temp.) soldering processes.

Package lead plating: Electrolytic plated Au over Ni.

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free
- Lead Free

Contact Information

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