MAGX-001214-650L00

GaN on SiC HEMT Pulsed Power Transistor
650 W Peak, 1200-1400 MHz, 300 μs Pulse, 10% Duty

Rev. V1

Features

- GaN on SiC Depletion-Mode Transistor Technology
- Internally Matched
- Common-Source Configuration
- Broadband Class AB Operation
- RoHS* Compliant and 260°C Reflow Compatible
- +50V Typical Operation
- MTTF = 600 Years (T_J < 200°C)

Applications

- L-Band pulsed radar.

Description

The MAGX-001214-650L00 is a gold-metalized matched Gallium Nitride (GaN) on Silicon Carbide (SiC) RF power transistor optimized for pulsed L-Band radar applications. Using state of the art wafer fabrication processes, these high performance transistors provide high gain, efficiency, bandwidth, and ruggedness over a wide bandwidth for today's demanding application needs. High breakdown voltages allow for reliable and stable operation under more extreme mismatch load conditions compared with older semiconductor technologies.

MAGX-001214-650L00

Ordering Information

Part Number	Description
MAGX-001214-650L00	GaN Transistor
MAGX-L21214-650L00	1200-1400 MHz Evaluation Board

Typical RF Performance Under Standard Operating Conditions, P_{OUT} = 650 W (Peak)

Freq. (MHz)	P_{IN} (W)	Gain (dB)	I_D (A)	Eff. (%)	RL (dB)	Droop (dB)	+1dB OD (W)	VSWR-S (3:1)
1200	8.7	18.8	21.3	61.0	-13.9	0.2	717	S
1250	8.5	18.9	22.0	58.9	-13.8	0.3	726	S
1300	8.0	19.1	22.4	57.8	-13.5	0.3	724	S
1350	7.0	19.7	21.8	59.7	-15.8	0.3	723	S
1400	7.0	19.7	21.1	61.4	-15.0	0.2	697	S

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Electrical Specifications: Freq. = 1200 - 1400 MHz, T_A = 25°C

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
RF Functional Tests: V_{DD} = 50 V; I_{DQ} = 500 mA; Pulse = 300 μs / 10%						
Peak Input Power	P_{OUT} = 500 W Peak (50 W avg.)	P_{IN}	-	7.5	10.3	W
Power Gain	P_{OUT} = 500 W Peak (50 W avg.)	G_P	18	19.5	-	dB
Drain Efficiency	P_{OUT} = 500 W Peak (50 W avg.)	η_D	55	60	-	%
Pulse Droop	P_{OUT} = 500 W Peak (50 W avg.)	Droop	-	0.3	0.6	dB
Load Mismatch Stability	P_{OUT} = 500 W Peak (50 W avg.)	VSWR-S	-	2:1	-	-
Load Mismatch Tolerance	P_{OUT} = 500 W Peak (50 W avg.)	VSWR-T	-	3:1	-	-

Electrical Characteristics: T_A = 25°C

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
DC Characteristics						
Drain-Source Leakage Current	V_{GS} = -8 V, V_{DS} = 175 V	I_{DS}	-	1.7	33	mA
Gate Threshold Voltage	V_{DS} = 5 V, I_D = 90 mA	$V_{GS (TH)}$	-5	-2.9	-2	V
Forward Transconductance	V_{DS} = 5 V, I_D = 21 mA	G_M	16.2	21.7	-	S
Dynamic Characteristics						
Input Capacitance	Not applicable - Input matched	C_{ISS}	N/A	N/A	N/A	pF
Output Capacitance	V_{DS} = 50 V, V_{GS} = -8 V, F = 1 MHz	C_{OSS}	-	55	-	pF
Reverse Transfer Capacitance	V_{DS} = 50 V, V_{GS} = -8 V, F = 1 MHz	C_{RSS}	-	5.5	-	pF

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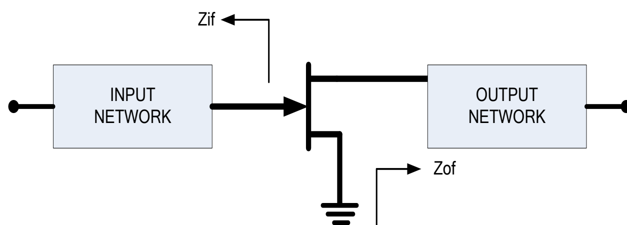
Absolute Maximum Ratings[1,2,3,4]

Parameter	Limit
Supply Voltage (V_{DD})	+65 V
Supply Voltage (V_{GG})	-8 to -2 V
Supply Current (I_{DMAX})	27 A
Input Power (P_{IN})	P_{IN} (nominal) + 3 dB
Absolute Max. Junction/Channel Temp	200ºC
Pulsed Power Dissipation at 85ºC	700 W
Thermal Resistance, (T_J = 70ºC) V_{DD} = 50 V, I_{DQ} = 500 mA, P_{OUT} = 650 W, 300 μs Pulse / 10% Duty	0.25ºC/W
Operating Temp	-40 to +95ºC
Storage Temp	-65 to +150ºC
Mounting Temperature	See solder reflow profile
ESD Min. - Charged Device Model (CDM)	1300 V
ESD Min. - Human Body Model (HBM)	4000 V

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Input Power Limit is +3 dB over nominal drive required to achieve P_{OUT} = 650 W.
3. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.
4. For saturated performance it recommended that the sum of (3*V_{DD} + abs(V_{GG})) <175 V.

Test Fixture Impedances

F (MHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
1200	0.8 - j0.9	1.4 + j0.2
1250	0.8 - j0.7	1.4 + j0.2
1300	0.7 - j0.6	1.4 + j0.1
1350	0.7 - j0.4	1.2 + j0.1
1400	0.7 - j0.2	1.1 + j0.2



Correct Device Sequencing

Turning the device ON

1. Set V_{GS} to the pinch-off (V_P), typically -5 V.
2. Turn on V_{DS} to nominal voltage (50 V).
3. Increase V_{GS} until the I_{DS} current is reached.
4. Apply RF power to desired level.

Turning the device OFF

1. Turn the RF power off.
2. Decrease V_{GS} down to V_P.
3. Decrease V_{DS} down to 0 V.
4. Turn off V_{GS}.

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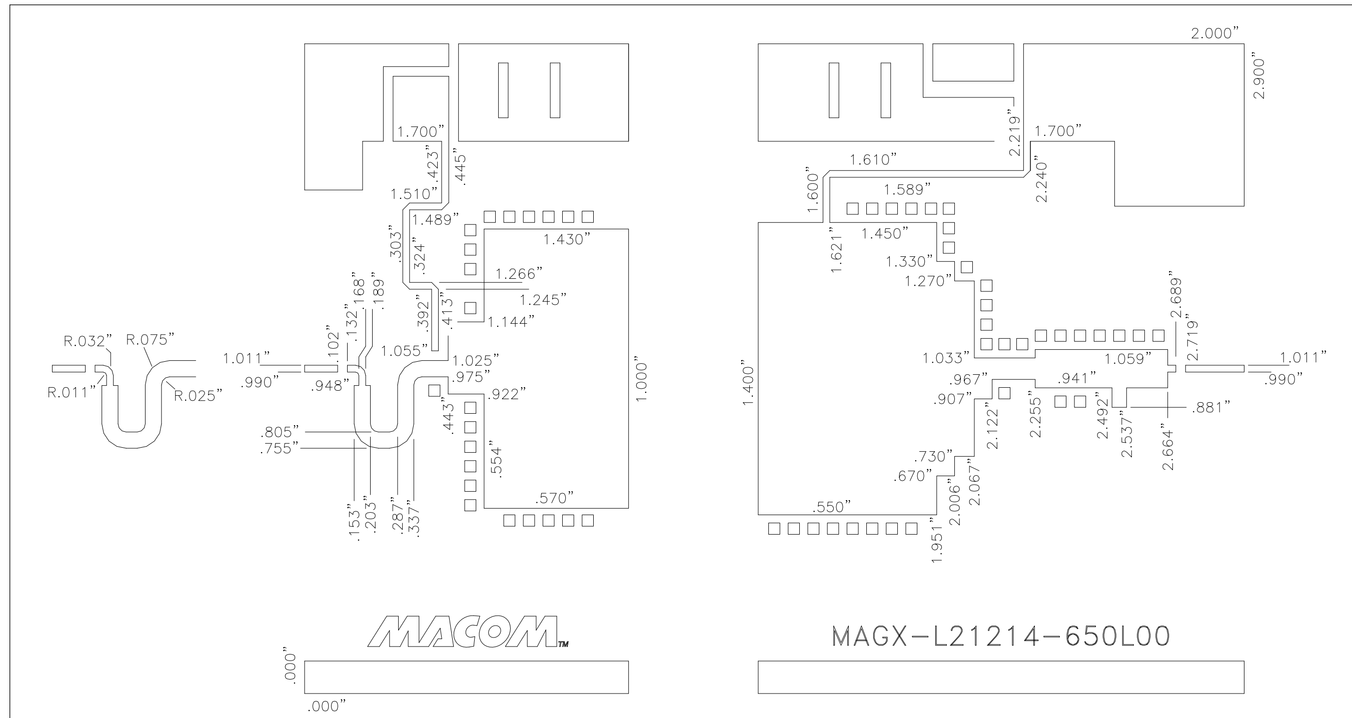
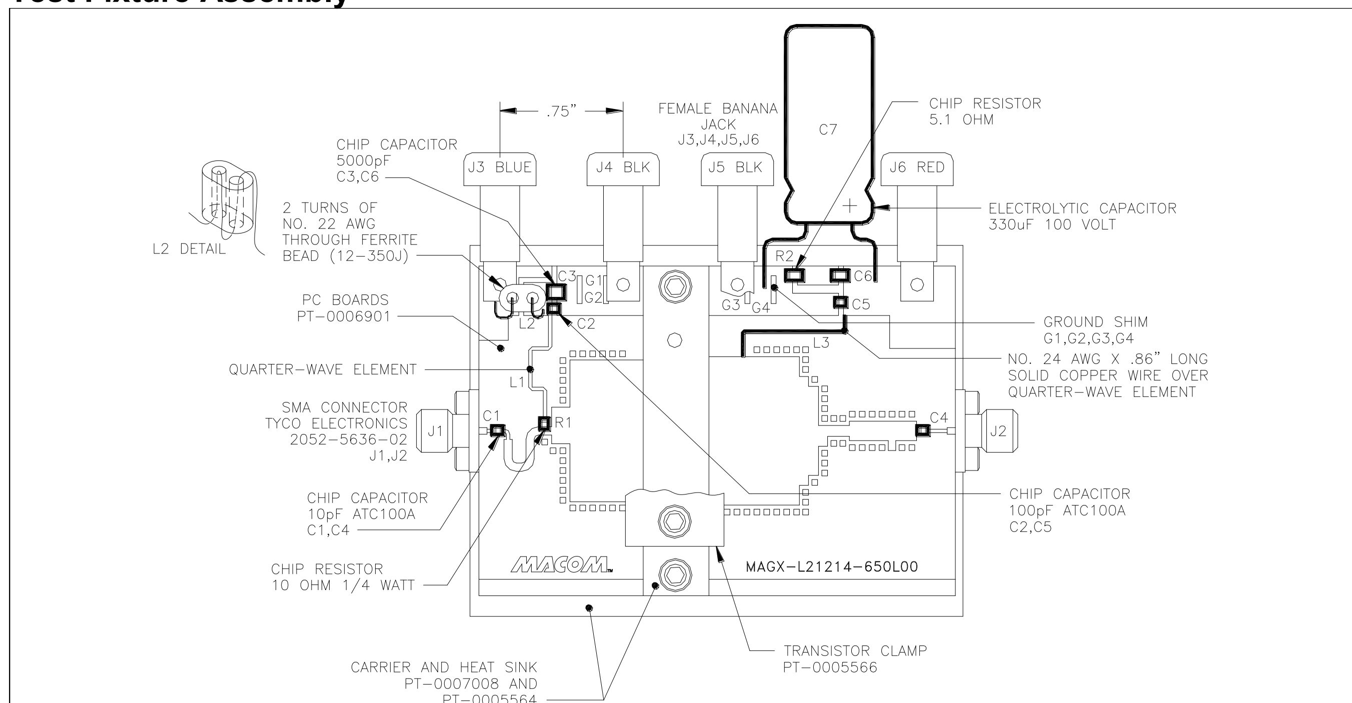
Test Fixture Circuit Dimensions



Test Fixture Assembly



Contact factory for gerber file or additional circuit information.

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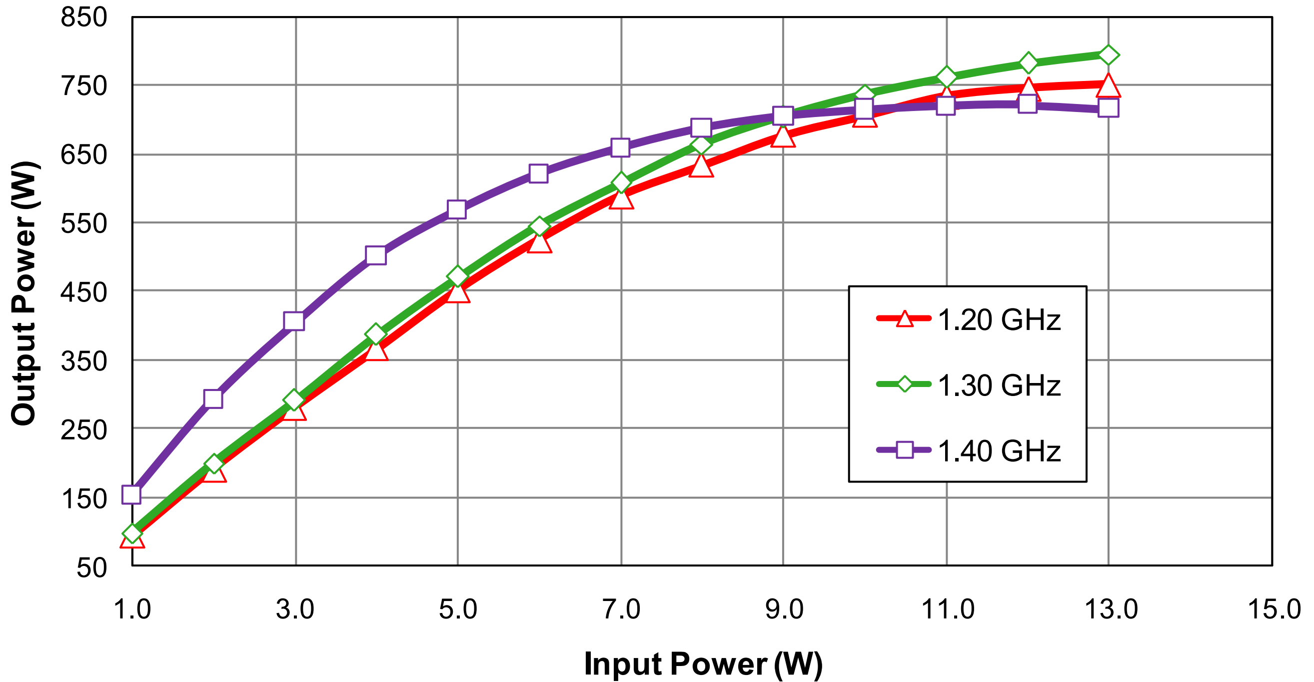
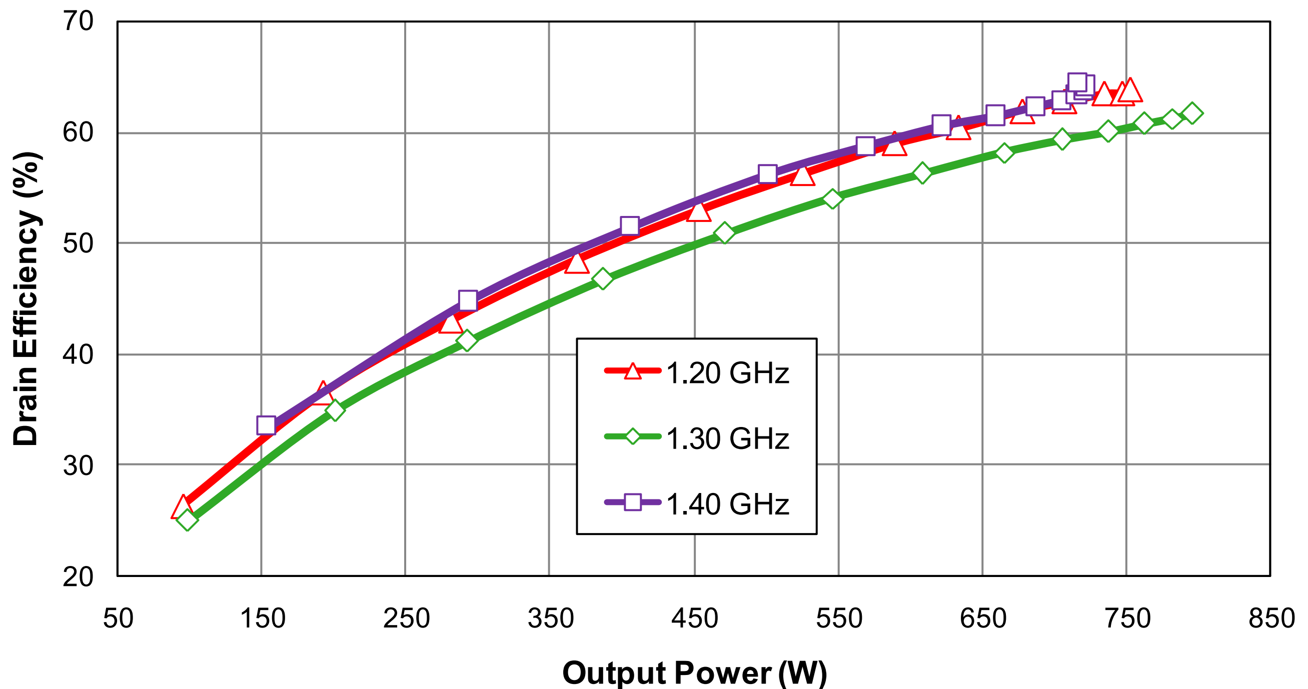
RF Power Transfer Curve (Output Power vs. Input Power)



RF Power Transfer Curve (Drain Efficiency vs. Output Power)



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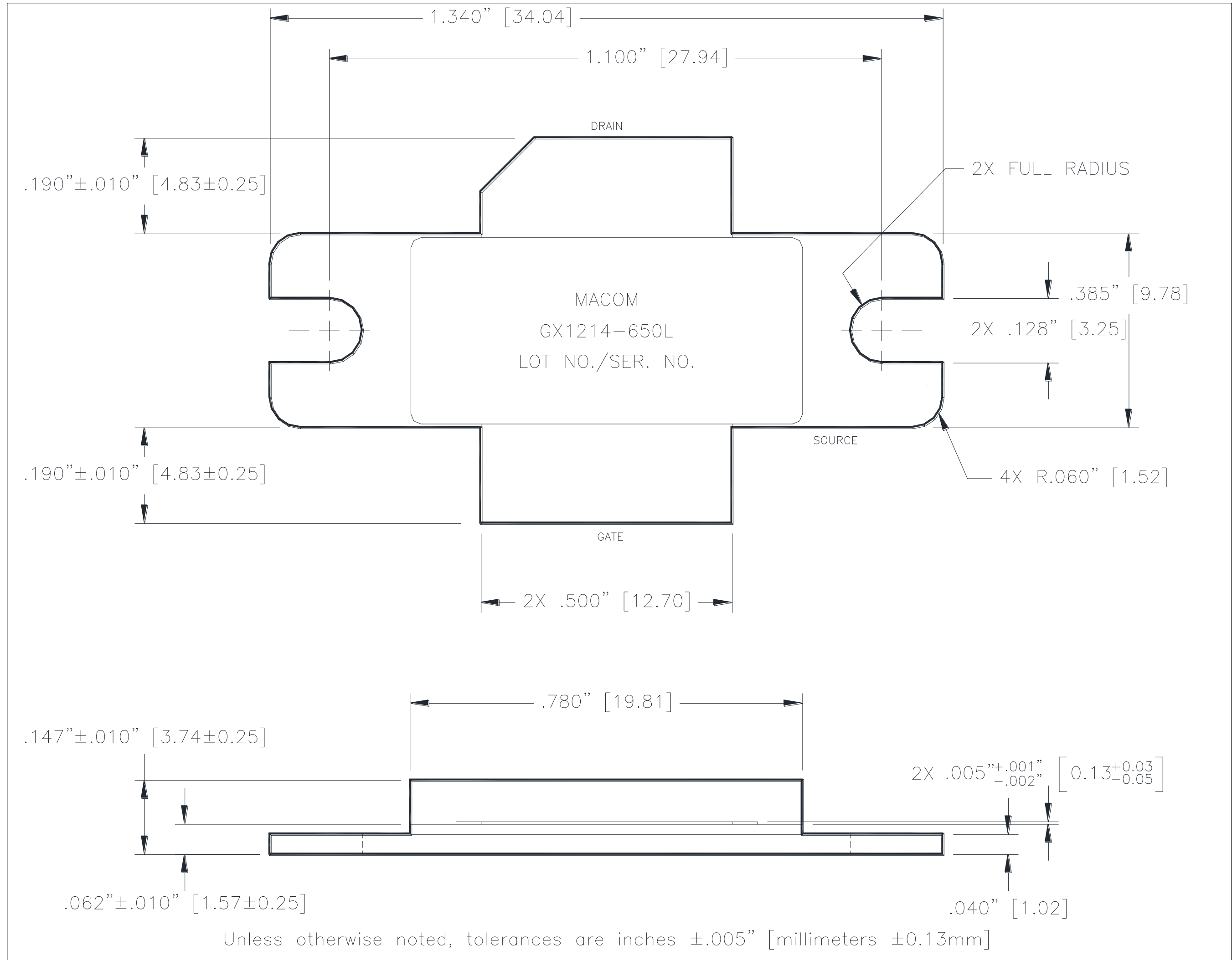
Outline Drawing MAGX-001214-650L00



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