

AT-273-PIN



Digital Attenuator
32.0 dB, 2-Bit, TTL Driver, DC-2.0 GHz

Rev. V9

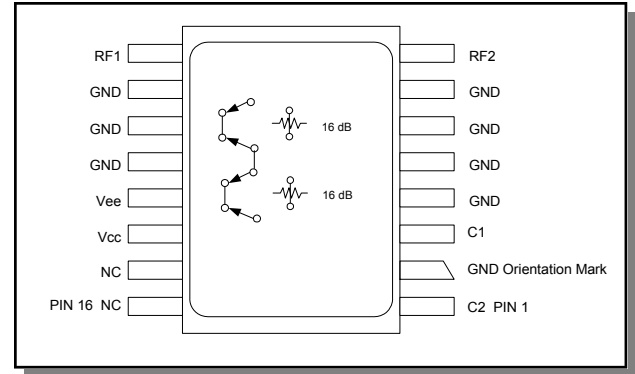
Features

- Attenuation: 16.0 dB Steps to 32 dB
- Low DC Power Consumption
- Hermetic Surface Mount Package
- Integral TTL Driver
- 50 ohm Impedance
- Temperature Stability: ± 0.18 dB from -55°C to $+85^{\circ}\text{C}$ Typ.
- Tape and Reel Packaging Available
- Lead-Free CR-11 Package
- 260°C Reflow Compatible
- RoHS* Compliant

Description

M/A-COM's AT-273-PIN is a GaAs FET digital attenuator with a 16.0 dB minimum step size and a 32 dB total attenuation range. This attenuator and integral TTL driver is in a hermetically sealed ceramic 16-lead surface mount package. The AT-273-PIN is ideally suited for use where accuracy, fast switching, very low power consumption and low intermodulation products are required. Typical applications include dynamic range setting in precision receiver circuits and other gain/leveling control circuits. Environmental screening is available. Contact the factory for information.

Functional Schematic¹



1. Use the C1 control for a single 16-dB bit.

Pin Configuration

| Pin No. | Function | Pin No. | Function |
|---------|----------|---------|----------|
| 1 | C2 | 9 | RF1 |
| 2 | GND | 10 | GND |
| 3 | C1 | 11 | GND |
| 4 | GND | 12 | GND |
| 5 | GND | 13 | Vee |
| 6 | GND | 14 | Vcc |
| 7 | GND | 15 | NC |
| 8 | RF2 | 16 | NC |

The metal bottom of the case must be connected to RF and DC ground.

Ordering Information

| Part Number | Package |
|-------------|----------------|
| AT-273-PIN | Bulk Packaging |

Note: Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Electrical Specifications: $T_A = 25^\circ\text{C}^{1,2}$

| Parameter | Test Conditions | Frequency | Units | Min | Typ | Max |
|---|---|---------------|--|------|-----|-------|
| Insertion Loss | — | DC - 0.5 GHz | dB | — | — | 1.6 |
| | | DC - 1.0 GHz | dB | — | — | 1.7 |
| | | DC - 2.0 GHz | dB | — | — | 1.9 |
| Attenuation Accuracy | C1 Bit | DC - 2.0 GHz | ± 3% of attenuation setting in dB | | | |
| | Full Attenuation (32 dB) | DC - 0.5 GHz | ± 3% of attenuation setting in dB | | | |
| | Full Attenuation (32 dB) | DC - 1.0 GHz | ± 3% of attenuation setting in dB, -1 dB | | | |
| | Full Attenuation (32 dB) | DC - 2.0 GHz | ± 3% of attenuation setting in dB, -3 dB | | | |
| VSWR | Full Range | DC - 2.0 GHz | Ratio | — | — | 1.6:1 |
| Trise, Tfall | 10% to 90% | — | ns | — | 7 | — |
| Ton, Toff | 50% Cntl to 90% / 10% RF | — | ns | — | 28 | — |
| Transients | In-Band (peak-to-peak) | — | mV | — | 30 | — |
| 1 dB Compression | Input Power Input Power | 0.05 GHz | dBm | — | +20 | — |
| | | 0.5 - 2.0 GHz | dBm | — | +28 | — |
| Input IP3 | Two-tone inputs up to +5 dBm | 0.05 GHz | dBm | — | +38 | — |
| | | 0.5 - 2.0 GHz | dBm | — | +48 | — |
| Input IP2 | Two-tone inputs up to +5 dBm | 0.05 GHz | dBm | — | +44 | — |
| | | 0.5 - 2.0 GHz | dBm | — | +68 | — |
| Vcc | — | — | V | 4.5 | 5.0 | 5.5 |
| -Vee | — | — | V | -8.0 | — | -5.0 |
| Vctl | Logic (0) TTL | — | V | 0.0 | — | 0.8 |
| Vctl | Logic (1) TTL | — | V | 2.0 | — | 5.0 |
| Input Leakage Current (Low) Input Leakage Current (High) | 0 to 0.8V 2.0 to 5.0V | — | µA | — | — | 1.0 |
| | | — | µA | — | — | 1.0 |
| Icc | Vcc = 4.5 to 5.5V Vctl = 0 to 0.8V, or Vcc -2.1V to Vcc | — | mA | — | — | 2.0 |
| -lee | Vee = -5.0 to -8.0V | — | mA | — | — | -1 |

1. All specifications apply when operated with bias voltages of +5V for Vcc and -5.0V for Vee.
2. This attenuator is guaranteed monotonic.

Absolute Maximum Ratings ^{3,4}

| Parameter | Absolute Maximum |
|---|---|
| Max. Input Power 0.05 GHz 0.5 - 2.0 GHz | +27 dBm +34 dBm |
| V_{CC} | $-0.5V \leq V_{CC} \leq +7.0V$ |
| V_{EE} | $-8.5V \leq V_{EE} \leq +0.5V$ |
| $V_{CC} - V_{EE}$ | $-0.5V \leq V_{CC} - V_{EE} \leq 14.5V$ |
| V_{in}^5 | $-0.5V \leq V_{in} \leq V_{CC} + 0.5V$ |
| Operating Temperature | $-55^{\circ}C$ to $+125^{\circ}C$ |
| Storage Temperature | $-65^{\circ}C$ to $+150^{\circ}C$ |

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

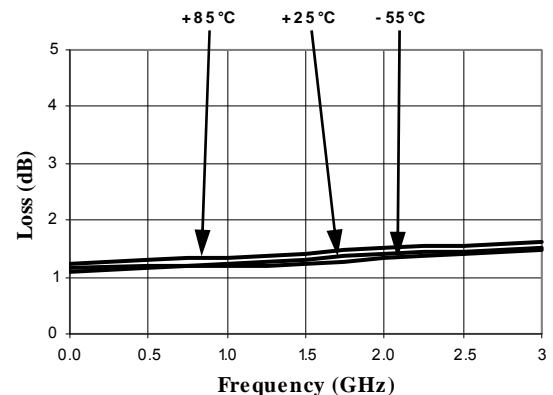
Truth Table (Digital Attenuator)

| C1 | C2 | Attenuation |
|----|----|-----------------|
| 0 | 0 | Loss, Reference |
| 0 | 1 | 16.0 dB |
| 1 | 1 | 32.0 dB |

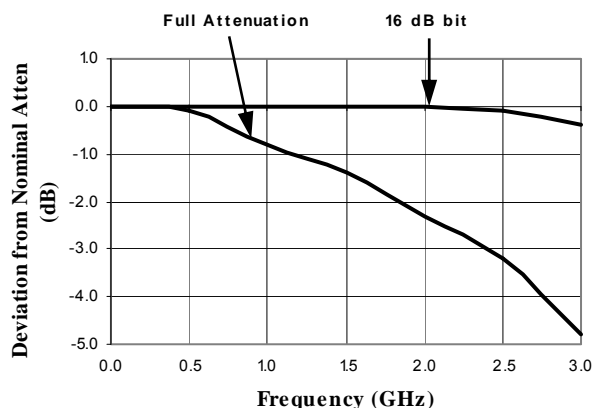
0 = TTL Low; 1 = TTL High

Typical Performance Curves

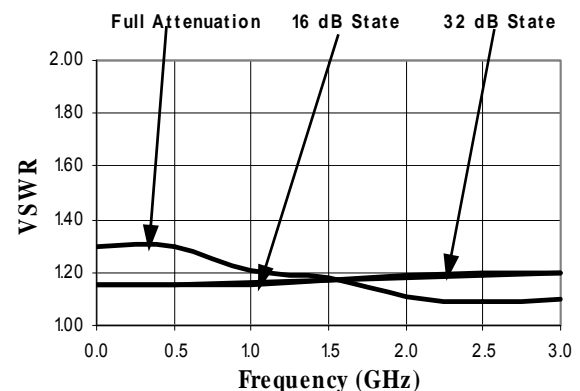
Ref. Insertion Loss vs. Frequency



Attenuation Accuracy vs. Frequency



VSWR vs. Frequency

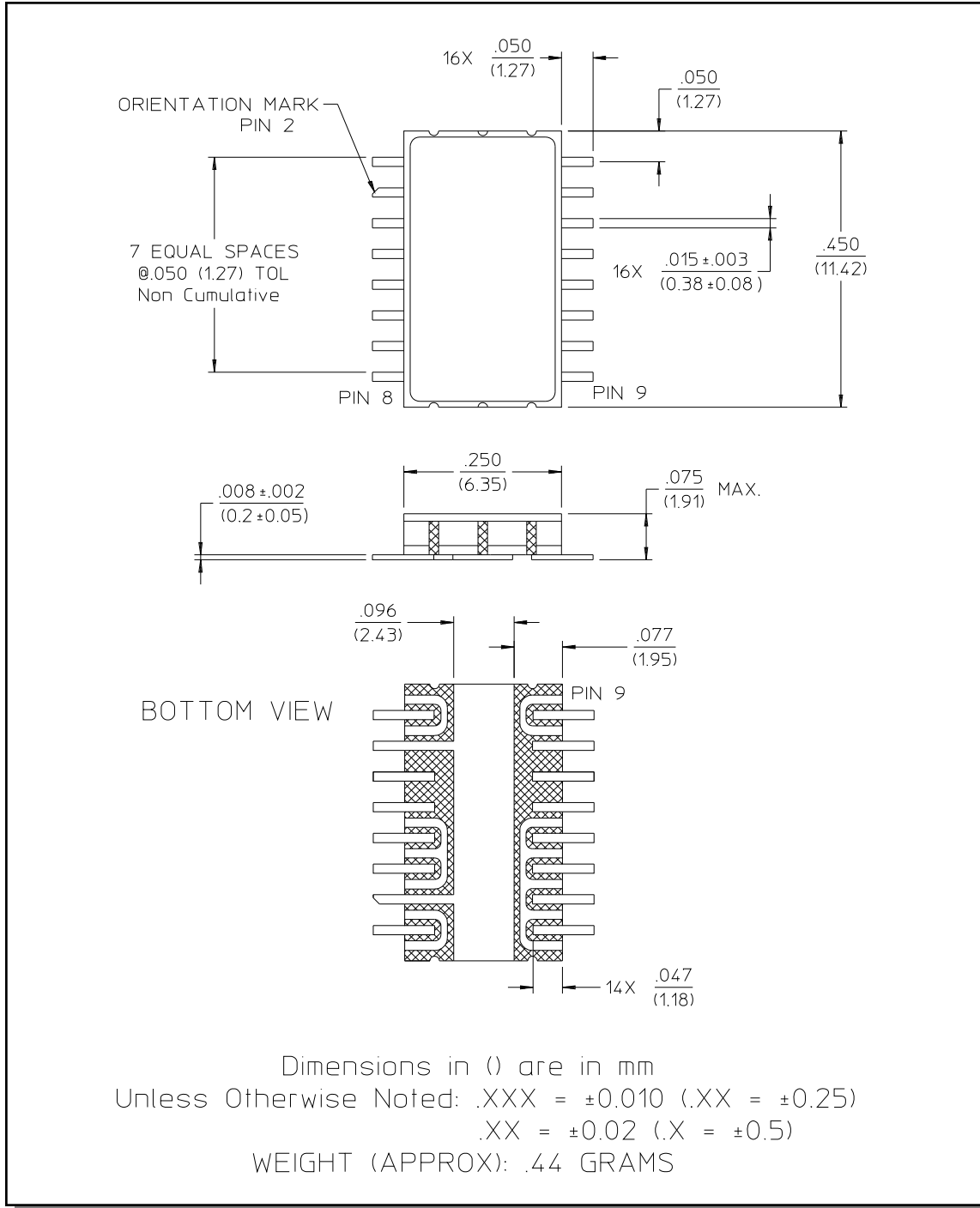


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Lead-Free, CR-11 Ceramic Package†



† Reference Application Note M538 for lead-free solder reflow recommendations.