

17-24GHz Medium Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

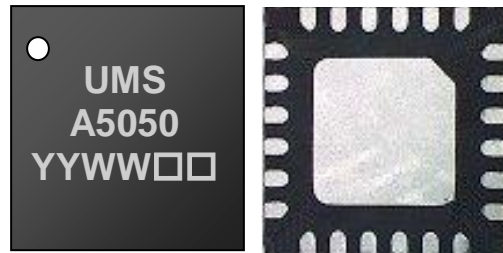
Description

The CHA5050-QDG is a medium power amplifier four stages monolithic circuit.

It is designed for a wide range of applications, from military to commercial communication systems.

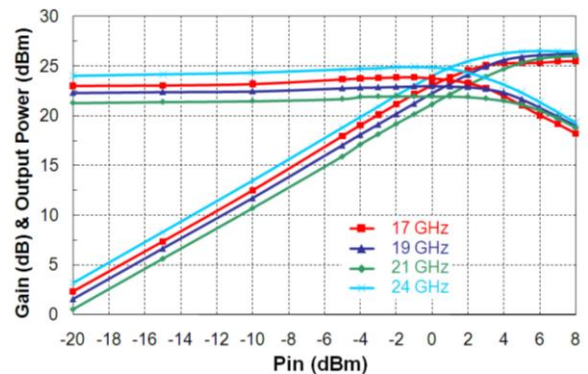
The circuit is manufactured with a pHEMT process, 0.15 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 17-24GHz
- 22dB Linear Gain
- 25dBm Pout @ 1dB comp
- 30dBm Output IP3
- DC bias: Vd=6.0Volt@Id=230mA
- 24L-QFN4x4
- MSL1



Main Electrical Characteristics

Tamb.= +25°C, Vd = Vd1 = Vd2 = Vd3 = Vd4 = 6.0V, Id = 230mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		24	GHz
Gain	Linear Gain		22		dB
P1dB	Output power @ 1dB compression		25		dBm
Psat	Saturated output power		26		dBm
OIP3	Output IP3		30		dBm

Electrical Characteristics

Tamb.= +25°C, Vd = Vd1 = Vd2 = Vd3 = Vd4 = 6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17		24	GHz
G	Small Signal Gain		22		dB
P1dB	Output power @ 1dB compression		25		dBm
Psat	Saturated output power		26		dBm
OIP3	Output IP3		30		dBm
Rlin	Input Return Loss		-7		dB
Rlout	Output Return Loss		-9		dB
Vg	DC gate voltage		-0.5		V
Id	Total drain current		230		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6.5	V
Id	Drain bias current	300	mA
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Maximum peak input power overdrive ⁽²⁾	+8	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

Typical Bias Conditions

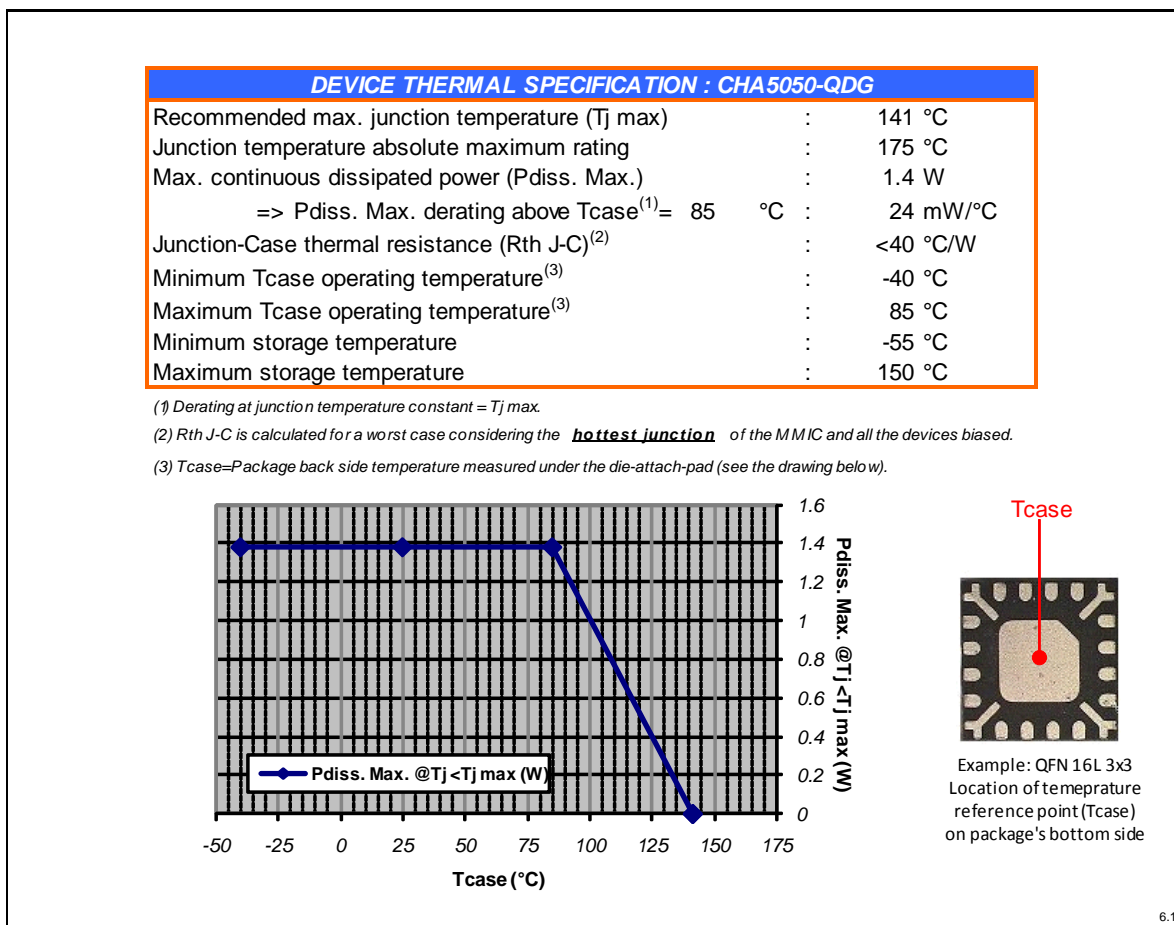
Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd4, Vd3, Vd2, Vd1	7, 9, 10, 12	Drain voltage	6.0	V
Id	7, 9, 10, 12	Drain current controlled with Vg	230	mA
Vg	22	Gate voltage	-0.5	V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).



Typical Package Sij parameters

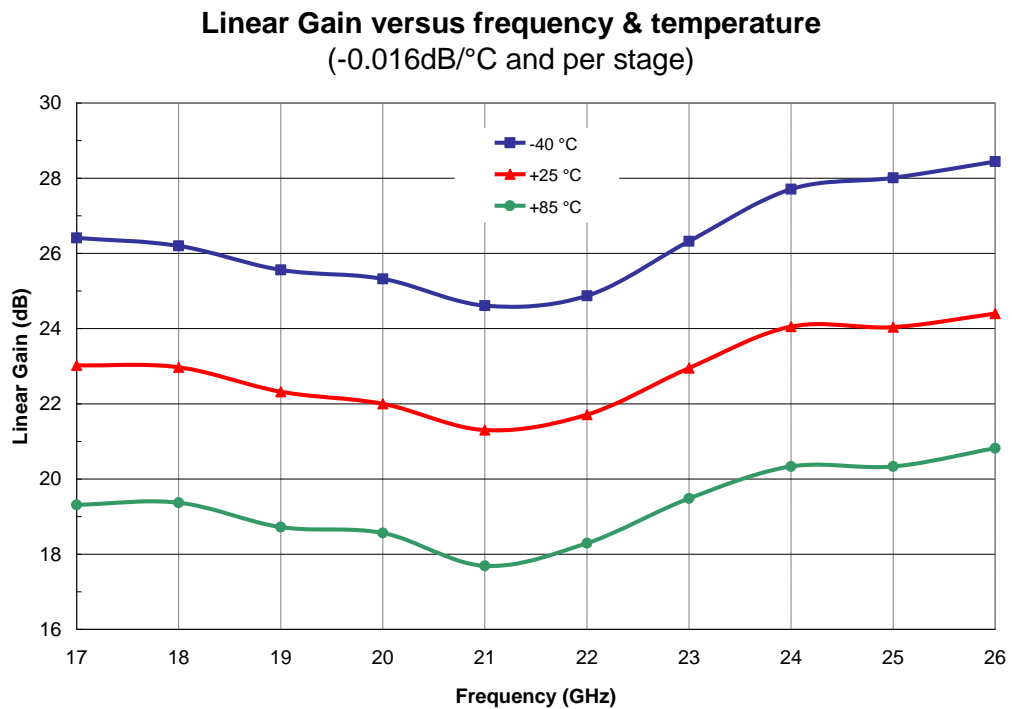
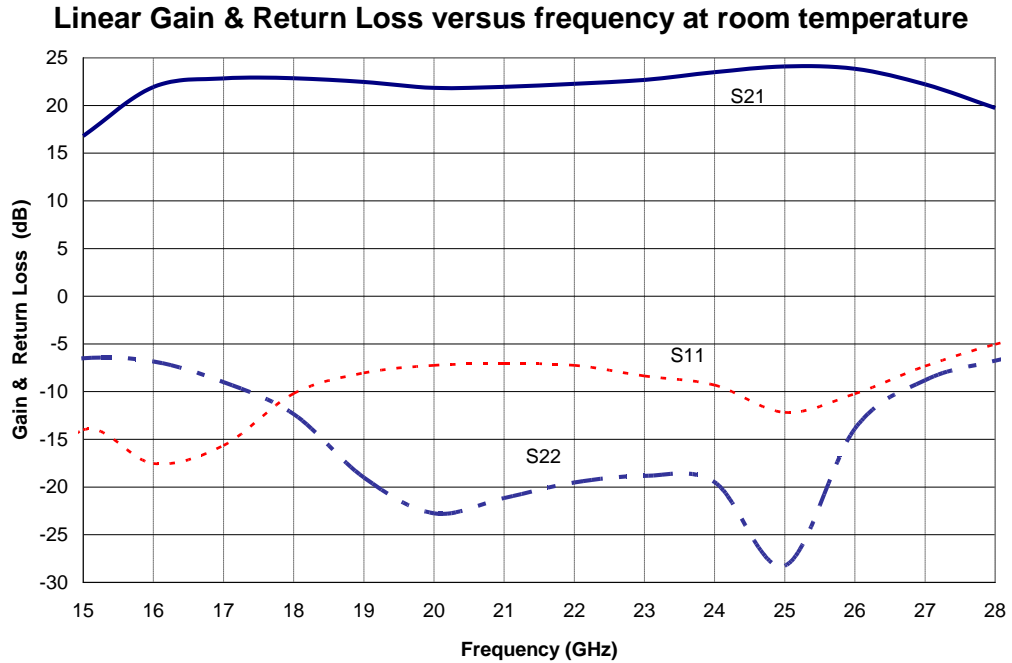
Tamb.= +25°C, Vd = Vd1 = Vd2 = Vd3 = Vd4 = 6.0V, Id = 230mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2	-0.15	-43.46	-79.12	82.91	-93.09	164.10	-0.10	-42.52
3	-0.26	-65.21	-84.47	139.40	-79.29	25.76	-0.17	-64.72
4	-0.34	-86.45	-75.82	-124.90	-76.78	-141.20	-0.19	-88.18
5	-0.67	-109.30	-71.70	-131.10	-62.69	-122.80	-0.41	-110.60
6	-0.92	-130.50	-69.28	165.70	-51.22	169.10	-0.83	-138.00
7	-1.42	-151.70	-67.06	88.13	-39.69	100.50	-1.61	-165.60
8	-1.90	-175.20	-62.98	87.70	-28.67	26.75	-3.05	167.40
9	-2.89	154.90	-65.44	44.97	-19.03	-56.92	-5.89	149.10
10	-4.10	131.00	-66.59	-63.19	-12.25	-138.70	-9.39	130.70
11	-6.29	110.20	-64.11	-74.28	-6.13	149.80	-19.41	118.30
12	-10.06	82.48	-76.01	145.90	-1.12	78.12	-14.19	-153.90
13	-18.87	53.88	-58.93	114.50	3.47	15.51	-9.91	-170.10
14	-21.88	-162.80	-54.27	105.60	9.91	-44.55	-7.87	-179.50
15	-13.42	158.20	-52.66	87.41	16.80	-118.70	-6.51	158.40
16	-16.95	115.40	-51.19	57.99	21.93	144.40	-6.85	128.00
17	-15.06	177.90	-49.55	21.75	22.82	55.31	-9.02	102.40
18	-9.61	150.10	-58.59	14.67	22.84	-23.65	-12.37	68.24
19	-7.45	124.80	-58.33	7.12	22.45	-95.31	-19.02	40.89
20	-6.66	100.90	-58.49	6.88	21.84	-158.90	-22.77	31.90
21	-6.47	79.07	-55.71	49.41	21.94	140.30	-21.18	11.18
22	-6.65	56.92	-64.74	17.23	22.25	79.89	-19.53	-14.93
23	-7.77	38.68	-52.31	77.06	22.66	18.99	-18.83	-45.54
24	-8.73	19.38	-49.00	47.85	23.47	-44.50	-19.50	-58.31
25	-11.58	12.05	-46.33	12.35	24.08	-115.30	-28.26	-19.30
26	-9.64	17.46	-48.81	-7.73	23.83	170.80	-13.90	14.74
27	-6.74	-1.09	-48.77	-9.68	22.20	94.00	-8.81	-13.81
28	-4.45	-25.01	-45.91	13.83	19.73	19.57	-6.77	-37.10
29	-2.70	-54.65	-43.31	0.89	16.01	-53.66	-5.28	-62.66
30	-1.71	-84.20	-40.58	-23.57	11.45	-120.30	-4.57	-92.53
31	-1.09	-110.70	-38.13	-40.14	6.53	176.90	-4.14	-127.00
32	-0.43	-135.10	-36.52	-79.36	1.40	116.70	-3.81	-165.60
33	0.07	-157.60	-38.59	-141.90	-4.67	58.50	-3.30	158.70
34	0.48	-178.40	-55.80	-143.50	-11.29	3.64	-2.54	128.80
35	0.42	162.70	-54.29	-123.80	-19.26	-45.30	-1.92	104.80
36	0.10	147.10	-50.38	-59.24	-27.82	-83.84	-1.32	86.13
37	-0.19	133.00	-48.15	-44.33	-37.07	-93.46	-0.94	70.42
38	-0.40	121.10	-44.07	-51.65	-40.71	-72.72	-0.81	57.16
39	-0.50	108.50	-39.58	-75.49	-38.32	-78.30	-0.71	44.64
40	-0.47	95.99	-38.86	-102.30	-38.42	-95.95	-0.73	30.49

Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Vg = -0.5V, Id = 230mA

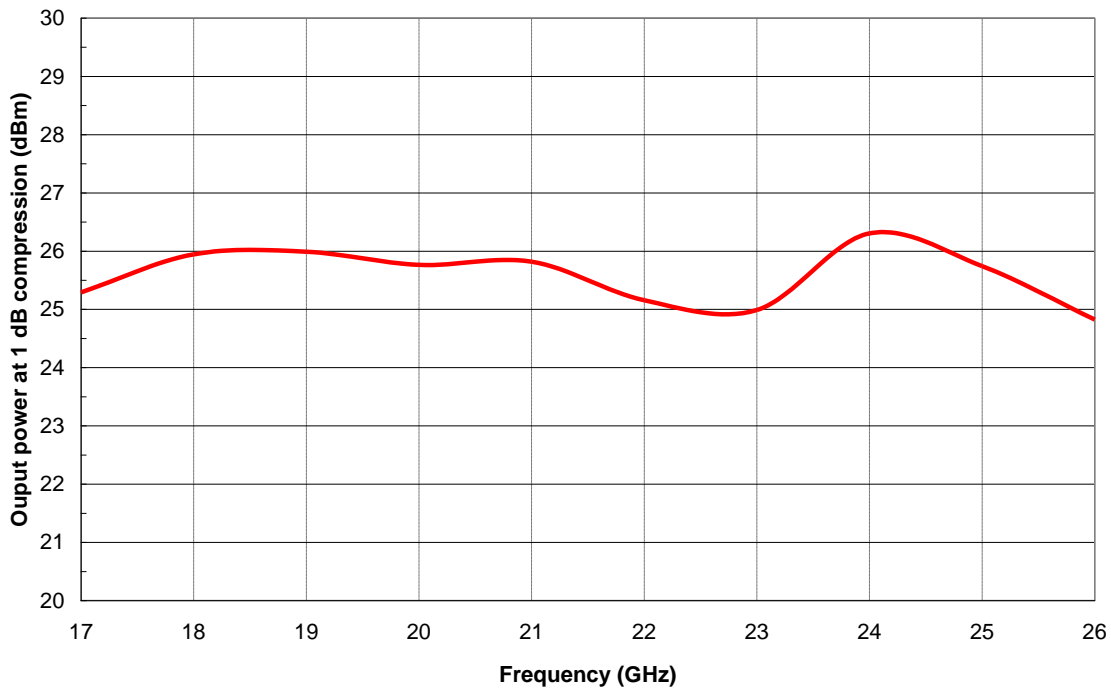
If no specific mention, the following values are representative of on board measurements (in QFN access planes) as defined on the paragraph "Evaluation mother board".



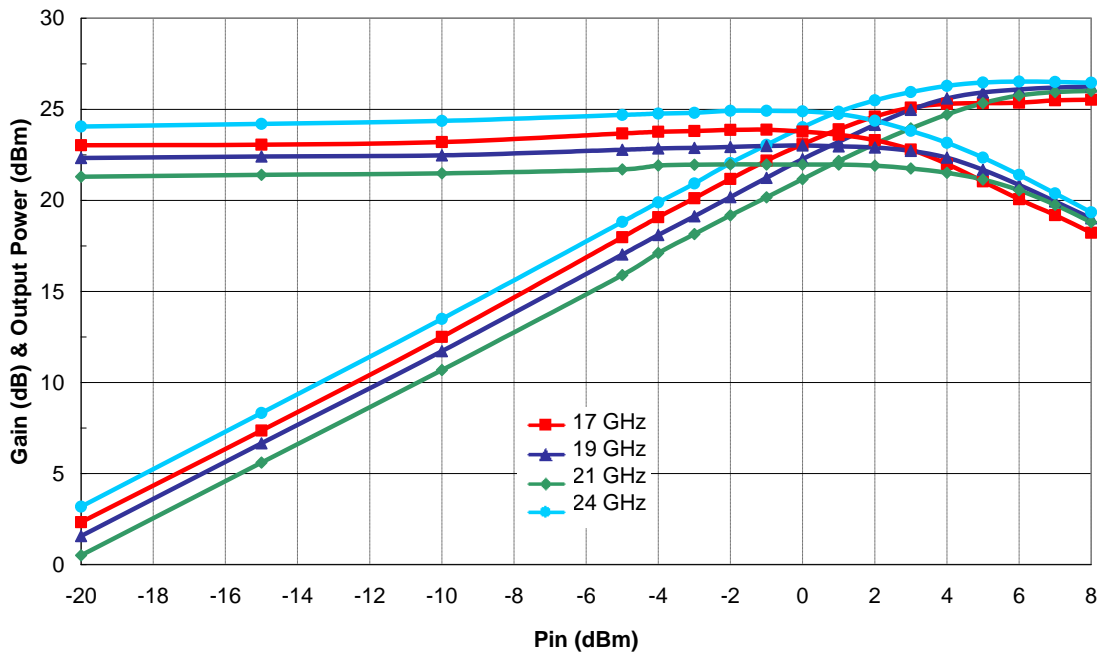
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Vg = -0.5V, Id = 230mA

Output Power at 1dB compression versus frequency



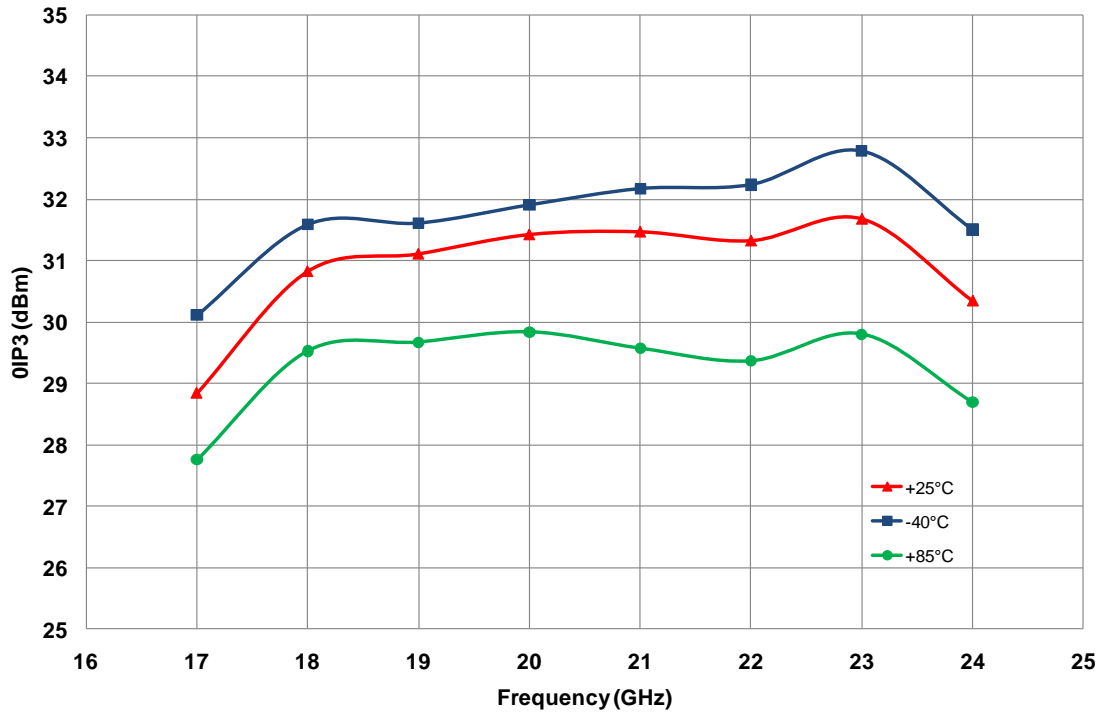
Gain & Output Power versus input power & frequency



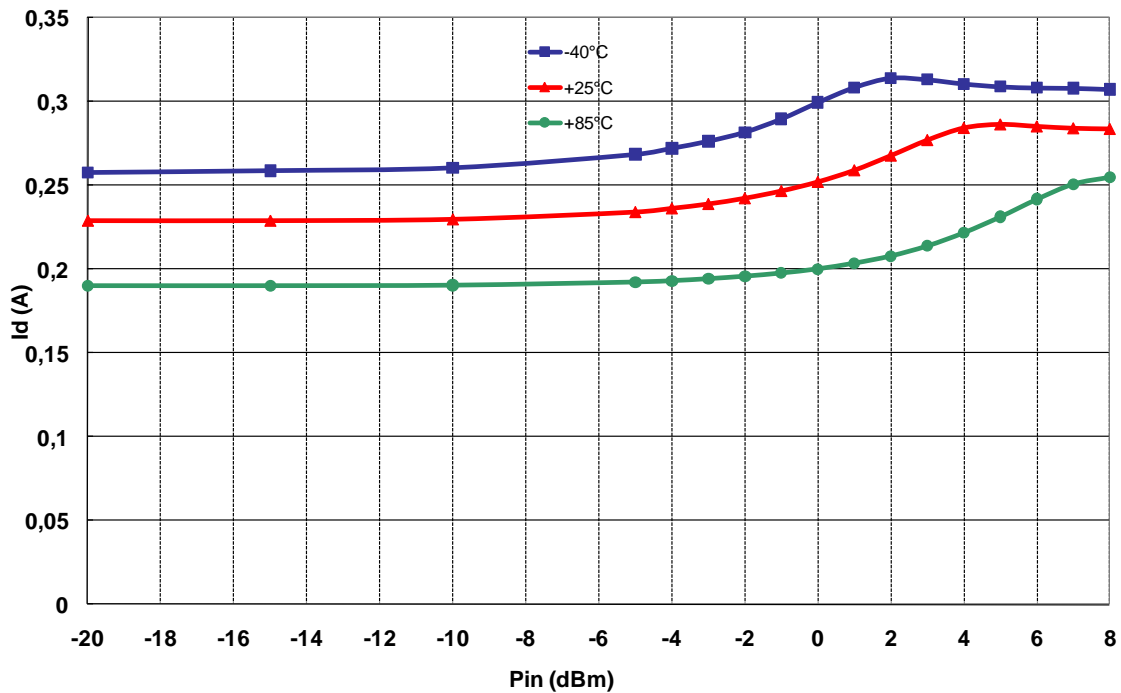
Typical Board Measurements

Vd = +6.0V, Vg = -0.5V, Id = 230mA

Output IP3 versus frequency & temperature



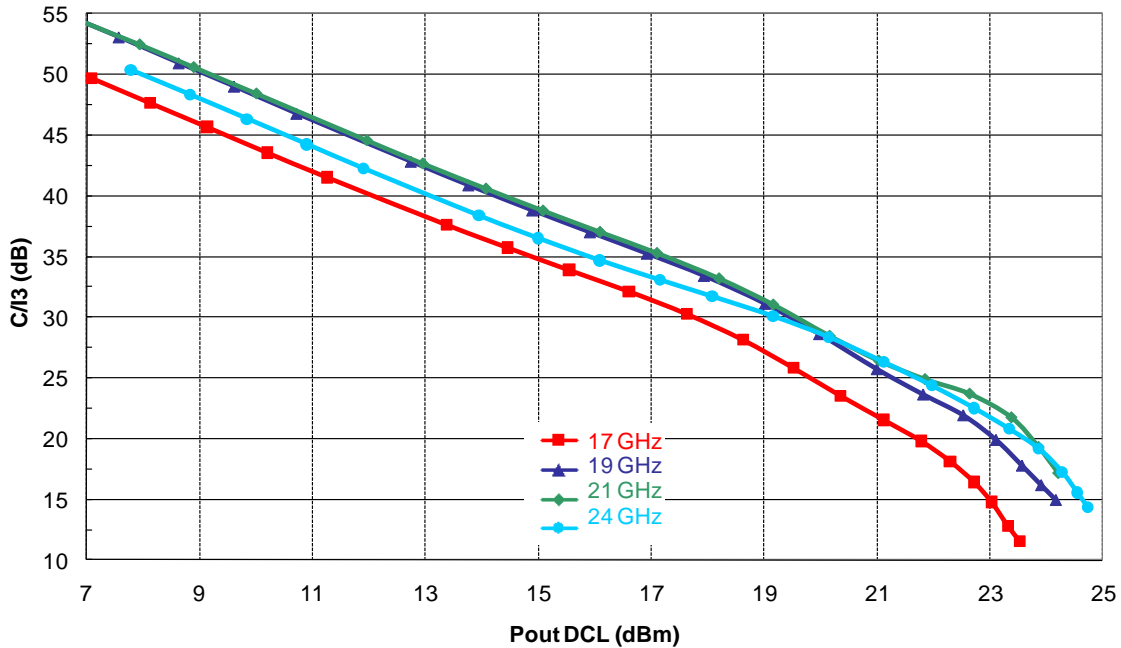
Drain current versus Input Power & temperature @ 20GHz



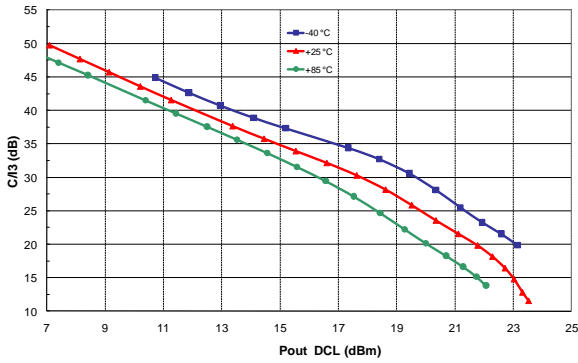
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Vg = -0.5V, Id = 230mA

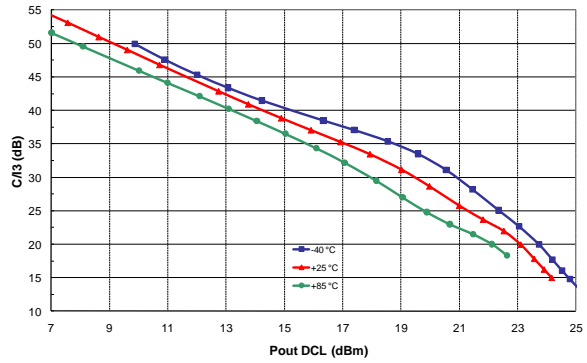
C/I3 versus Pout DCL & frequency at ambient temperature



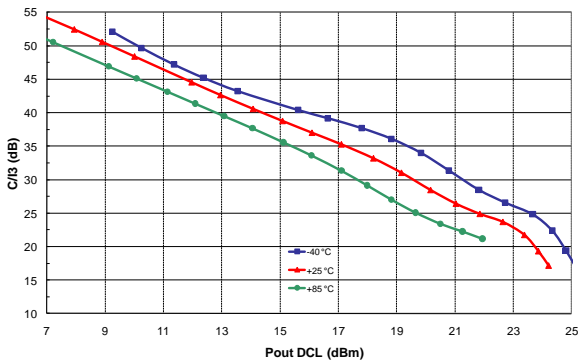
C/I3 versus Pout DCL at 17GHz



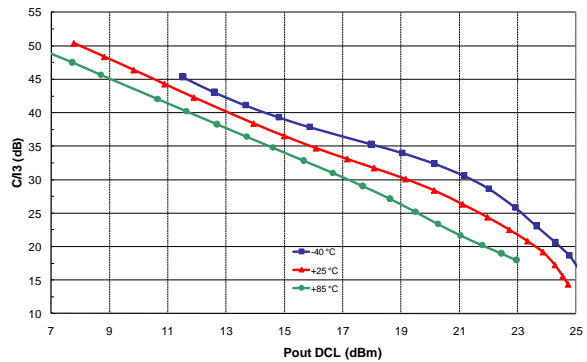
C/I3 versus Pout DCL at 19GHz



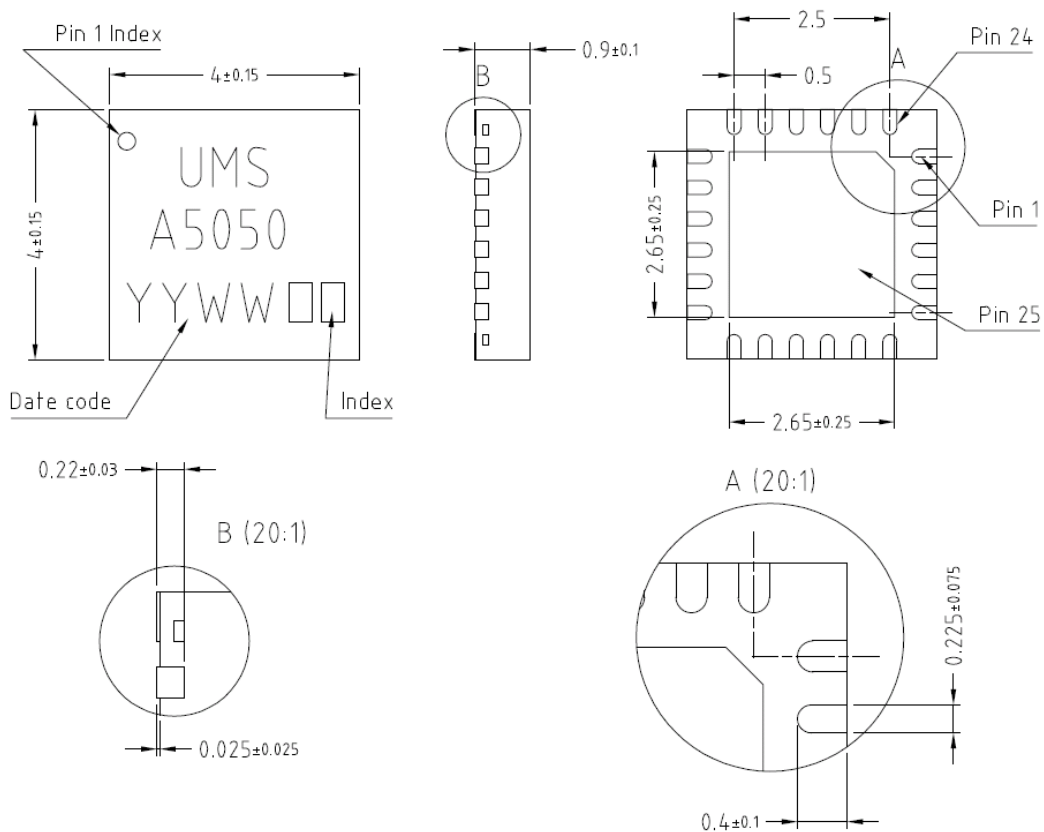
C/I3 versus Pout DCL at 21GHz



C/I3 versus Pout DCL at 24GHz



Package outline ⁽¹⁾



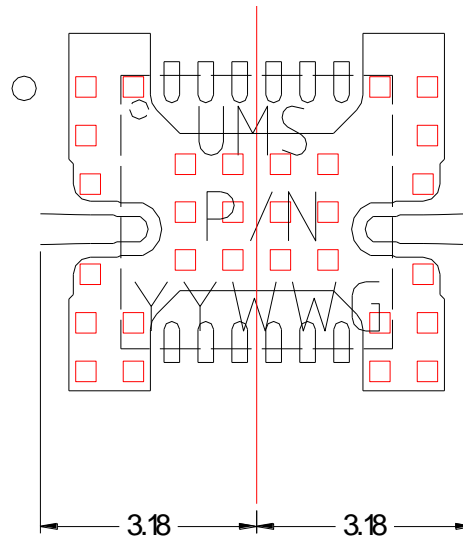
Matt tin, Lead Free	(Green)	1- Nc	9- Vd3	17- GND ⁽²⁾
Units :	mm	2- GND ⁽²⁾	10- Vd2	18- Nc
From the standard :	JEDEC MO-220	3- GND ⁽²⁾	11- GND ⁽²⁾	19- Nc
	(VGGD)	4- RF out	12- Vd1	20- Nc
	25- GND	5- GND ⁽²⁾	13- GND ⁽²⁾	21- Nc
		6- GND ⁽²⁾	14- GND ⁽²⁾	22- Vg
		7- Vd4	15- RF in	23- Nc
		8- GND ⁽²⁾	16- GND ⁽²⁾	24- Nc

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

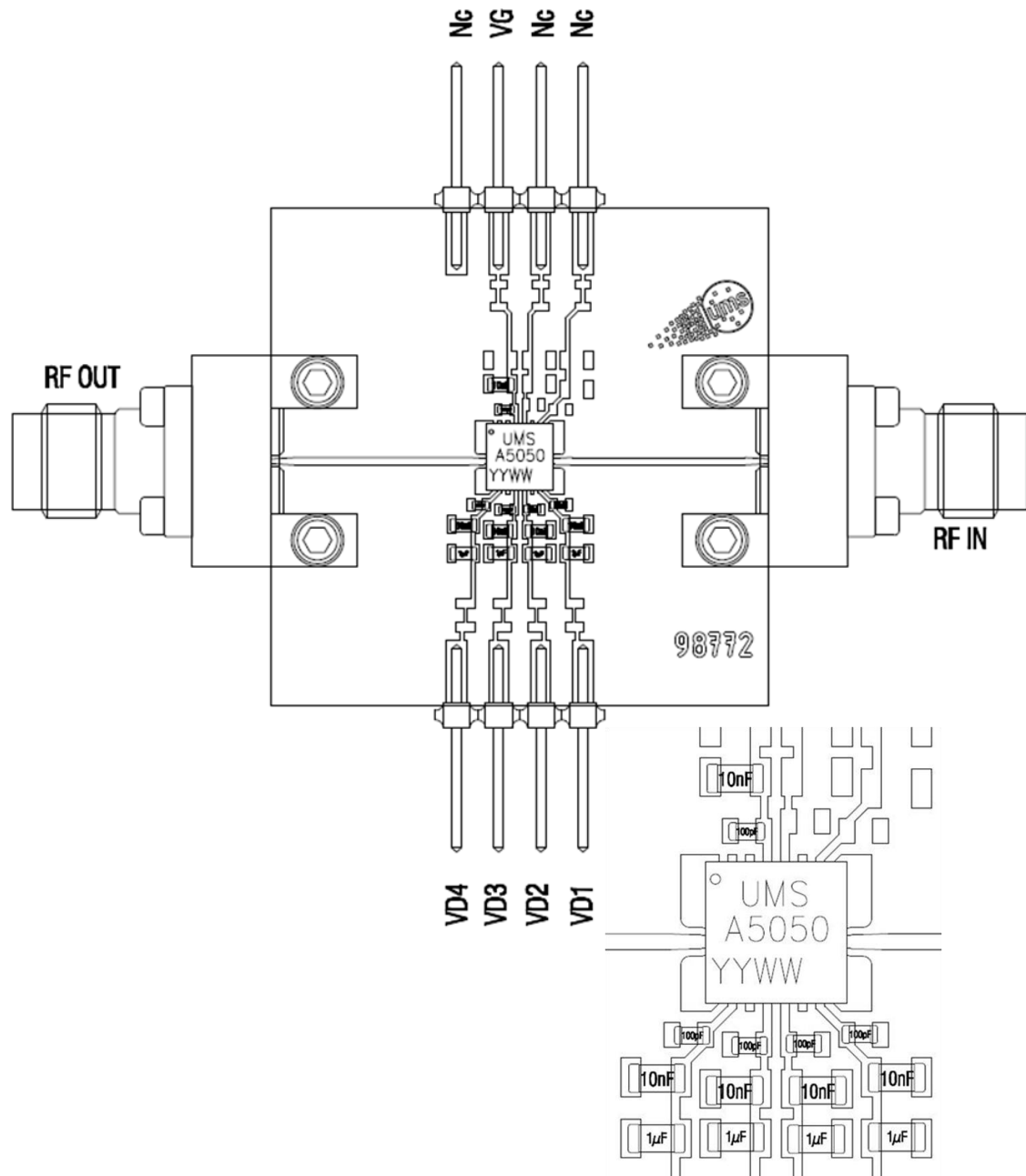
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".



Evaluation mother board

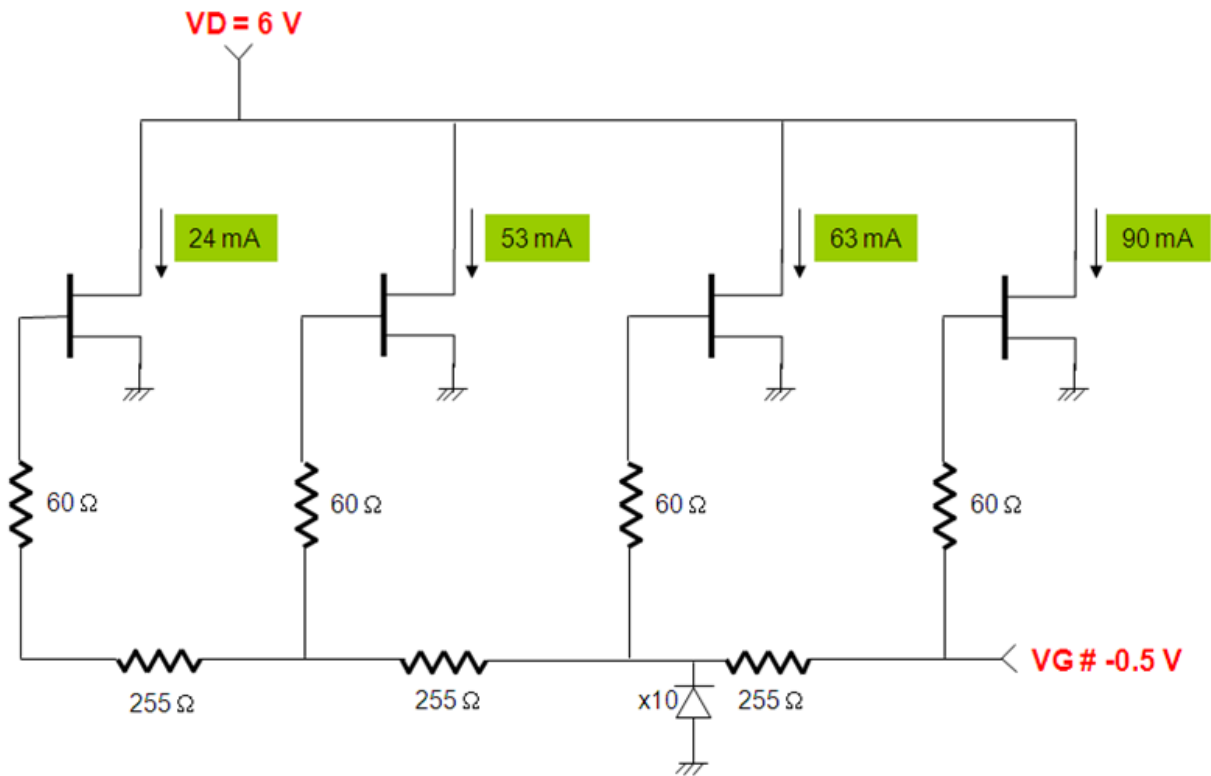
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF \pm 10%, 100pF \pm 5% and 1 μ F \pm 10% are recommended for all DC access.
- See application note AN0017 for details.



Notes

DC Schematic

$I_d = 230\text{mA}$



Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at <http://www.ums-gaas.com> for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 RoHS compliant package:

CHA5050-QDG/XY

Stick: XY = 20

Tape & reel: XY = 21

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.** Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**