XP1080-QU

Power Amplifier
37.0 - 40.0 GHz

Rev. V2

Features

- Linear Power Amplifier
- On-Chip Power Detector
- Output Power Adjust
- 25.0 dB Small Signal Gain
- +27.0 dBm P1dB Compression Point
- +38.0 dBm OIP3
- Lead-Free 7 mm 28-lead SMD Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

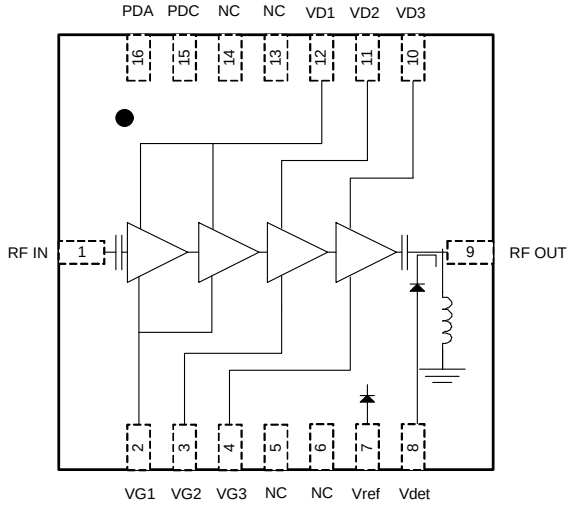
The XP1080-QU is a four stage 37.0-40.0 GHz packaged GaAs MMIC power amplifier that has a small signal gain of 25.0 dB with a +38.0 dBm Output Third Order Intercept. The amplifier contains an integrated, temperature compensated, on-chip power detector. This MMIC uses M/A-COM Technology Solutions' GaAs pHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity.

The device comes in a RoHS compliant 7x7mm QFN Surface Mount Package offering excellent RF and thermal properties. This device has been designed for use in 38 GHz Point-to-Point Microwave Radio applications.

Ordering Information

Part Number	Package
XP1080-QU-0N00	bulk quantity
XP1080-QU-0N0T	tape and reel
XP1080-QU-EV1	evaluation module

Functional Schematic



Pin Configuration [1]

Pin No.	Function	Pin No.	Function
1	RF Input	9	RF Output
2	Gate Bias, Stage 1	10	Drain Bias for Stage 3
3	Gate Bias, Stage 2	11	Drain Bias for Stage 2
4	Gate Bias, Stage 3	12	Drain Bias for Stage 1
5-6	Not Connected	13,14	Not Connected
7	Detector Reference Output	15	PDC
8	Detector Output	16	PDA

1. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Power Amplifier
37.0 - 40.0 GHz

Rev. V2

Electrical Specifications: 37-40.15 GHz (Ambient Temperature T = 25°C)

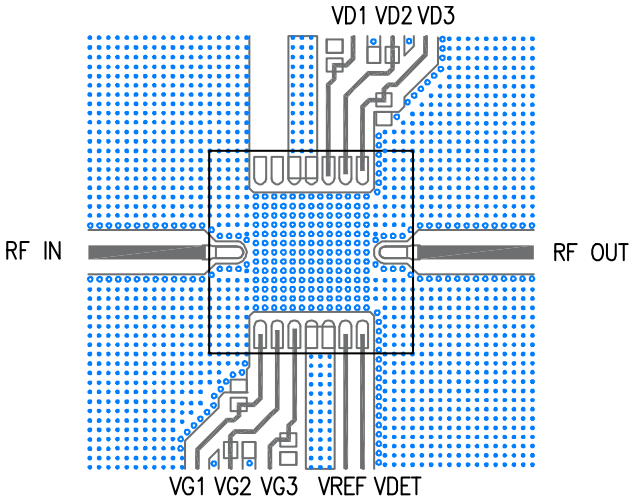
Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11)	dB	10.0	14.0	-
Output Return Loss (S22)	dB	4.0	8.0	-
Small Signal Gain (S21)	dB	21.0	25.0	30.0
Gain Flatness (ΔS21)	dB	-	+/-1.0	-
Reverse isolation (S12)	dB	-	50	-
Output Power for 1dB Compression Point (P1dB)	dBm	-	27.0	-
Output IMD3 with Pout (scl) = 14 dBm	dBc	43.0	48.0	-
Output IP3	dBm	35.5	+38.0	-
Drain Bias Voltage (Vd)	VDC	-	4.0	4.0
Gate Bias Voltage (Vg)	VDC	-1.0	-0.3	-0.1
Supply Current (Id1) (Vd=4.0V, Vg=-0.3V)	mA	-	1000	1200

Absolute Maximum Ratings [2,3]

Parameter	Absolute Max.
Supply Voltage (Vd)	+4.3 V
Gate Bias Voltage (Vg)	1.5 V < Vg < 0 V
Input Power (Pin)	15 dBm
Abs. Max Junction/Channel Temp	MTTF Graph 1
Max. Operating Junction/Channel Temp	175°C
Continuous Power Dissipation (Pdiss) at 85 °C	7.0 W
Thermal Resistance (Tchannel=150°C)	12°C/W
Operating Temperature (Ta)	-40°C to +85°C
Storage Temperature (Tstg)	-65°C to +150°C
Mounting Temperature	See solder reflow profile
ESD Min. - Machine Model (MM)	Class A
ESD Min. - Human Body Model (HBM)	Class 1A
MSL Level	MSL3

2. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.
3. For saturated performance it recommended that the sum of (2*Vdd + abs (Vgg)) <9V

Recommended Layout



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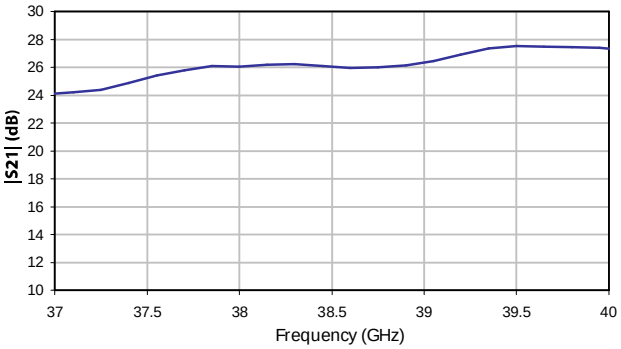
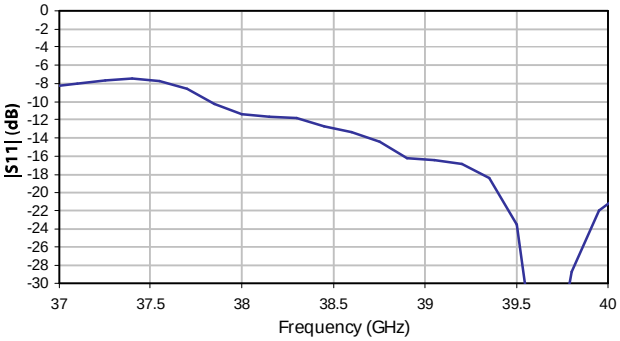
Typical Performance Curves

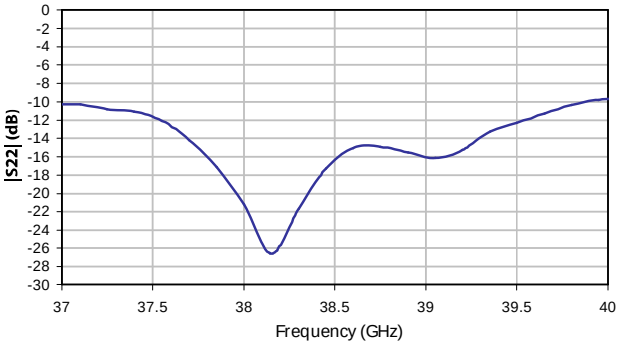
XP1080-QU-0N00: Small signal Gain (S21)
Vd=4.0V, Id=1000mA



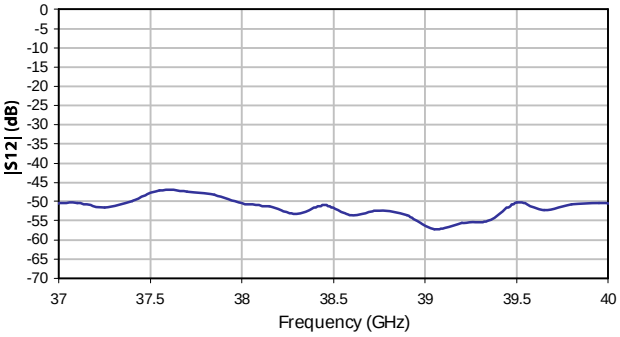
XP1080-QU-0N00: Input Return Loss (S11)
Vd=4.0V, Id=1000mA



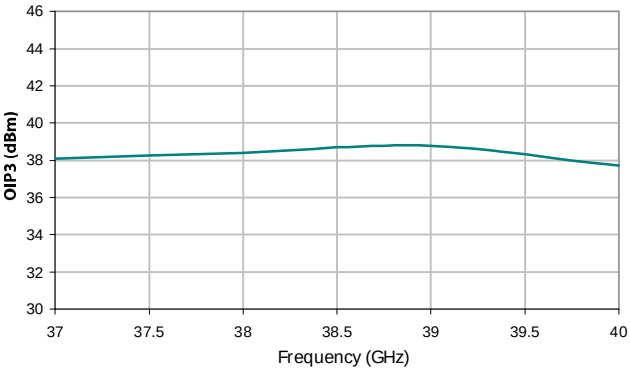
XP1080-QU-0N00: Output Return Loss (S22)
Vd=4.0V, Id=1000mA



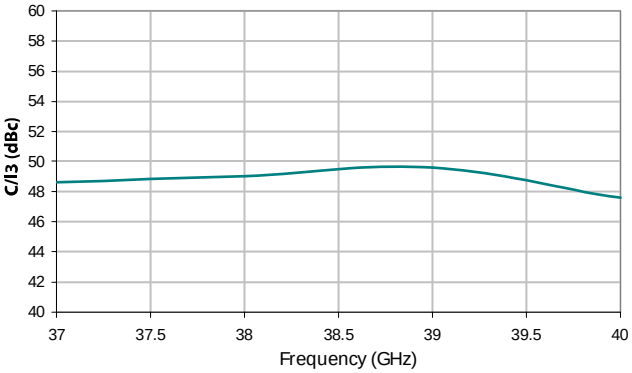
XP1080-QU-0N00: Reverse Isolation (S12)
Vd=4.0V, Id=1000mA



XP1080-QU-0N00; Output IP3 vs Freq
Vd=4V, Id=1000mA

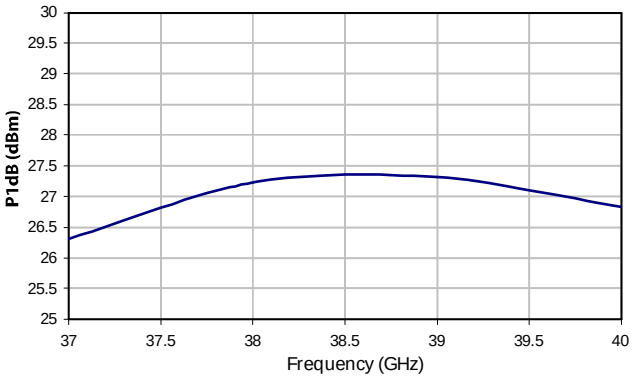


XP1080-QU-0N00; C/I3 vs Freq
Pscl=14dBm, Vd=4V, Id=1000mA

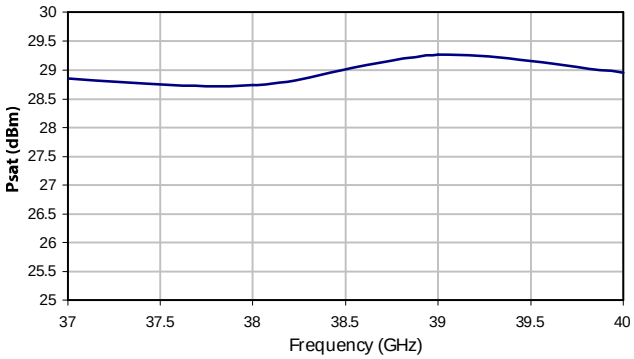


Typical Performance Curves (cont.)

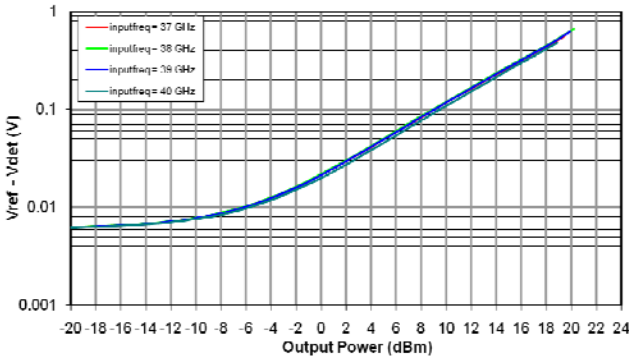
XP1080-QU: P1dB vs Freq
Vd=4V, Id=1000mA



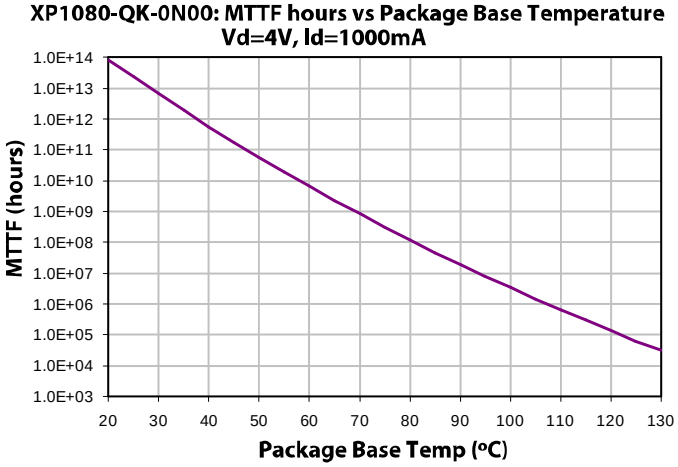
XP1080-QU: Psat vs Freq
Vd=4V, Id=1000mA

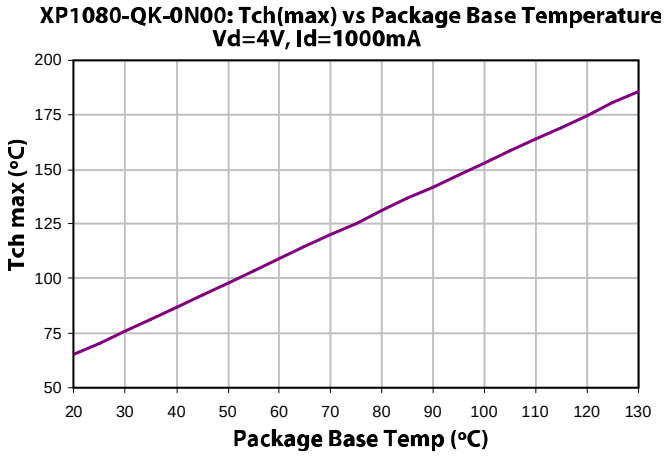


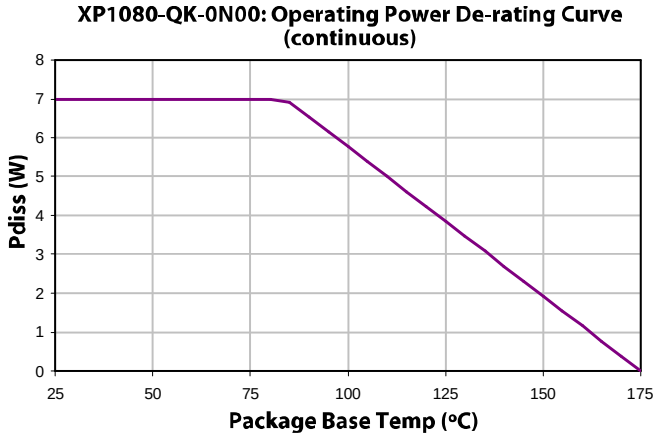
XP1080-QU: Detector Output (Diff) vs Freq
Vd=4V, Id=1000mA, Vdet/ref Bias = +5V/100k



MTTF



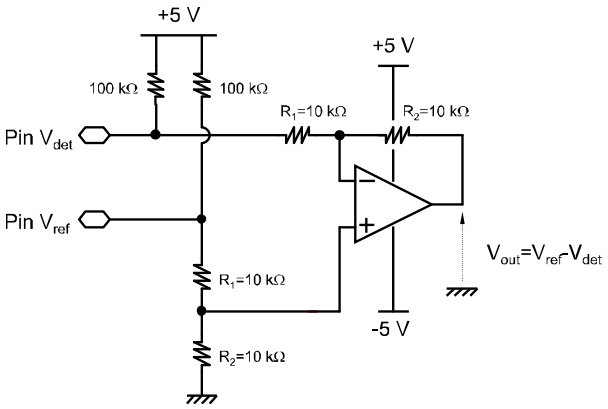




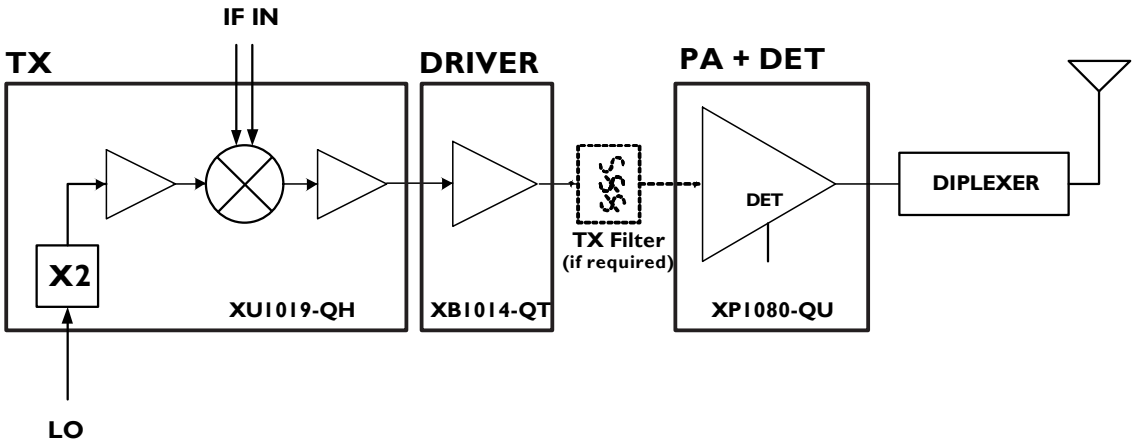
App Note [1] Biasing - It is recommended to bias the amplifier with Vd=4.0 V and Id=1000 mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.3V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement - Each DC pin (Vd1,2,3 and Vg1,2,3) needs to have DC bypass capacitance (10 nF/1 µF) as close to the package as possible.

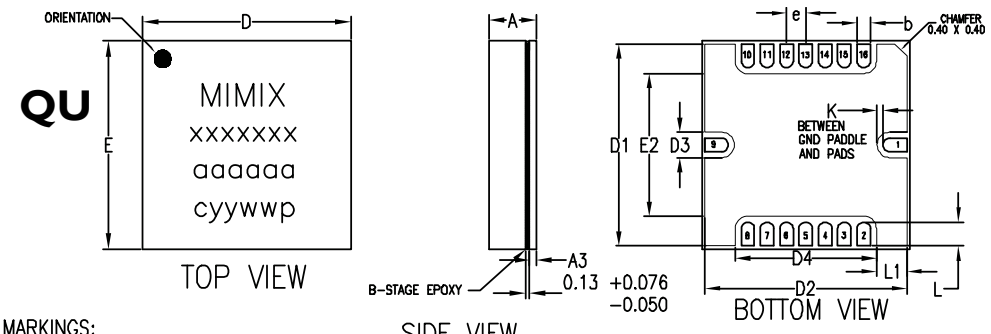
App Note [3] Power Detector - As shown in the schematic below, the power detector is implemented by providing +5 V bias and measuring the difference in output voltage with standard op-amp in a differential mode configuration.



Typical Application

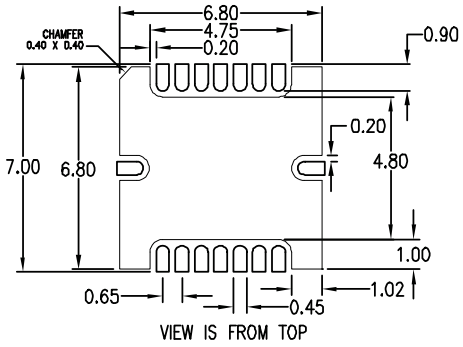


Lead-Free 7 mm 28-Lead SMD†



MARKINGS:
MIMIX PART/MODEL NO.
WAFER LOT NUMBER
DATE CODE = YYWW
C = COUNTRY OF ORIGIN
P = PLATING OPTION

GENERIC RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
DIMENSIONS ARE IN MM



DIMENSIONS ARE IN MM			
	MIN	TYP	MAX
A	1.48	1.58	1.68
A3		0.20	
b	0.40	0.45	0.50
K	–	0.20	–
D		7.00	
E		7.00	
D1	6.75	6.80	6.85
D3	0.80	0.85	0.90
D4	4.70	4.75	4.80
e		0.65	
D2	6.75	6.80	6.85
E2	4.75	4.80	4.85
L	0.75	0.80	0.85
L1	0.97	1.02	1.07

NOTES:
1. VIEWS ARE NOT TO SCALE: USE DIMENSIONS AND TABLE.
2. MARKINGS ARE FOR ILLUSTRATION PURPOSES ONLY. ACTUAL MARKINGS MAY VARY FOR EACH DEVICE TYPE MODULE.
3. ALL INFORMATION CONTAINED HEREIN IS GENERIC FOR USE WITH MIMIX BROADBAND APPLICATION NOTES AND SPECIFICATION DOCUMENTS FOR MIMIX BROADBAND DEVICES. INFORMATION MAY NOT REFLECT SPECIFIC REQUIREMENTS FOR EACH UNIQUE CIRCUIT DESIGN USING THIS PACKAGE TYPE.

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is 100% matte tin over copper.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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