

## Applications

- Base Station Receivers
- Tower Mount Amplifiers
- Repeaters
- FDD-LTE, TDD-LTE, WCDMA
- General Purpose Wireless

## Product Features

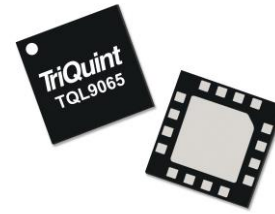
- 1.5 – 3.8 GHz Operational bandwidth
- 2<sup>nd</sup> stage LNA with integrated bypass mode
- Ability to turn LNA and bypass mode OFF
- Ultra low noise, 0.5 dB at 1.95 GHz
- 36 dB Gain at 1.95 GHz, 16 dB in Low Gain Mode
- +35 dBm Output IP3 in High Gain Mode
- +33 dBm Output IP3 in Low Gain Mode
- Internally matched
- Positive supply only, +3.3 to +5 V
- 3.5x3.5 mm 16-pin SMT package

## General Description

The TQL9065 is a high-linearity, ultra-low noise 2-stage gain block amplifier module with a bypass mode functionality integrated to the second stage in the product. At 1.95 GHz, the amplifier, under high gain mode, typically provides 36 dB gain, +35 dBm OIP3, and 0.5 dB noise figure while drawing 140 mA current from a +5V supply. The component also provides high performance in the low gain mode with 16 dB gain, 0.5dB noise figure and +33dBm OIP3 while drawing 67mA current.

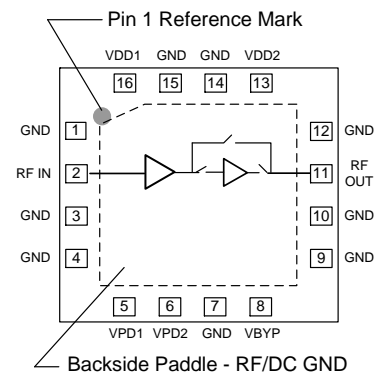
The TQL9065 is internally matched using a high performance E-pHEMT process. This low noise amplifier contains an internal active bias to maintain high performance over temperature.

The TQL9065 covers the 1.5–3.8 GHz frequency band and is targeted for wireless infrastructure. The TQL9065 is housed in a 3.5 x 3.5 mm SMT package.



16-pin 3.5 x 3.5 mm Package

## Functional Block Diagram



## Pin Configuration

Pin No.	Label
1,3,4,7,9,10,12,14,15	GND
2	RFin
5	V <sub>PD1</sub>
6	V <sub>PD2</sub>
8	V <sub>BYP</sub>
11	RFout
13	V <sub>DD2</sub>
16	V <sub>DD1</sub>
Backside Paddle	RF/DC GND

## Ordering Information

Part No.	Description
TQL9065	2-stage Bypass LNA
TQL9065-PCB	1.5-2.7 GHz Evaluation Board

Standard T/R size = 2500 pieces on a 7" reel

### Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
Drain Voltage (V <sub>DD</sub> )	+7 V
Input Power (CW)	+22 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

### Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V <sub>DD</sub> )	+3.3	+5.0	+5.25	V
Operating Temp. Range	-40		+85	°C
T <sub>ch</sub> (for >10 <sup>6</sup> hrs MTTF)			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

### Electrical Specifications

Test conditions unless otherwise noted: V<sub>DD</sub> = +5 V, Temp. = +25°C.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1500		3800	MHz
Test Frequency			1950		MHz
Gain	LNAs ON, Bypass OFF		36		dB
Input Return Loss	LNAs ON, Bypass OFF		15		dB
Output Return Loss	LNAs ON, Bypass OFF		13		dB
Noise Figure	LNAs ON, Bypass OFF		0.55		dB
Output P1dB	LNAs ON, Bypass OFF		+20		dBm
Output IP3	LNAs ON, Bypass OFF, P <sub>out</sub> =+5 dBm/tone, Δf=1 MHz		+35		dBm
Gain	LNA1 ON, Bypass ON		16		dB
Input Return Loss	LNA1 ON, Bypass ON		20		dB
Output Return Loss	LNA1 ON, Bypass ON		11		dB
Noise Figure	LNA1 ON, Bypass ON		0.55		dB
Output P1dB	LNA1 ON, Bypass ON		+18		dBm
Output IP3	LNA1 ON, Bypass ON, P <sub>out</sub> =+5 dBm/tone, Δf=1 MHz		+33		dBm
Control Voltage, V <sub>PD</sub> , V <sub>BYP</sub> <sup>(1)</sup>	V <sub>IH</sub>	1.6		V <sub>DD</sub>	V
	V <sub>IL</sub>	0		0.5	V
Current, I <sub>D</sub>	LNAs ON, Bypass OFF		155		mA
	LNA1 ON, Bypass ON		65		mA
Thermal Resistance, θ <sub>jc</sub>	Channel to case		TBD		°C/W

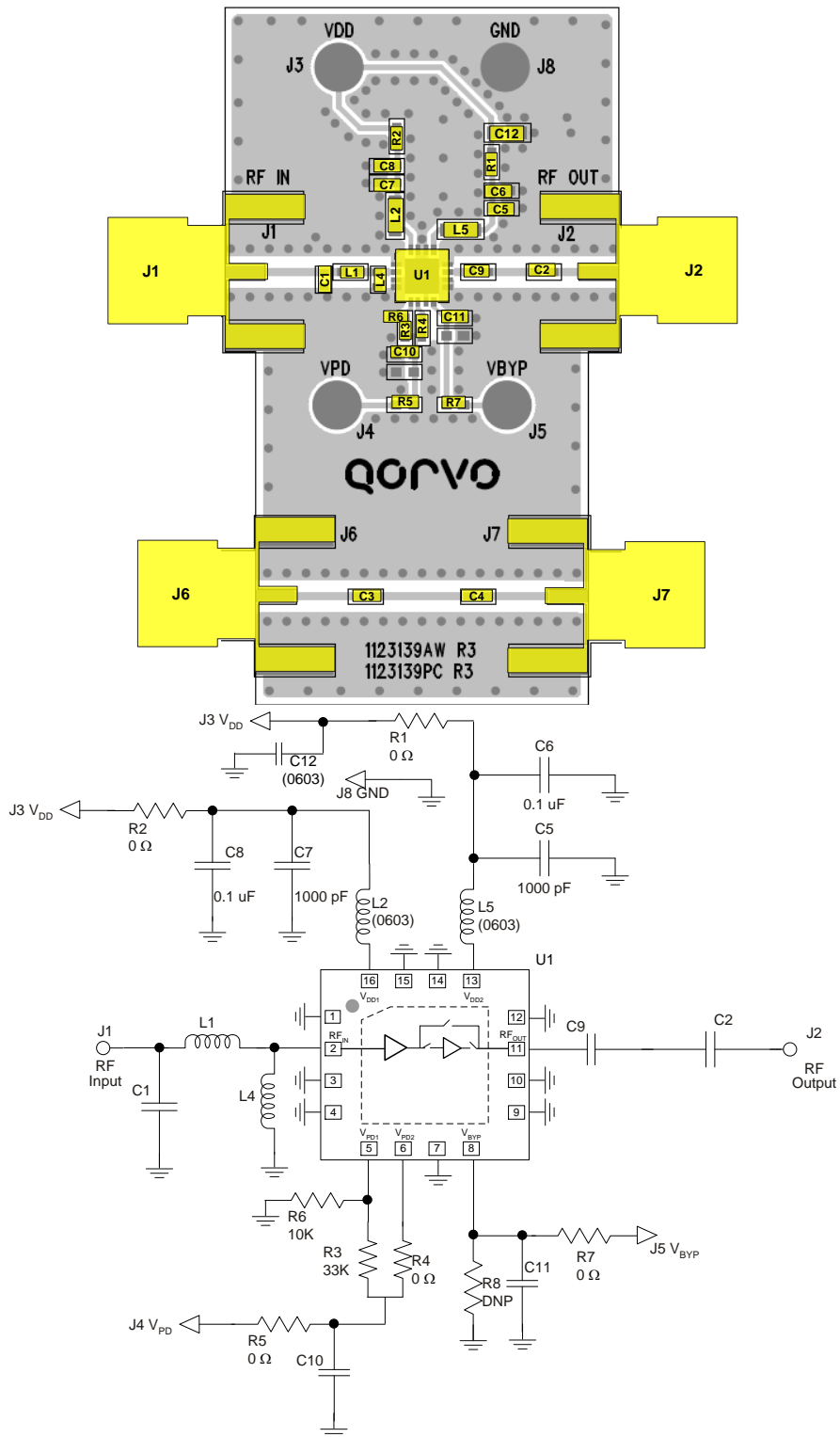
Notes:

1. These voltages are reference at the turrets labelled V<sub>PD</sub> and V<sub>BYP</sub> on the circuit schematic on page 3.

### Control Truth Table

V <sub>PD1</sub>	V <sub>PD2</sub>	V <sub>BYP</sub>	State
1	1	0	LNA1 OFF, LNA2 OFF, Bypass OFF
0	0	0	LNA1 ON, LNA2 ON, Bypass OFF
0	x	1	LNA1 ON, LNA2 OFF, Bypass ON
1	x	1	LNA1 OFF, LNA2 OFF, Bypass ON

TQL9065-PCB Evaluation Board



See Evaluation Board PCB Information section for PCB material and stack-up.

### Bill of Material – TQL9065-PCB

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	PCB	Qorvo	1123139
U1	n/a	2-Stage Bypass LNA	Qorvo	TQL9065
R1, 2, 4, 5, 7, C2	0 Ω	RES, 0402, +/-5%, 1/16W	Various	
R3	33K	RES, 0402, 5%, 1/16W	Various	
R6	10K	RES, 0402, 5%, 1/16W	Various	
C1	0.5 pF	CAP, 0402, +/-0.1pF, 50V, C0G	Murata	GJM1555C1HR50BB01
L1	1.5 nH	IND, 0402, +/-0.1nH	Murata	LQP15MN1N5B02D
L4	6.8 nH	IND, 0402, 5%	Murata	LQG15HS6N8J02
C3, 4, 5, 7, 9, 10, 11	100 pF	CAP, 0402, +/-5%, 50V	Various	
C6, 8	0.1 uF	CAP, 0402, 20%, 16V, Y5V	Various	
C12	4.7 uF	CAP, 0603, 20%, 10V, Y5V	Various	
L2	5.6 nH	IND, 0603, 5%, 700mA	Coilcraft	0603CS-5N6XJLU
L5	18 nH	IND, 0603, 5%	Coilcraft	0603CS-18NXJL

### Typical Performance - High Gain Mode (LNA1 ON, LNA2 ON, Bypass OFF)

Test conditions unless otherwise noted:  $V_{DD1} = V_{DD2} = +5\text{ V}$ ,  $V_{PD} = 0.5\text{ V}$ ,  $V_{BYP} = 0.5\text{ V}$ ,  $I_D = 140\text{ mA}$ ,  $\text{Temp.} = +25\text{ }^\circ\text{C}$ .

Parameter	Typical Value			Units
Frequency	1800	2200	2600	MHz
Gain	37.5	34.7	33	dB
Noise Figure	0.50	0.60	0.65	dB
Input Return Loss	16.5	15.5	17	dB
Output Return Loss	14	14.3	12	dB
OIP3 (Pout/tone=+5 dBm, $\Delta f = 1\text{ MHz}$ )	+37.2	+37.2	+36.7	dBm
P1dB	+22.1	+21.6	+21.1	dBm

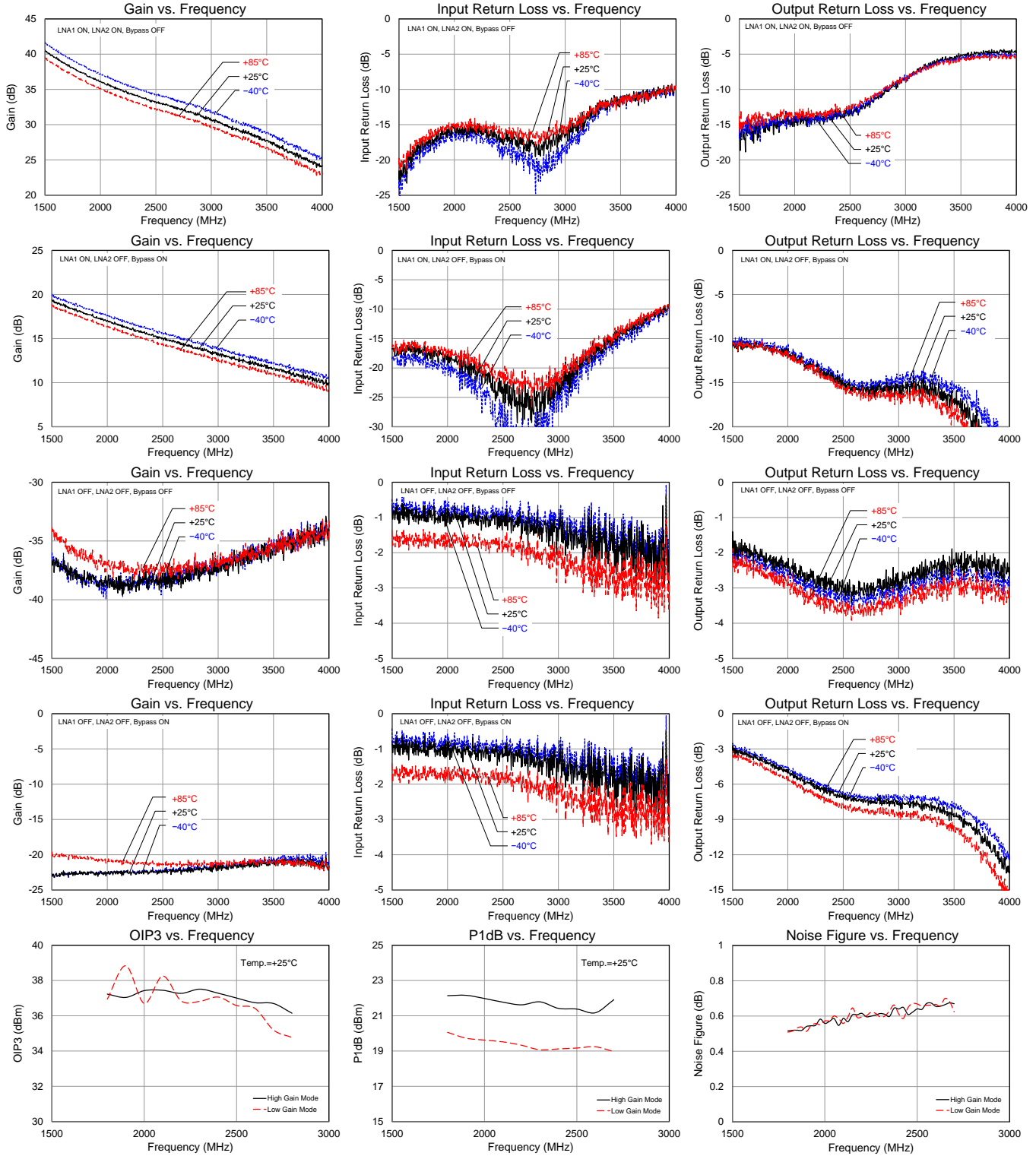
### Typical Performance - Low Gain Mode (LNA1 ON, LNA2 OFF, Bypass ON)

Test conditions unless otherwise noted:  $V_{DD1} = V_{DD2} = +5\text{ V}$ ,  $V_{PD} = 0.5\text{ V}$ ,  $V_{BYP} = 1.8\text{ V}$ ,  $I_D = 67\text{ mA}$ ,  $\text{Temp.} = +25\text{ }^\circ\text{C}$ .

Parameter	Typical Value			Units
Frequency	1800	2200	2600	MHz
Gain	17.8	16	13.3	dB
Noise Figure	0.50	0.50	0.50	dB
Input Return Loss	16.5	20	24	dB
Output Return Loss	11	13.5	16	dB
Output IP3 (Pout/tone=+5 dBm, $\Delta f = 1\text{ MHz}$ )	+36.9	+36.8	+36.4	dBm
P1dB	+20	+19.3	+19.2	dBm

Performance Plots

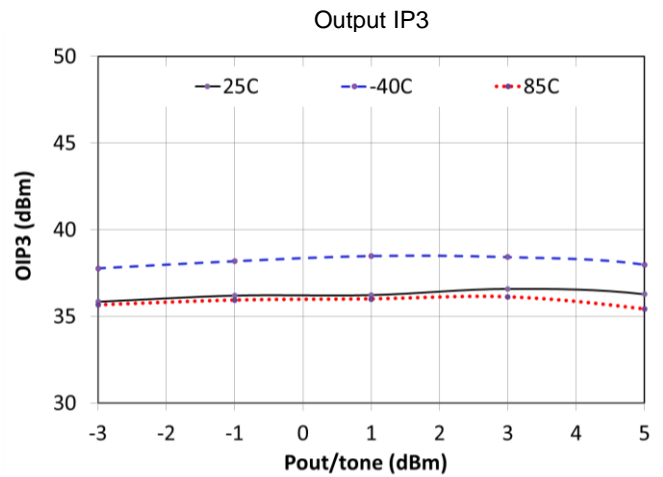
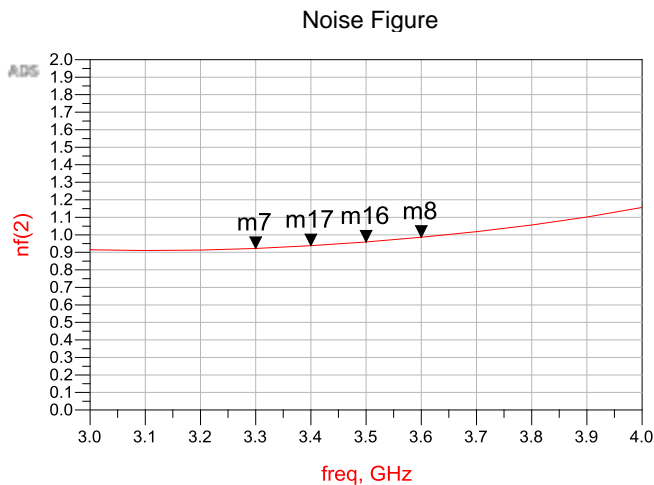
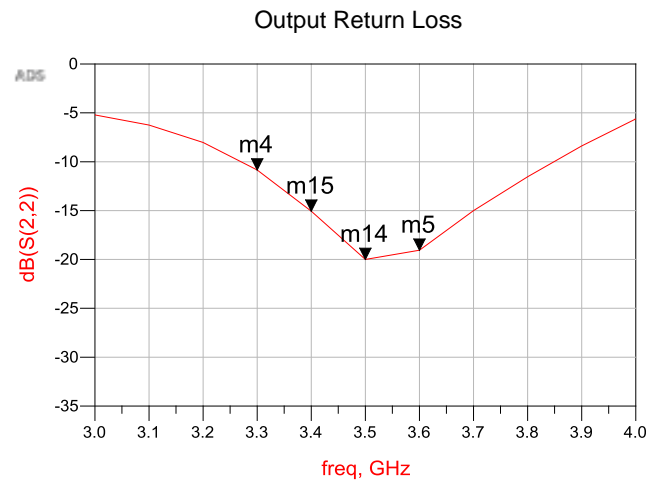
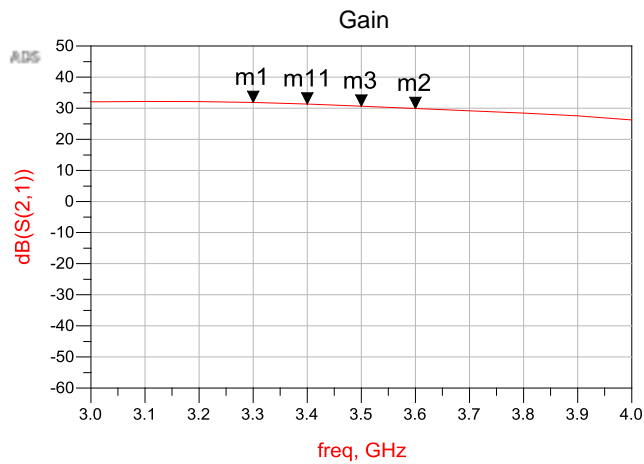
Test conditions unless otherwise noted:  $V_{DD1} = V_{DD2} = +5\text{ V}$



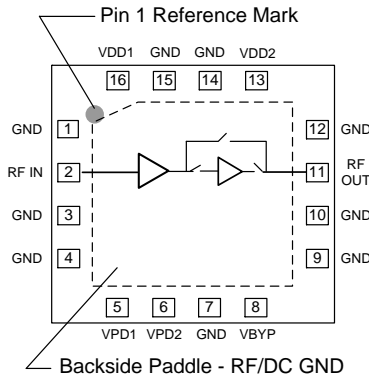
**Expected Performance (based on Simulations) - High Gain Mode**

Test conditions unless otherwise noted:  $V_{DD1} = V_{DD2} = +5\text{ V}$ ,  $V_{PD} = 0.5\text{ V}$ ,  $V_{BYP} = 0.5\text{ V}$ ,  $I_D = 140\text{ mA}$ ,  $Temp. = +25\text{ }^\circ\text{C}$ .

Parameter	Typical Value			Units
Frequency	3400	3500	3600	MHz
Gain	31.3	30.6	29.9	dB
Noise Figure	0.94	0.96	0.99	dB
Output Return Loss	15	20	19	dB
OIP3 (Pout/tone=+5 dBm, $\Delta f = 1\text{ MHz}$ )	+36	+36	+36	dBm
P1dB	+19	+19	+19	dBm



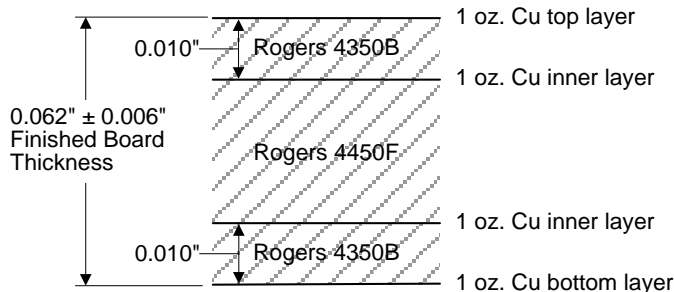
**Pin Configuration and Description**



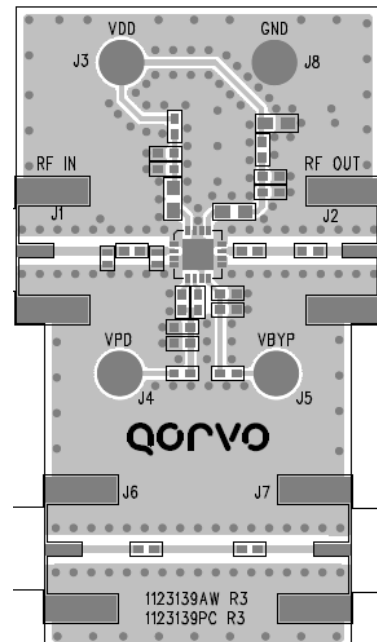
Pin No.	Label	Description
1,3,4,7,9,10,12,14,15	GND	RF/DC Ground pin.
2	RFin	RF input pin. DC block required.
5	VPD1	Power Down control for LNA1. Refer to truth table on pg. 2.
6	VPD2	Power Down control for LNA2. Refer to truth table on pg. 2.
8	VBYP	Bypass mode enable pin for LNA2. Refer to truth table on pg. 2.
11	RFout	RF output pin. DC block required.
13	VDD2	Supply voltage pin for LNA2.
16	VDD1	Supply voltage pin for LNA1.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

**Evaluation Board PCB Information**

TriQuint PCB 1123139 Material and Stack-up



50 ohm line dimensions: width = .020", spacing = .032"

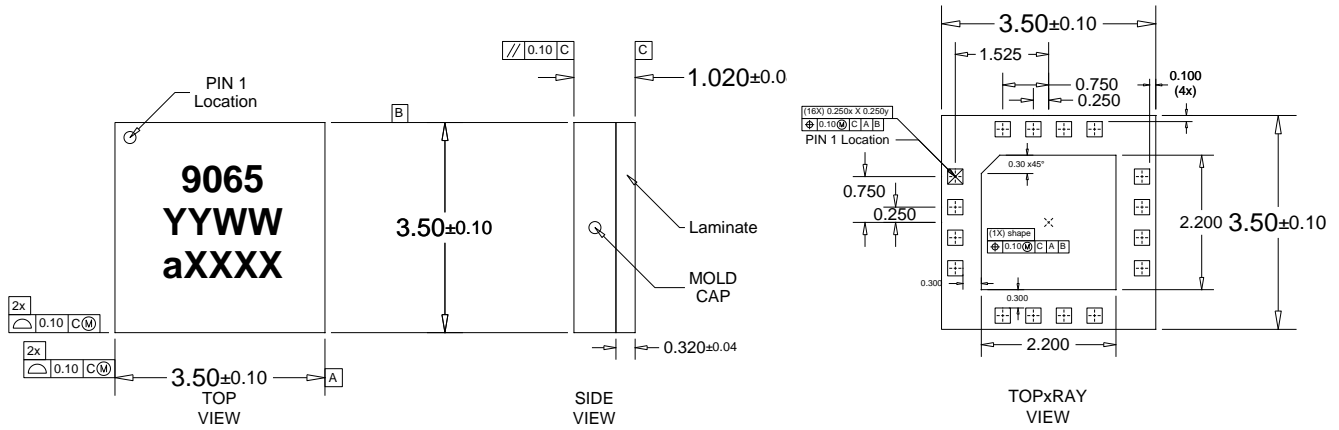




**Mechanical Information**

**Package Marking and Dimensions**

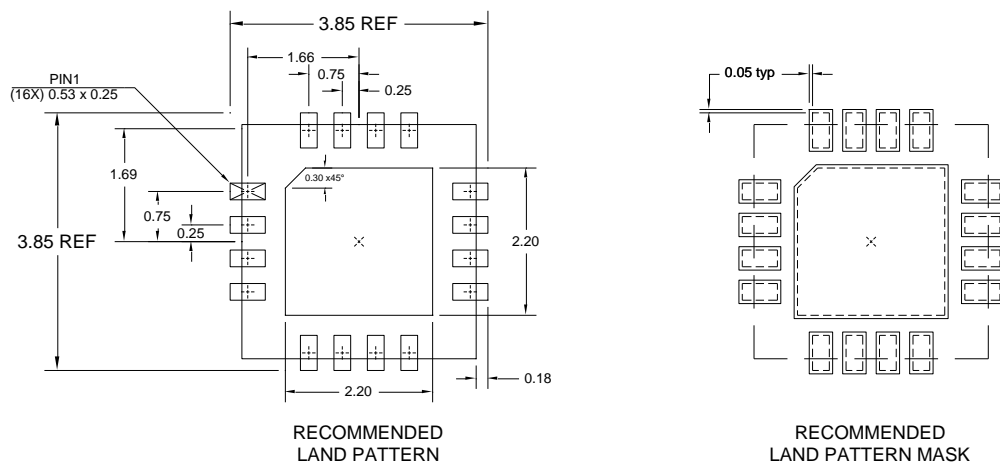
Marking: Part number – 9065  
Year/Week – YYWW  
Lot Code – aXXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-229.
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

**PCB Mounting Pattern**



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

## Product Compliance Information

### ESD Sensitivity



Caution! ESD-Sensitive Device

ESD Rating: TBD  
Value:  
Test: Human Body Model (HBM)  
Standard: JEDEC Standard JS-001-2012

ESD Rating: TBD  
Value:  
Test: Charged Device Model (CDM)  
Standard: JEDEC Standard JESD22-C101F

### MSL Rating

MSL Rating: Level 1  
Test: 260°C convection reflow  
Standard: JEDEC Standard IPC/JEDEC J-STD-020

### Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

Package contact plating: Electrolytic plated Au over Ni.

### RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

For information about the merger of RFMD and TriQuint as Qorvo:

**Web:** [www.qorvo.com](http://www.qorvo.com)

For technical questions and application information:

**Email:** [sjcapplcations.engineering@qorvo.com](mailto:sjcapplcations.engineering@qorvo.com)

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